早稲田大学大学院理工学研究科

博 士 論 文 概 要

論 文 題 目

**RESEARCH ON
CAD ALGORITHMS APPLIED FOR ANALOG IC
LAYOUT GENERATION**

アナログICレイアウト生成用
CADアルゴリズムに関する研究

申 請 者

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A large class of Application Specific ICs (ASIC) that are currently designed involve a combination of analog as well as digital circuits. Unlike digital circuits, the performance of analog circuits is strongly influenced by their layout, which represents a bottleneck to analog design automation. The primary concerns here are the effects of device mismatches, parasitics, and noise couplings on analog circuit performance degradation. To overcome these effects, performance specifications are usually translated into physical constraints such as symmetry, common orientation, and distance constraints among certain components. Then, the layout design of custom analog circuits and analog part of mixed analog/ digital circuits is done manually by experienced layout designers. Unfortunately, the manual design is time consuming and highly labor intensive process.
Recently, automatic digital layout tools are adopted and modified to deal with the imposed performance constraints on the analog layout. However, the above mentioned analog layout concerns still have not been fully and systematically handled yet. Most of existing systems are characterized by the use of stochastic optimization techniques based placement, grid based or channel routers, and lack of compaction. Hence, in order to deal with the analog layout constraints efficiently, a new analog layout system is essential. The objective of this thesis is to show that the heuristic techniques can be employed effectively to enhance CAD algorithms to devise that system.

In this thesis, a layout design system which consists of automatic and interactive algorithms for analog circuit element generation, placement, routing, and spacing is presented. The proposed automatic algorithms consider the analog oriented constraints, which are important from an analog layout point of view, and reduce the computation cost.Interactive algorithms allow the designer to control the layout design process and support the analog layout constraints. The automatic and interactive functions are fully integrated via a proposed analog layout data management system. The system is easily accessed through a proposed graphical user interface. This interface hides the supporting hardware and software, and lets the designer switch functions and modes rapidly and smoothly.

Analog Layout Data Management System (ADMS) is introduced to manage the layout design data, to control the information flow through the system and as communication interface among different modules of the system.

The automatic element generation algorithm has two parts: a procedural generator for single elements and a geometry specific generator for analog structures (e.g. common centroid). It reads technology and netlist files and generates the mask layout of elements, simulation model parameters and bounding box information needed by the placer and the router.

The automatic placement algorithm is based on a force directed method and consists of two main phases, each of which includes a tuning procedure. In the first phase, we solve a set of simultaneous linear equations, based upon attractive forces. These attractive forces represent the interconnection topology of given blocks and some specified constraints. Symmetry constraint is considered throughout the tuning procedure. In the second phase, block overlap resulting from the first phase is resolved iteratively, where each iteration is followed by the symmetry tuning procedure.

Linear and quadratic objective functions have been employed in the placement algorithm. An evaluation process is carried out for these two functions in terms of computation time and analog constraints satisfaction.

Automatic routing is performed using a line expansion based gridless router. Routing constraints are taken into account and several routing priorities are imposed on input nets. Avoiding cross talk is considered through the evaluation of a cost function, while symmetry routing is treated using a specific technique.

The automatic spacer employs a constraint graph based algorithm while considering the analog symmetry constraints. It performs the compaction in one direction at a time and provides the final layout as its output. Unlike other spacers, which used linear programming methods to solve the symmetry problem, it uses a graph based algorithm to deal with this problem.

"Interactive" means that interactive layout systems allow the designer to create circuit primitives (e.g. current mirror), to swap alternate instances of a functional block (element, primitive) in a placement area, to route a specific net, to move blocks or wire segments in an already place_ routed layout maintaining interconnections between blocks, etc., by using interactive functions on the CRT without any design rules violations. Interactive algorithms are proposed to achieve these interactive functions. An efficient sketch routing algorithm is proposed to deal with some interactive functions.

The automatic algorithms as well as ADMS are implemented and integrated as an automatic analog layout design system. Experimental results for two OP AMPs, one provided by MCNC (Microelectronics Center of North Carolina) as benchmark data and the other from text books, are shown to demonstrate the performance of the algorithms. From the experimental results, it is verified that the presented system achieves analog constraints satisfaction within reasonable CPU time.

The thesis is devided into five parts. The first part deals with introducing the subject of VLSI physical design as well as the objective of the thesis. In the second part, the problem specification, existing solutions and proposed one are discussed. The third part presents the proposed automatic analog layout algorithms for element generation, placement, routing, and spacing. Interactive commands and algorithms are described in the forth part. The fifth part deals with the experimental evaluation of the system developed in this research using benchmark analog circuits. Each part is represented by a chapter. The summaries of each chapter are shown one by one as follows.

In chapter 1, current CAD approaches for VLSI (Very Large Scale Integrated circuits) are summarized. The physical design of VLSI is reviewed. The objective of the thesis is stated.

Analog circuit design process in general and the position of layout problem within it as well as related problems are discussed in Chapter 2. Then analog layout problem statement, review of existing solutions and the proposed solution are presented. To implement a complete analog circuit design system, either constraint generation or analog circuit synthesis needs knowledge-based system which will be the future extension of the presented system.

Chapter 3 describes the proposed automatic algorithms for analog layout system: element generator, placer, router, and spacer. The element generator expresses flexibility in parameterizing several elements and producing several views for the same element. While placer, router and compactor programms satisfy user specified analog constraints, the CPU time consumed is reasonable. The discussion of the placement objective function shows that the linear objective function is more suitable for handling the analog objectives. In routing, the use of gridless line expansion algorithm allows symmetry routing, which none of channel router based systems seem able to perform in separated channels. It also can handle variable widths of wiring. In spacing, the implemented constraint graph based compactor handles the symmetry problem efficiently. Extended Bellman-Ford or

DBR algorithms are candidates for the implementation to support spacing with design rule violations.

Chapter 4 presents the interactive algorithms of the analog layout system. Interactive commands as well as user interface are described. Algorithms for interactive routing and spacing commands are presented. In this chapter, an O(n log s log n) spoke creation algorithm (where n is the number of line segments and s is the number of spokes), which is applied as routability testing as well as routing algorithm of a sketch, is presented. Based on enhanced plane sweep, the same algorithm is described to avoid the polar scanning technique and its associated floating point operations. The presented algorithm is much more better than the already known algorithm $O(n^2 \log n)$.

Chapter 5 presents the implementation and experimental results of the proposed analog layout system. Two examples are chosen to demonstrate the analog layout system, which is proposed in Chapter 3. The first example is an Op amp with eleven transistors. This is the only analog circuit example provided by MCNC benchmark. The other one is a typical Op amp with nineteen transistors which can be found in text books. The reported experimental results show that the imposed analog constraints on both examples are satisfied. Again, the first Op amp example is used to evaluate the placement algorithm performance in two cases of objective function: linear and quadratic. It has been shown that the linear objective function yields better results in terms of analog constraint satisfaction and computation cost.

The last chapter is devoted to conclusion. The future work is also included in this chapter. The implemented automatic system satisfies user specified analog oriented geometrical constraints within a reasonable time. Linear objective function is proved to be the most suitable for analog analytic placement. A new efficient algorithm for routing a sketch is presented. The extension of the implemented analog compactor to analog spacer, using of mixed analytical- knowledge based approach to generate the analog constraints from the required analog circuit performance and implementation of interactive algorithms are mentioned as future work.