博士論文概要

論文題目

Research on Ultra-low-power Voltage References with Body Biasing Technologies

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In recent years, the research of analog circuit design pays more attention on the design of ultra-low-power VLSI circuits. Voltage scaling is the most effective solution to stringent power requirements and has been practically demonstrated in a number of designs in scaled CMOS technology. Hence, ultra-low-power design translates into ultra-low-voltage design. All kinds of subthreshold integrated circuits have been developed because the weak inversion biasing of MOS transistors allows minimum energy consumption when the voltage is scaled below the device threshold voltage, which is an energy-efficient design. Voltage reference, as an important analog building block, plays a critical function in determining the performance of these subthreshold integrated circuits. Therefore, a reference voltage below the threshold voltage and an nano-power dissipation consumed by the circuit are essential to ensure the operation of these subthreshold designs.

Voltage references can supply a fixed dc voltage of known amplitude that does not change with temperature, supply voltage and process variations. The most important performances of a voltage reference are represented by temperature behavior, power supply rejection ratio, transient response, and power dissipation. Most of voltage reference circuits are fundamentally implemented in bipolar and CMOS technology. Some elementary voltages, e.g., base-emitter voltage, gate-source voltage or threshold voltage, thermal voltage, or their linear combinations are used for realizing a reference voltage with zero temperature coefficient, the disadvantages of these designs are the values of their outputs are above the threshold voltage. Through the low output can be obtain by using the component networks (resistors and capacitors), a trade-off between the power dissipation and chip area cannot be avoided. Several designs make use of the difference in the threshold voltage between two distinct devices, e.g. depletion transistor, or native transistor, or low-threshold-voltage transistor and standard transistor. Such approach requires special technology for fabrication, and the actual value of the reference is difficult to determine accurately because of the process sensitivity of the difference between threshold voltage levels from two distinct transistors. In this research, the focus is on the design and development of novel circuit architectures and design techniques to implement voltage references for application in subthreshold LSI, the low output under threshold voltage can be directly achieved without using any component dividers, and the circuits consume nano-power dissipation.
In the reported ultra-low-power applications, body biasing technologies are all tools that have the potential to lower supply voltage and consequently the total energy consumed by the circuit. The technologies for designing voltage references using MOS body effect are developed to improve the performance of the circuits. Detailed theoretical analysis is presented and measurement results are given to prove the merits of the proposed circuits. The outline of the dissertation is listed as following:

Chapter 1 starts with the introduction of the background, and explains the importance and necessity of the voltage reference for application in subthreshold LSI. The previous arts are presented and the existing problems in these designs are analyzed in detail. And the objectives in this research are clarified.

Chapter 2 gives an overview of several designs using MOS body effect. For voltage references, the fundamental principles are described in detail, and the classic structures are discussed. Based on the self-biased architecture, a simple design has been proposed to improve the typical architecture. According to simulations, the typical T.C. is 14.8 ppm/°C. The line sensitivity is approximately 0.0019 %/V. The power dissipation at 1.4 V supply voltage is 1.4 μW. Thanks to the only two current branches in the proposed circuits, the design areas are small, approximately 0.014 mm².

Chapter 3 concentrates a novel approach for implementing an ultra-low-power voltage reference using the structure of self-cascode MOSFET, operating in the subthreshold region with a self-biased body effect. The difference between the two gate-source voltages in the structure enables the voltage reference circuit to produce a low output voltage below the threshold voltage. The trimming procedures are implemented for this design. The circuit is designed with only MOSFETs and implemented in standard 0.18-μm CMOS technology. Measurements show that the reference voltage is about 107.5 mV, and the temperature coefficient is about 40 ppm/°C, at a range from -20 °C to 80 °C. The voltage line sensitivity is 0.017 %/V. The minimum supply voltage is 0.85 V, and the supply current is approximately 24 nA at 80 °C. The occupied chip area is around 0.028 mm².

Chapter 4 presents a nano-power CMOS voltage reference. A combination of switched-capacitor technology and the body effect in MOSFETs for the
implementation of voltage reference is first developed, the output voltage is defined as the difference between two gate-source voltages using only a single PMOS transistor operated in the subthreshold region, which has low sensitivity to the temperature and supply voltage. A low output, which breaks the threshold restriction, is produced without any subdivision of the components and scaled by adjusting the ratio of capacitors, and flexible trimming capability can be achieved with a composite transistor, such that the chip area is saved. The chip is implemented in 0.18-μm standard CMOS technology. Measurements show that the output voltage is approximately 123.3 mV, the temperature coefficient is 17.6 ppm/°C, and the line sensitivity is 0.15 %/V. When the supply voltage is 1 V, the supply current is less than 90 nA at room temperature. The area occupation is approximately 0.03 mm².

Chapter 5 proposes another novel architecture for implementing switched-capacitor voltage reference. With body biasing technology in MOSFET, the operation uses a single on-chip capacitor and a PMOS transistor to generate a output voltage which has low sensitivity to the temperature. The low output is under the threshold voltage without the use of components dividers, which saves the chip area. The design is simulated in 0.18-μm CMOS technology. The temperature coefficient is approximately 36 ppm/°C. The supply current is approximately 104 nA when the supply voltage is 1 V. The layout occupies 0.013 mm² chip area.

Chapter 6 concludes the proposals in this dissertation, and the future works are presented.