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博 士 論 文 概 要

論 文 題 目

Controlling Value Based Pseudo Power Gating for Power-efficient LSI Design

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Continuous increase in chip density and switching speed of LSI circuits enables over 100 million of integrated gates running at several Giga-hertz in a chip. However, high density and switching speed result in significant power consumption and the demand for low power LSI design has been accelerated significantly. Low power design methodologies have been studied at all design levels for reducing dynamic power and static power. Dynamic power relates to the output changes of logic gates and static power relates to the leak current of them. Dynamic power reduction is important to reduce the runtime power for high performance operations.

The dynamic power dissipation is affected by switching activity of each gate and an avoidance of unnecessary switching activities is effective to reduce the dynamic power. To avoid unnecessary switching activities, a controlling value (CV) of a logic gate takes an important role. Focusing on one gate, if one input takes a CV, then switching of other inputs do not affect to the output of the gate. The CV can stop unnecessary output changes of the focused gate, but there exist unnecessary changes in gate blocks computing other inputs. In other words, switching activities in blocks computing other inputs are unnecessary and give the waste of the dynamic power when one input takes CV. In entire circuit, such power dissipation accounts for a significant amount of overall power consumption. Thus an effective method to reduce redundant switching activities is expected for improving the power efficiency.

In this dissertation, Pseudo Power Gating (Pseudo PG) method based on CV of gates is proposed to save such waste of power for computing unnecessary input values. In Pseudo PG, an input taking the CV of one gate is added as a control signal to gate blocks for other inputs to stop unnecessary changes. The control signal is used to stop the output change of each gate in the block for reducing dynamic power. Distinguished from other power gating methods, the proposed method can reduce dynamic power efficiently by optimizing the switching activities in ultra-fine grained region without extra hardware circuitry. Several heuristic block decision algorithms are proposed for applying Pseudo PG method on combinational circuits. In addition, Pseudo PG is enhanced to dual-stage structure for further reduction of potential power dissipation.

This dissertation consists of 6 Chapters organized as follows:

Chapter 1 [Introduction] briefly summarizes current low power technologies for different levels of LSI design including the gate level circuits. The related works of reducing dynamic and static power are

introduced and their advantages and drawbacks are clarified and several challenges for saving dynamic dissipation are observed. The objective and scope of this research are indicated and the motivations and contributions of this dissertation are described.

Chapter 2 [Preliminaries] shows controlling value based power gating method for reducing static power as a basis of our proposal. Binary Decision Diagram (BDD) is also introduced. BDD is a data structure to represent a Boolean function and logic operations can be done on BDD's. The method to estimate switching activities by using BDD is also presented in this chapter.

Chapter 3 [Pseudo Power Gating Method based on SW-first Algorithm] proposes a CV based Pseudo PG method to optimize the power consumption of combinational circuits by reducing the switching activities. CV of a gate can inactivate other inputs and the switching activities of the blocks computing other inputs can be stopped by the input taking CV as a control signal.

In Pseudo PG, a control signal is associated to the controlled gates. In other words, a cluster of gates can be determined for each control signal. The clustering algorithm to identify the optimum control signal and corresponding power-controlled blocks is essential. A basic size based algorithm and a switching activity first (*SW*-first) algorithm are proposed. In the basic algorithm, the candidate control signals are sorted with the number of controllable gates, and control signals are fixed one by one with the order of gate numbers. On the other hand, the *SW*-first algorithm manipulates the reduction of switching activates by adding a control signal, and maximizes the total reduction. Control signals are sorted by the reduction, and are selected one by one with the order of reductions. The depth might increase after inserting a control signal and the steady maximum depth constraint is applied to prevent performance degradation.

The proposed method has been implemented in C language and applied to ISCAS85 standard benchmark circuits based on the existing BDD manipulation system. Experimental results show that 1.0%~11.6% of reduction of switching activity is obtained by the basic size based algorithm and 1.9%~26.0% reduction is obtained by the SW-first algorithm. The power consumption is evaluated by simulating the netlist which is extracted from the layout using the VDEC (VLSI Design and Education Center in Tokyo University) Rohm 0.18μm process. Evaluations on the ISCAS'85 benchmarks show that the reduction of total power consumption

has been achieved to 3.0%-25.3% (12.8% on average). This work provides a solution for switching activity reduction in very fine-grained region of logic level LSI design with small overhead.

Chapter 4 [Transitive Fanin based Algorithm for Further Power Saving] propose a transitive fanin based algorithm to obtain a control signal with smaller depth under the steady maximum depth constraint. By the constraint, several gates are excluded from a power-controlled block, and considerable potential power reduction is lost. We found that a CV can be propagated from a gate to another gate on a path of serially connected gates. The proposed transitive fanin based algorithm finds control signal candidates with smaller depth based on the propagation of controlling condition via a fanin path, with which more opportunities can be obtained.

As a result, power reduction achieved by the transitive fanin based algorithm ranges from 3.6% to 27.7% (19.1% on average) and exceeds the previous SW-first algorithm by 6.3%. The transitive fanin based algorithm have obvious advantages in detection of control condition favorable for power reduction.

Chapter 5 [Dual-Stage Pseudo Power Gating] newly introduces dual-stage Pseudo PG structure where up to two extra control signals are added to a gate if effective. No matter how effective clustering algorithms are used, there still exist unnecessary computations in power-controlled blocks when their control signals take non-controlling value. The dual-stage structure with two control signals improves power reduction capability. When one signal might take a non-controlling value, another signal can stop the activity by taking a controlling value. Dual-stage structure is realized by adopting another Pseudo PG to the inside of a power-controlled block to stop unnecessary computation while the single-stage control signal takes non-controlling value.

The proposed dual-stage Pseudo PG structure is implemented and 23.23% of power reduction in average has been obtained with 5.3% of propagation delay. Compared with the single-stage Pseudo PG with the transitive fanin based algorithm, 4.18% more power reduction has been achieved.

Chapter 6 [Conclusions and Future Works] concludes this dissertation on the low power design method called pseudo power gating and its clustering algorithms. Future works related to the application of Pseudo PG for large scale power aware design are also shown.