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博士論文概要

論文題目

**Study on Modeling Techniques for
Overshooting Effect of
Multiple-Input Gates in VLSI
Timing Analysis**

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Timing analysis is a useful verification method in modern VLSI designs. It can be used to verify the timing characteristics of complicated digital VLSI systems. Gate delay is an important performance parameter in timing analysis. Many gate delay models are proposed in order to improve the accuracy or speed of verification work in timing analysis. Meanwhile, gate delay models always need to be improved with the development of CMOS process technology.

The overshooting effect, caused by the existence of input-to-output coupling capacitances, is the phenomenon that the output signal of CMOS logics gets out of power supply at the beginning of transition. Traditionally, the gate delay models of CMOS logics are related to transistors' sizes, input signal transition times, and output loads while the overshooting effect is not considered. Since the advent of submicron range, the second-order effects which include input slope and input-to-output coupling effects become domain factors. Then the overshooting effect becomes a concern factor in order to improve the accuracy while modeling the gate delay for CMOS logics. When CMOS process technology enter nanometer regime, the overshooting effect becomes much more obvious and should be considered specially when calculating the gate delay of CMOS logics. Recently, researchers begin to pay more attention to the overshooting effect when modeling the gate delay and they have already proposed the overshooting effect models for an inverter. Although the overshooting effect of multiple-input gates have the same influence on the gate delay as an inverter, the overshooting effect model for multiple-input gates is seldom presented .

In order to model the overshooting effect of multiple-input gates accurately and comprehensively, two models are proposed in this dissertation. Firstly, by simplifying a 2-input gate to an inverter and using the proportional coefficient method, a simple overshooting effect model is proposed which can calculate the overshooting time of 2-input gates accurately and simply. In the second model, an effective method is proposed to model the overshooting effect of multiple-input gates comprehensively. The proposed model is

formula-based and useful not only for 2-input gates but also for other multiple-input gates.

The dissertation is organized with five chapters as follows:

In Chapter 1, “Introduction”, the background and some conceptions of the research are presented. Then the motivation of this dissertation is discussed. At last the organization of this dissertation is described.

In Chapter 2, “Preliminaries”, the phenomenon of the overshooting effect for CMOS gate and its influence are introduced in detail. Firstly, conventional overshooting effect models for CMOS inverter are reviewed. Subsequently, the overshooting effect of CMOS multiple-input gates is analyzed. Then the influence of the overshooting effect for multiple-input gates on the gate delay calculation is considered. After analyzing the overshooting effect models for CMOS inverter and multiple-input gates, why modeling the overshooting effect of multiple-input gates is concluded finally.

In Chapter 3, “Modeling the Overshooting Effect of 2-Input Gates in Nanometer Technologies”, a simple model which can model the overshooting effect of 2-input multiple-input gates accurately is proposed. Firstly, the background and preliminaries of the research are presented. Then a 2-input NOR gate is analyzed under two different input conditions. For the first input condition, the 2-input NOR gate can be simplified to an inverter and the overshooting time can be obtained using the conventional overshooting effect model for an inverter. For the second input condition, the proportional coefficient method is used to calculate the overshooting time based on the first input condition. Moreover, how to extend the proposed overshooting effect model of 2-input NOR gate to 2-input NAND gate conveniently is introduced. Simulation results show that the maximum error of the proposed model is only 3.6% compared with SPICE simulations using 32nm PTM model.

In Chapter 4, “An Effective Model of the Overshooting Effect for Multiple-Input Gates in Nanometer Technologies”, an effective model which can model the overshooting effect of many multiple-input gates is proposed.

Firstly, the background and the research purpose are given. Subsequently, the motivation and the advantages of the proposed model are introduced. Then a formula-based overshooting effect model for 2-input NOR gate is given. Based on the proposed formula-based model, the overshooting effect of 3-input NOR gate is also analyzed and three methods are proposed to calculate the overshooting time of 3-input NOR gate. After proposing the overshooting effect model for 2-input and 3-input gates, the extension methods of the proposed model to other multiple-input gates are presented where 2-input NAND gate, 3-input NAND gate, 4-input NOR gate and AOI12 gate are chosen as the example. Many experimental results show that the error of the overshooting time for multiple-input gates obtained from the proposed model is no more than 3.4% compared with the results obtained from SPICE simulations using 32nm PTM model. At last, the application of the proposed overshooting effect model for multiple-input gates is discussed.

Finally, in Chapter 5, “Conclusions”, contains the conclusion of the dissertation and future work.