Waseda University Doctoral Dissertation

Study on Modeling Techniques for Overshooting Effect of Multiple-Input Gates in VLSI Timing Analysis

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CONTENTS

Chapter1
Introduction

Since the birth of the integrated circuit (IC) by Jack Kilby in 1958, the development of semiconductor technology is always attracting the eyes of the world. Nowadays life is more and more convenient due to the rapid development of very large scale integrated (VLSI) circuit.

With the scaling of process technology, the number of transistors in one chip is increased. Meanwhile, the complexity of VLSI circuit is also increased. In the practical industry, the cost and time are two main metrics for VLSI design and fabrication. Especially, when the process technology enters nanometer era, the value of semiconductor factory has reached to ten billion dollars. Therefore, VLSI verification is becoming one critical step in VLSI process. Designers can use VLSI verification technology to check the accuracy and performance of the circuit which will save the cost and time consumption. In fact, over 50% of the resources invested in developing systems are reportedly spent on verification [1].

VLSI systems include digital design and analog design. Timing analysis is an important verification method in digital VLSI design. It simply refers to the analysis of timing issues in the design. There are two main methods for timing analysis: static timing analysis (STA) and timing simulation. STA is one of the many techniques available to verify the timing of a digital design [2]. An alternate approach used to verify the timing is the timing simulation which can verify the functionality as well as the timing of the design [2].

Digital VLSI system contains a large number of gates and interconnects. Delay is an important performance in timing analysis research. The delay of digital IC includes gate delay and interconnect delay. For digital CMOS integrated circuits, models of gate delay have been proposed in many conventional researches. With the scaling of CMOS process technology, the overshooting effect is become obvious which cannot be neglected [3]. Especially, when digital VLSI enters nanometer era, the overshooting effect is much more obvious and the overshooting time become a dominant component of gate delay [4]. Therefore, the overshooting effect of CMOS gates is analyzed in this dissertation and how to calculate overshooting time of multiple-input gates is also proposed.

The rest of the introduction is composed of three sections. In Sect. 1.1, the

background of the research is introduced. In Sect. 1.2, the motivation of this research is proposed. Finally, Sect. 1.3 the rest of the dissertation is given.

1.1 Background

1.1.1 Timing Analysis in VLSI Design

The evolution of CMOS technology allows designs with millions of gates to be integrated on a single chip. When designers analyze these complicated digital VLSI systems, timing analysis is widely used to estimate the ability of a VLSI circuit to operate at the specified frequency. In Fig. 1.1 [2], a typical CMOS digital design flow is shown. In a CMOS digital design flow, timing analysis can be performed at many different stages of the implementation [2]. For example, during the logic design, designers can use timing analysis to calculate the path delay and confirm whether the longest path delay meets the design criteria. During the physic design, timing analysis can be used to analyze the influence of interconnect and calculate the interconnect delay.

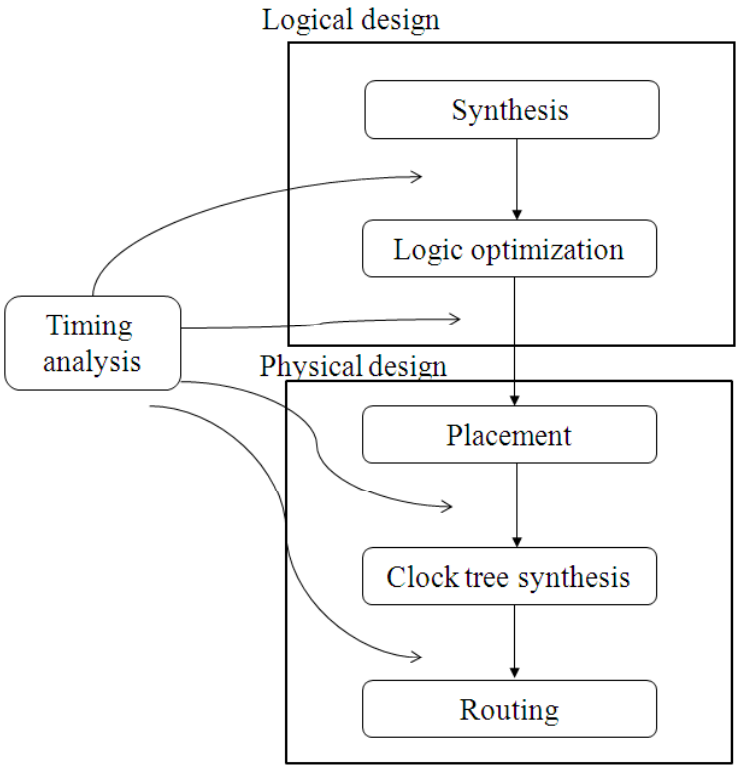

Figure 1.1 CMOS digital design flow.

The crucial work in timing analysis is to calculate the signal propagation delay. The propagation delay is the length of time which starts when the input to a logic gate becomes stable and valid, to the time that the output of that logic gate is stable and valid [2]. Without considering the interconnect affection, the propagation delay can be regarded as the gate delay. The gate delay of an inverter is shown in Fig. 1.2. The gate delay is defined as the time difference when the input and the output voltages are at 50% of supply voltage V_{DD} [28].

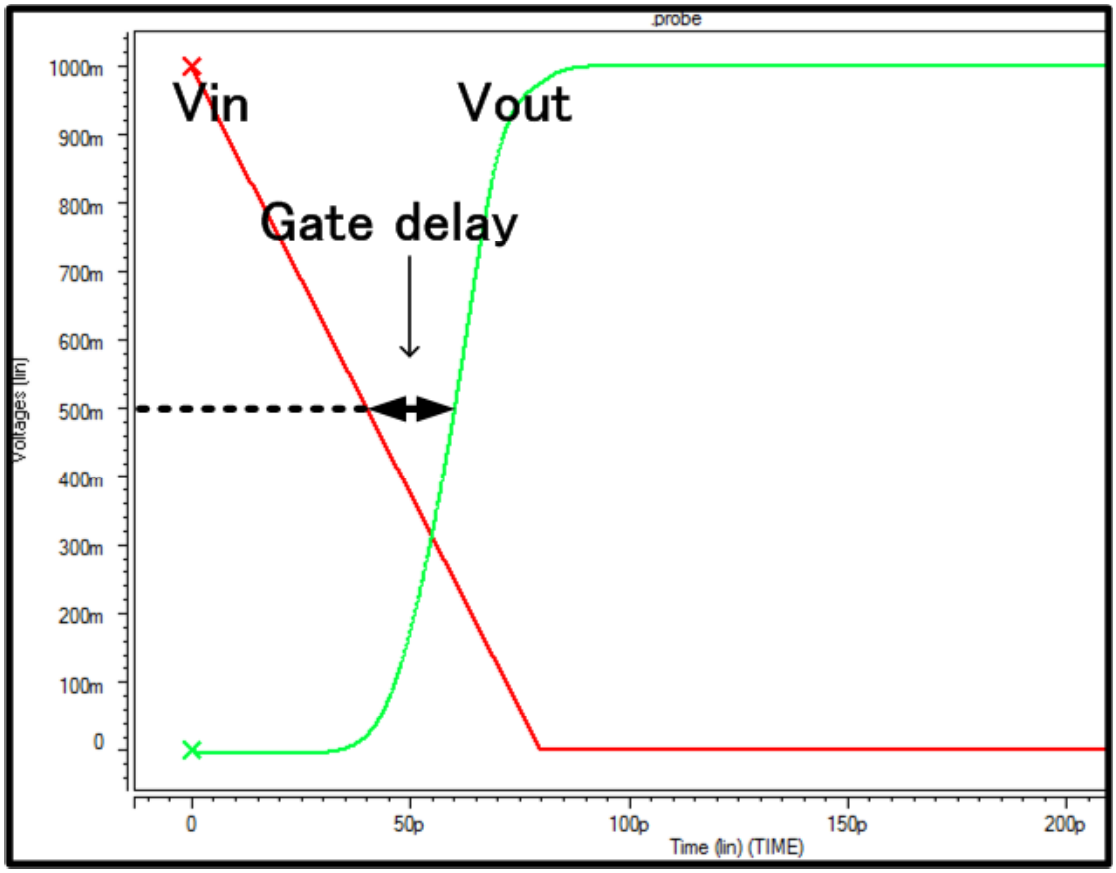

Figure 1.2 Gate delay of an inverter.

The interconnect resistance comes from the interconnect traces in various metal layers and vias in the design implementation [2]. The interconnect capacitance contribution is also from the metal traces and is comprised of grounded capacitance as well as capacitance between neighboring signal routes [2]. If considering the interconnect resistance and capacitance, the propagation delay is composed of gate delay and interconnect delay as shown in Fig. 1.3. In the conventional gate delay models, some models [5]-[10] focus on the modeling of CMOS gate without

considering the interconnect and some models [11]-[16] focus on the analysis of the interconnect influence on the delay.

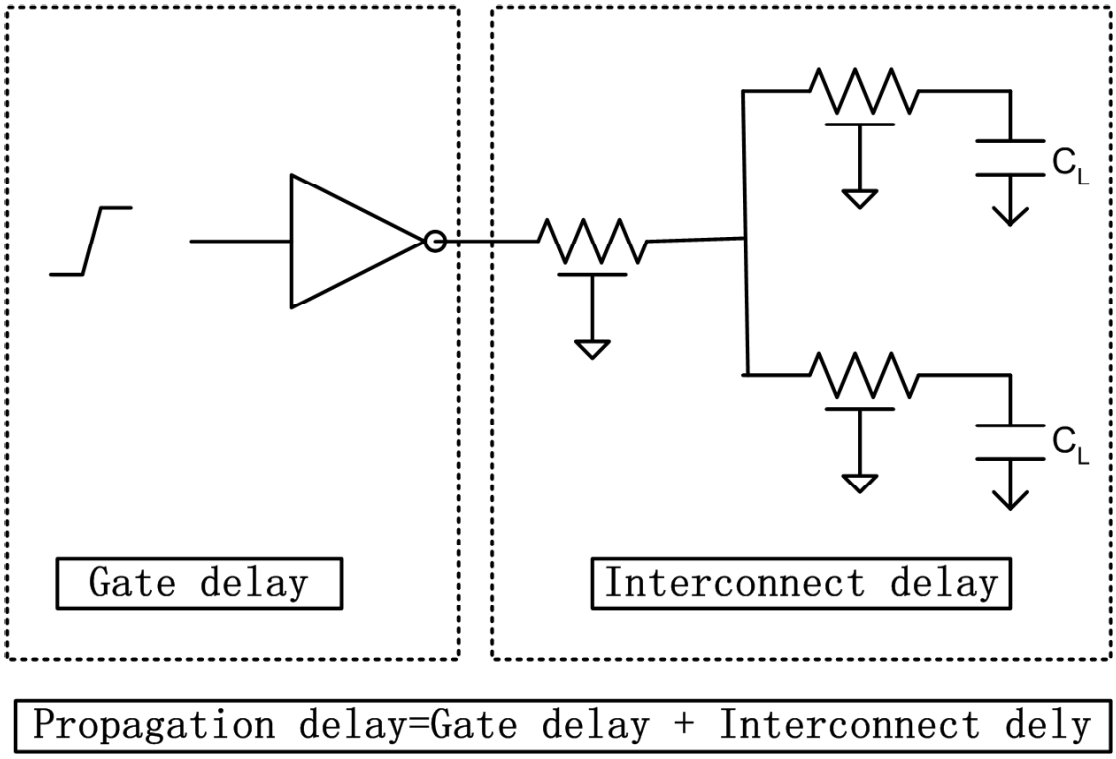

Figure 1.3 Propagation delay of an inverter.

1.1.2 Empirical Gate Delay Model

A simple timing model is linear delay model [2], where the delay of CMOS logics is expressed as a linear function of the two parameters: input signal transition time and load capacitance. The general expression of the delay t_D using the linear delay model is shown below

$$t_D = t_{D0} + t_{D1} * t_{in} + t_{D2} * C_L \ , \qquad (1.1)$$

where t_{D0}, t_{D1}, t_{D2} are constant parameters, t_{in} is the input signal transition time, and C_L is the load capacitance. However, only considering the input signal transition time and load capacitance is not accurate enough to reflect the gate delay for CMOS logics in submicron and nanometer range. Therefore most cell libraries presently use the more complex models such as the non-linear delay model [2].

The lookup table model, which is widely used as empirical gate delay model in industry, is referred to as NLDM (Non-Linear Delay Model) and used for delay,

output slew, or other timing verification [2]. Lookup table model use a two-dimensional table which stores the gate delay data considering the variations of input signal transition times and load capacitances. In Fig. 1.4, the lookup table of an inverter is given. The horizontal axis is the information of different load capacitances and the input signal transition times are listed in the vertical axis. Circuit designers can check the timing information of CMOS logics easily according to the lookup table date proposed by manufacturers in advance.

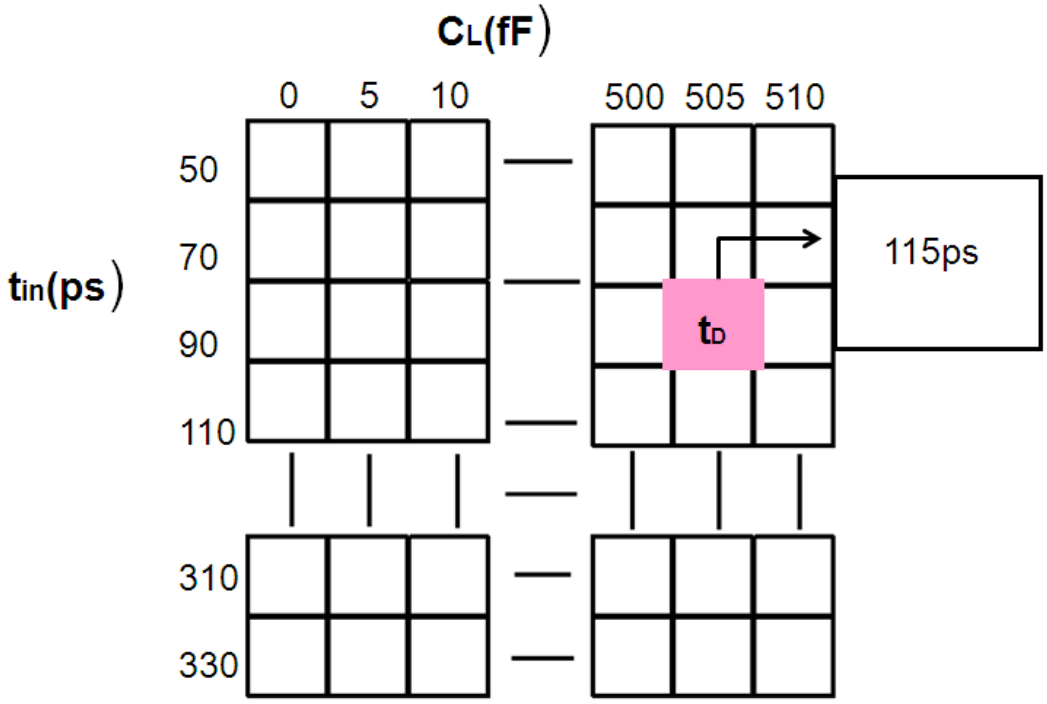

Figure 1.4 Lookup table for gate delay calculation.

With the scaling of CMOS process technology, the effect of interconnect resistance becomes larger which cannot be neglected in delay calculation. In order to model the CMOS gate with RC interconnect load, a one-segment RC-π model is proposed by O' Brien and Savarino in [17] as shown in Fig. 1.5.

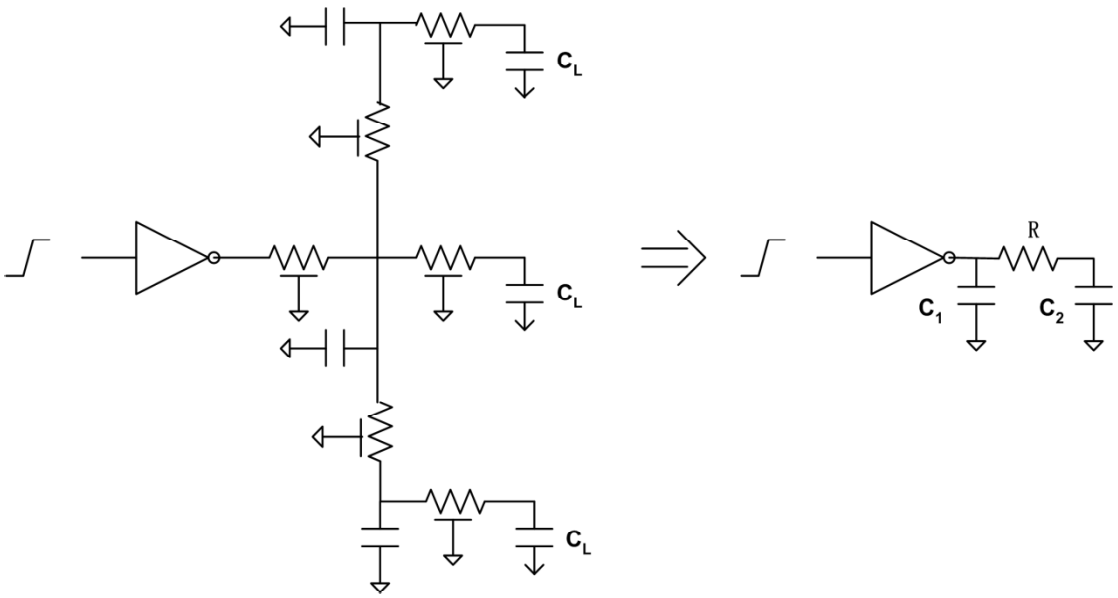

Figure 1.5 RC-π model for gate delay calculation.

After using RC-π model, the gate with complicated RC tree can be simplified to the gate driving only three factors. Although the simplified gate driving RC tree is simple, it can reflect the influence of interconnect factors. The delay of CMOS gate using RC-π model is related with four parameters which is shown as

$$t_D = f(t_{in}, C_1, R, C_2) \quad . \tag{1.2}$$

Lookup table model is widely used in practical industry, while RC-π model with four parameters shown in Eq. (1.2) make it difficult to use the lookup table model. Therefore, the effective capacitance models [18]-[23] are presented to calculate the gate delay when RC-π model is used. As shown in Fig. 1.6, an effective capacitance is used to replace the RC loads of RC-π model. The appearance of effective capacitance model can make the lookup table model widely used in practical industry.

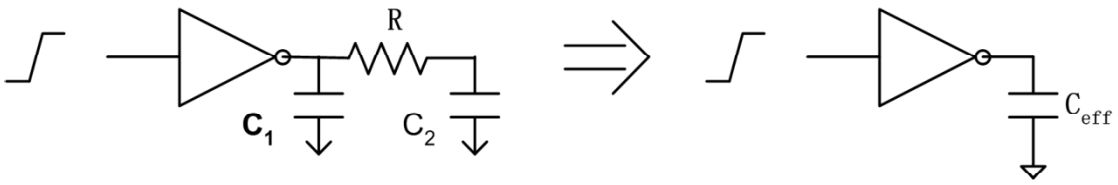

Figure 1.6 Effective capacitance used in RC-π model.

1.1.3 Formula-Based Gate Delay Model

Although empirical gate delay model is very convenient in practical industry, the lookup table needs to be improved according to the improvement of CMOS process technology. Moreover, what parameters of transistors will affect the gate delay and how can those parameters affect the gate delay are also not understood easily if only using the empirical gate delay model.

Therefore, formula-based gate delay models are proposed in [24]-[38]. These models predict the gate delay through analyzing the electrical characteristics of transistors. They construct many equations according to analyzing the operations of transistors. After using reasonable approximation method, these equations can be solved and the gate delay can be expressed in the form of expressions which include electrical parameters, input conditions and output conditions. Obviously, the advantage of formula-based gate delay model is that we can find which parameters affect the gate delay and how those parameters affect the gate delay.

1.1.4 Overshooting Effect of CMOS Gate

The overshooting effect, caused by the existence of input-to-output coupling capacitances, is the phenomenon that the output signal of CMOS logics gets out of power supply at the beginning of transition [3]. A CMOS inverter considering the input-to-output coupling capacitances is shown in Fig. 1.7.

In Fig. 1.7, V_{in} and V_{out} are the input and output voltage. C_L is the load capacitance. C_M is the input-to-output coupling capacitance. When a falling signal is connected to the input of the inverter in Fig. 1.7, the output voltage will be below 0 at the beginning of transition due to the existence of input-to-output coupling capacitance as shown in Fig. 1.8.

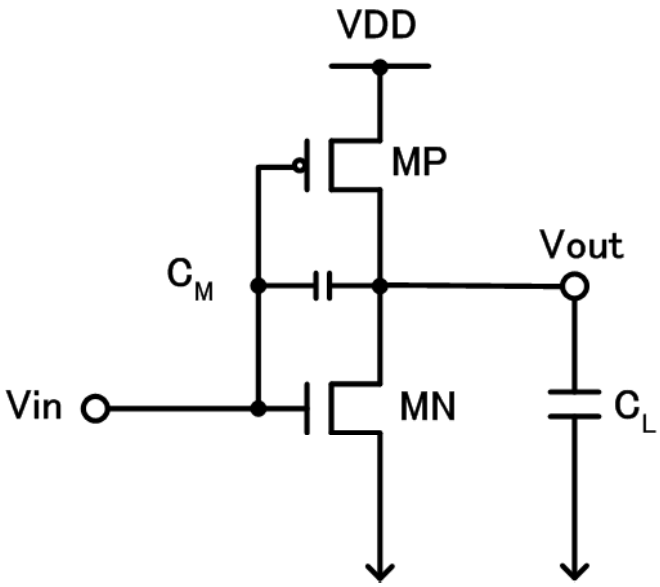

Figure 1.7 CMOS inverter considering the input-to-output coupling capacitance.

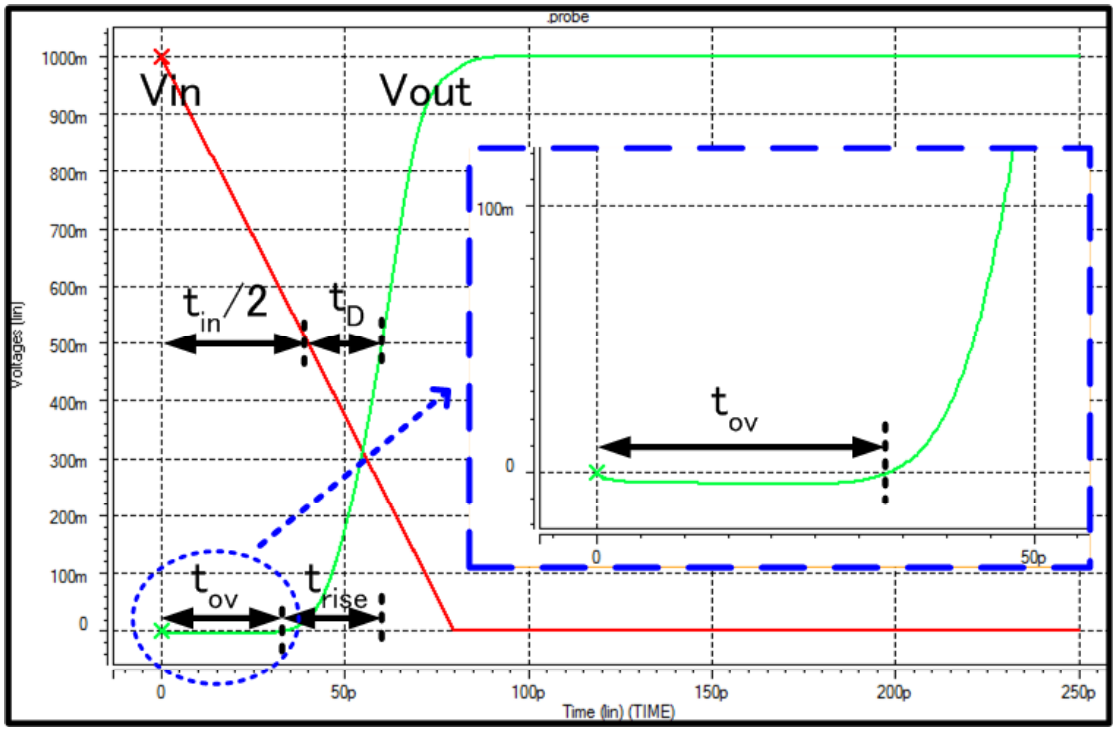

Figure 1.8 Output voltage of the inverter.

In Fig. 1.8, the gate delay is expressed as

$$t_D = t_{ov} + t_{rise} - \frac{t_{in}}{2} \tag{1.3}$$

where t_{ov} is the overshooting time, t_{rise} is the output voltage rise time which is defined from $t = t_{ov}$ to the time when the output voltage reach 50% of the supply

voltage, t_{in} is the input signal transition time. It can be obtained from Eq. (1.3) that the overshooting time t_{ov} is a component of gate delay t_D.

When the long channel transistors are used conventionally for CMOS gate, the overshooting effect is not significant for digital circuits and is only important for analog circuits [40]. Transitional gate delay models [24]-[27] consider the input transition time, output load capacitance and transistor size while the influence of the overshooting effect is not taken into account. In submicron range, the overshooting effect becomes significant and thus begins to be considered in CMOS gate analysis [28]-[33][41][42]. With the scaling of CMOS process technology to nanometer range, the overshooting effect is paid much attention in gate delay models. Moreover, accurate overshooting effect models for CMOS inverter are specially presented in [2][3]. However, accurate model of the overshooting effect for multiple-input gate is seldom presented although the overshooting time of multiple-input gate still has significant influence on the gate delay.

1.2 Motivation of this Dissertation

Timing analysis is a useful verification method which is widely used in digital VLSI designs. Gate delay is an important focus in timing analysis research. Accurate gate delay model is convenient for designers to estimate the delay. Some formula-based models are also helpful for researchers understand how the parameters of transistors and load conditions affect the gate delay. Moreover, the nature of simulation methods for timing analysis is using mathematic equations to predicting some action or performance of digital circuit. Therefore, an effective and accurate gate delay model is strongly needed which can be incorporated in simulation tools.

Gate delay models need to be improved frequently due to the improvement of CMOS process technology. Traditionally, the gate delay models of CMOS logics [24]-[26] are related to transistors' sizes, input signal transition times, and output loads while the overshooting effect is not considered. Since the advent of submicron range, the second-order effects which include input slope and input-to-output coupling effects become dominant factors. Then the overshooting effect becomes a concern factor in order to improve the accuracy while modeling the gate delay or power consumption for CMOS logics [31][32][41][42]. Along with the further research, simple expressions describing overshooting times of an inverter are given in the gate delay model and power consumption model in [33] and [39], respectively.

With the obviousness of the overshooting effect for CMOS gates in the nanometer regime, more and more attention has been paid to the research about modeling the overshooting effect for CMOS gates. Recently, accurate overshooting effect models for CMOS inverter are specially presented in [2][3]. For multiple-input gates, the overshooting effect is also obvious and has the same influence to gate delay and power consumption as an inverter. However, less work has been done to develop an accurate overshooting effect model for multiple-input gates.

Therefore, the overshooting effect of multiple-input gates is considered as the theme of this dissertation. Two overshooting effect models for multiple-input gates are

proposed. Firstly, a simple model using proportional coefficient is presented and it can model the overshooting effect of two-input gate accurately. Secondly, in order to expand the scope of the overshooting effect model, an effective model of the overshooting effect for multiple-input gates is proposed. The second model is formula-based and can be applied to many kinds of multiple-input gate accurately.

1.3 Dissertation Organization

The dissertation is organized with five chapters as follows:

In Chapter 1, “Introduction”, the background of the research in this dissertation is presented. Timing analysis is widely used in VLSI verifications. Firstly, the importance of timing analysis is introduced and the gate delay in timing analysis is also introduced. Secondly, empirical gate delay models are analyzed where the look-up table model and RC-π is reviewed. Subsequently, the advantage of the formula-based gate delay models is clarified. Because the overshooting effect is the main research objective of this dissertation, it is briefly introduced in Chapter 1. Moreover, motivation of this dissertation is given. At last the organization of this dissertation is described in this chapter.

In Chapter 2, “Preliminaries”, the phenomenon of the overshooting effect for CMOS gate and its influence is introduced in detail. Firstly, conventional overshooting effect model for CMOS inverter is reviewed in Sect. 2.1. Subsequently, the overshooting effect of CMOS multiple-input gates is analyzed in Sect. 2.2. Then the influence of the overshooting effect for multiple-input gates is considered in Sect. 2.3. After analyzing the overshooting effect models for CMOS inverter and multiple-input gates, why modeling the overshooting effect of multiple-input gates is concluded in Sect. 2.4.

In Chapter 3, “Modeling the Overshooting Effect of 2-Input Gates in Nanometer Technologies”, a model which can model the overshooting effect of 2-input multiple-input gates is proposed. In Sect. 3.1, the background and purpose of Chapter 3 are given. Then the overshooting effect of 2-input NOR gate is analyzed briefly in Sect. 3.2. After that, the proposed model of the overshooting effect for 2-input gates is introduced in detail. There are two different input conditions for 2-input NOR gate, the overshooting time expressions and the proportional coefficient method are given in Sect. 3.3. How to extend the proposed model in Sect. 3.3 to 2-input NAND gate condition is presented in Sect. 3.4. In order to verify the accuracy of the proposed

model, simulation results are shown in Sect. 3.5 under many conditions. Finally, Chapter 3 is concluded in Sect. 3.6.

In Chapter 4, “An Effective Model of the Overshooting Effect for Multiple-Input Gates in Nanometer Technologies”, the model which can model the overshooting effect of many multiple-input gates is proposed. Firstly, the background and the research purpose are given in Sect. 4.1. Subsequently, the motivation and advantage of proposing the model are analyzed in detail in Sect. 4.2. Section 4.3 is the main part of Chapter 4 where the proposed model is introduced comprehensively. In Sect. 4.3.1, the formula-based overshooting effect model for 2-input gate is given. How to model the overshooting effect of 3-input gate is presented in Sect. 4.3.2 where three different input conditions are all considered. After giving the overshooting effect model for 2-input and 3-input gates, the extension method of the proposed model to other multiple-input gates is presented in Sect. 4.3.3. After giving the model of the overshooting effect for multiple-input gates, experimental results are shown in Sect. 4.4 which reflect that the proposed model can predict the overshooting time of multiple-input gates accurately. Section 4.5 clarify the application of the proposed model, in which, the proposed model is used to improve the accuracy of gate delay calculation and predicting the output waveform of Thevenin equivalent model. Chapter 4 is concluded in Sect. 4.5.

Finally, “Conclusions”, contains the conclusions of the dissertation and future work, is presented in Sect. 5.

Chapter2
Preliminaries

With the development of CMOS process technology, gate delay models of timing analysis need to be improvement frequently. In micron range, the overshooting effect of CMOS gates is not considered. When entering the submicron range, the overshooting effect begins to be considered. Recently, the CMOS process technology has been in the nanometer era, the overshooting effect becomes much more obvious and cannot be neglected again. Moreover, the overshooting time of CMOS gate will have a significant influence on gate delay calculation.

The phenomenon and the induction of the overshooting effect for an inverter are firstly introduced. Subsequently, how can the overshooting time of an inverter affect the gate delay is also analyzed. Due to the importance of the overshooting effect for an inverter in nanometer technologies, researchers have already proposed accurate overshooting effect models for an inverter. The conventional overshooting effect model for an inverter is reviewed comprehensively because it is useful for further research.

Although the overshooting effect model for an inverter has been proposed, the overshooting effect model for multiple-input gates is seldom considered. Therefore, some multiple-input gates are chosen as the objective to verify whether the overshooting effect of multiple-input gats is still obvious. The answer is yes and the phenomenon of the overshooting effect for multiple-input gates is clearly shown. The influence of the overshooting effect for multiple-input gates is considered in this section. It can be found that the overshooting time of multiple-input gates still occupy a large amount of gate delay. Without including the influence of the overshooting effect, the gate delay calculation for multiple-input gates will induce errors.

Therefore, based on specific clarification, the reason why the dissertation focuses on the modeling of the overshooting effect for multiple-input gates are presented at the end of this section.

2.1 Overview of Conventional Overshooting Effect Model for CMOS Inverter

As introduced in Chapter 1, the overshooting effect of CMOS gates is important when the process technology enters nanometer regime. Therefore, some researchers begin to model the overshooting effect for CMOS inverter specially. In this section, a conventional overshooting effect model of CMOS inverter in [3] is reviewed.

2.1.1 Introduction of the Overshooting Effect for CMOS Inverter

In micron range, the common value of the gate delay for CMOS gates is more than 10ns. In submicron range, the gate delay for CMOS gates decreases to no more than 10ns. However, the overshooting time in micron and submicron range is very small. For the gate delay, the overshooting time is a very little component. As shown in Fig. 2.1, when a falling signal is connected to the input of an inverter using 0.18um CMOS process, the overshooting time is 346ps and the gate delay is about 3.27ns. It can be clearly found that, compared with the gate delay, the overshooting time is so small that can be almost neglected. Therefore, the overshooting effect is also not paid much attention in micron and submicron range.

When the process enters nanometer regime, the high requirement for the speed means the decrease of input signal transition time. Thus, the gate delay for CMOS gates also decreases to picoseconds. Meanwhile, the order of the overshooting time is picoseconds. The overshooting time begins to be an important component for the gate delay. Therefore, the overshooting effect becomes significant and cannot be ignored anymore.

A CMOS inverter with the load capacitance C_L is shown in Fig. 2.2, where the input-to-output coupling capacitance C_M is considered.

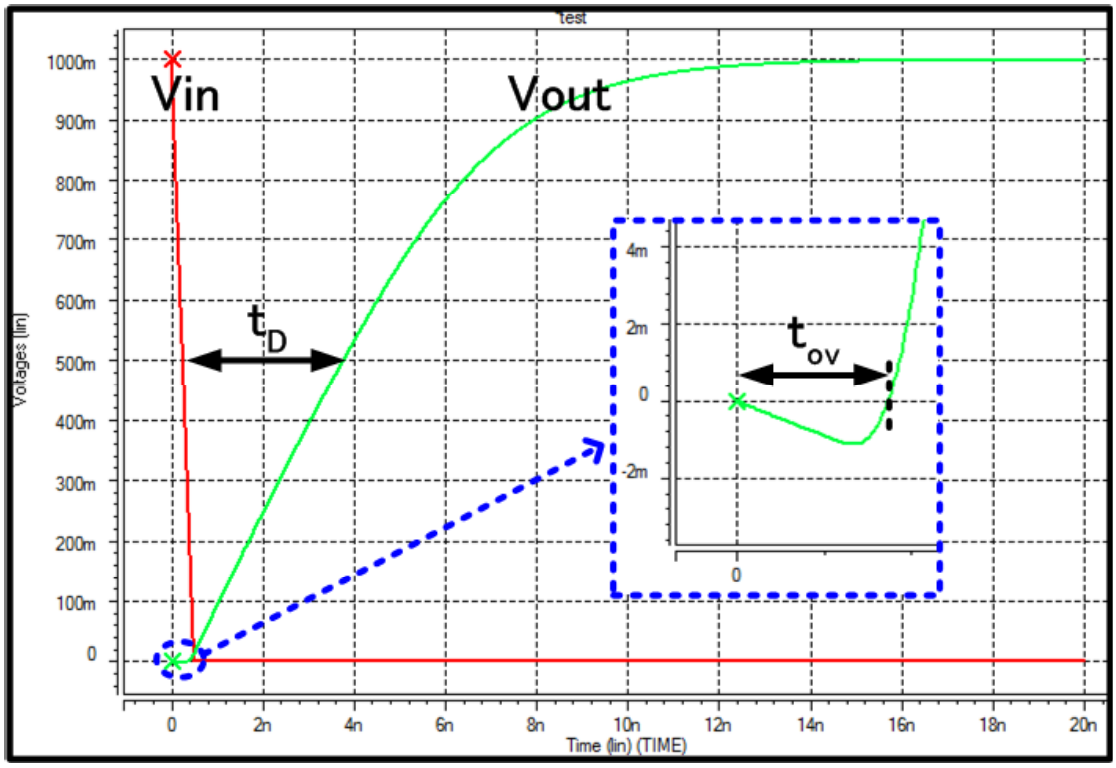

Figure 2.1 Output voltage of an inverter using 0.18um CMOS process.

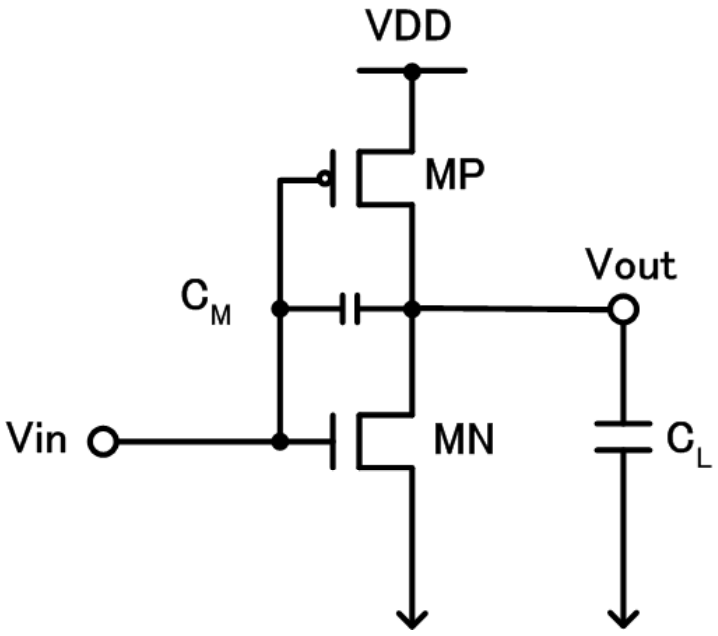

Figure 2.2 CMOS inverter considering the input-to-output coupling capacitance.

Figure 2.3 shows the output voltage V_{out} of the CMOS inverter when a falling input signal applied using CMOS 32nm PTM model [43]. The gate delay t_D is defined as the time interval from $V_{in} = V_{DD}/2$ to $V_{out} = V_{DD}/2$. According to the

output voltage shown in Fig. 2.3, the gate delay t_D can be expressed as

$$t_D = t_{ov} + t_{rise} - \frac{t_{in}}{2} \tag{2.1}$$

where t_{ov} is the overshooting time, t_{rise} is the output voltage rise time which is defined from the time $t = t_{ov}$ to the time when the output voltage reach half of V_{DD}, t_{in} is the input signal transition time.

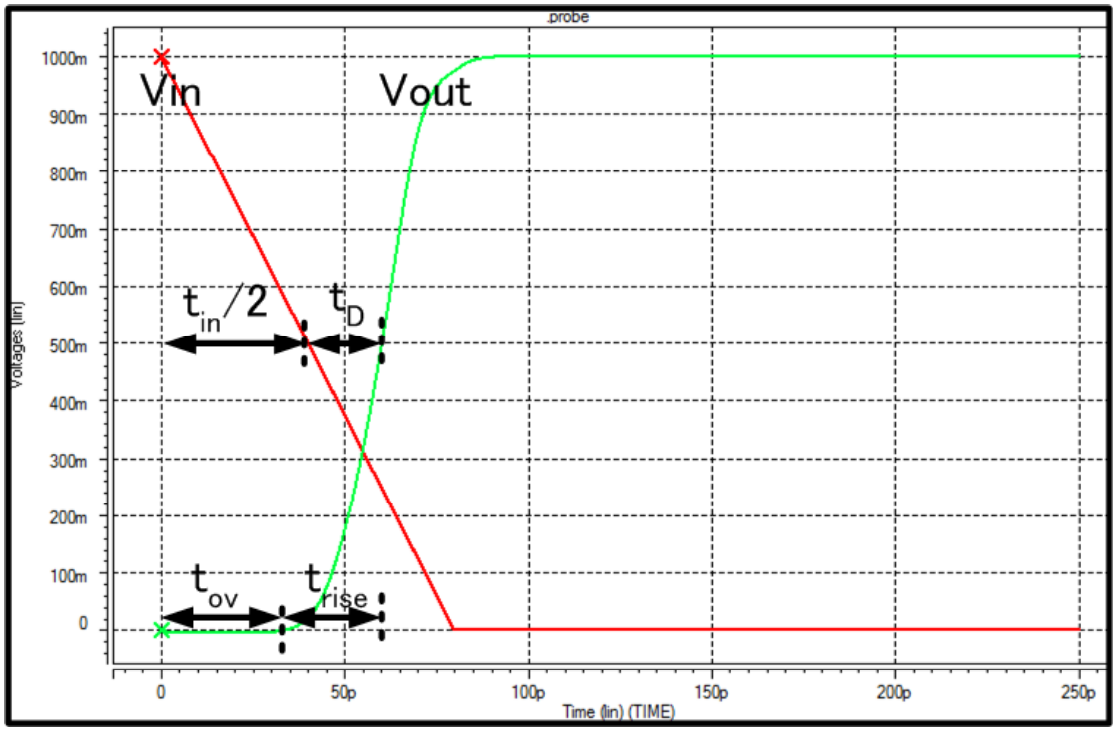

Figure 2.3 Output voltage of CMOS inverter when a falling input signal applied.

From the equation shown in Eq. (2.1), it can be found that the overshooting time t_{ov} is a component of the gate delay t_D. Figure 2.4 shows the overshooting time t_{ov}, the gate delay t_D and the ratio of t_{ov}/t_D for an inverter versus different transistor sizes. The length of the inverter is $L_n = L_p = 40\text{nm}$, the width of the inverter is $W_p = 2W_n$, the input signal transition time is $t_{in} = 60\text{ps}$ and the load capacitance is $C_L = 1\text{fF}$. The width of NMOS W_n increases from 80nm to 640nm.

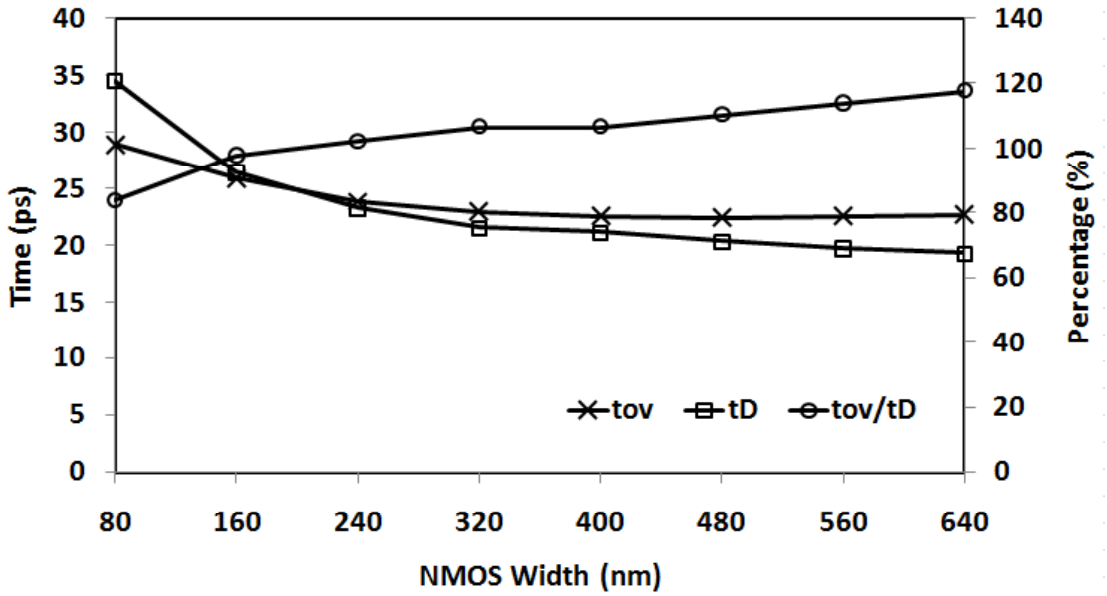

Figure 2.4 The overshooting time t_{ov}, the gate delay t_D and the ratio of t_{ov}/t_D for a CMOS inverter versus different transistor sizes.

It is reflected from Fig. 2.4 that the overshooting time and the gate delay decrease with the increase of NMOS width. However, the ratio of t_{ov}/t_D increases from 84% to 118% when NMOS width increase from 80nm to 640nm.

Simulation result shown in Fig. 2.4 reflect that the overshooting time account a large amount of gate delay. It can be also concluded that the overshooting time t_{ov} is one of the most dominant parts of the gate delay t_D. Therefore, the overshooting time should be calculated accurately when calculating the gate delay of CMOS inverter. Meanwhile, modeling the overshooting effect of CMOS inverter in nanometer regime is inevitable.

2.1.2 Conventional Overshooting Effect Models for CMOS Inverter

Transitionally, the gate delay models for CMOS logics are included with input signal transition times, transistor sizes and input signal transition times [4]. However, the overshooting effect is not considered in traditional gate delay models [24]-[27].

With the scaling of process technology, the overshooting time is begun to be considered.

In [59], the overshooting time is regarded as a constant shift time while how to get the value of that time is not given.

In [31]-[32], the input-to-output coupling capacitance is researched and the expression for the overshooting time is simply presented.

In [24] and [28], a simple model is used to calculate the overshooting time for an inverter. When a falling signal is applied to the input terminal of an inverter shown in Fig. 2.2, the PMOS transistor is opened at the time when $t = t_P$, the time t_P is assumed as the overshooting time for the inverter. Similarly, when a rising signal is connected to the input terminal of the inverter in Fig. 2.2, the NMOS transistor is opened at the time when $t = t_N$, then the time t_N is assumed as the overshooting time for the inverter.

However, the methods in [24][28][31][32][59] cannot be applied to the model of overshooting effect for an inverter accurately in nanometer regime.

When the process enters nanometer regime, researchers begin to model the overshooting effect for an inverter specially.

In [4], an analytical method to calculate the overshooting time of an inverter is proposed. By using the linear approximation of PMOS drain current, the overshooting time for an inverter is finally expressed with the input signal transition time and a normalized time value. The main work in [4] is to obtain the normalized time value using an analytical method.

In nanometer regime, Huang's group have spent much effort on the research of modeling the overshooting effect for an inverter [3][45]-[47]. The proposed models in this dissertation are also partly based on the conventional research by Huang's group in [3]. Therefore, the derivation method of the equations for t_{ov} in [3] is reviewed in order to make the description later understood easily.

In [3], the differential equation for the inverter in Fig. 2.2 is firstly established which is shown as

$$C_L \frac{dV_{out}}{dt} = I_p - I_n + C_M \frac{d(V_{in} - V_{out})}{dt} \tag{2.2}$$

where C_L is the load capacitance, C_M is the input-to-output coupling capacitance, V_{out} and V_{in} are the output and input signals, respectively. I_p and I_n are the drain

currents of PMOS and NMOS, respectively. In [3], the input terminal is connected to a falling signal while similar expressions can be obtained if a rising signal is used. The falling signal is expressed as

$$V_{in} = \begin{cases} V_{DD}: t \le 0 \\ \left(1 - \frac{t}{t_{in}}\right) V_{DD}: 0 < t \le t_{in} \\ 0: t > t_{in} \end{cases}, \quad (2.3)$$

where t_{in} is the input signal transition time.

By using the linear approximation of the load capacitance current, the overshooting time is expressed as

$$t_{ov} = \frac{2Q_1}{I_{CL}(t_{ov})} + t_{vmin}, \quad (2.4)$$

where Q_1 is the charge flowing out of the load capacitance C_L, $I_{C_L}(t_{ov})$ is the current of the load capacitance when $t = t_{ov}$, t_{vmin} is the time when the output voltage is at its minimum value.

In [3], the authors try to find the expressions for Q_1, $I_{C_L}(t_{ov})$ and t_{vmin} using many reasonable approximate methods. Finally, by solving the equation (2.4), the overshooting time expression is shown as

$$t_{ov} = t_{vmin} - t_\gamma + \sqrt{\frac{2Q_1}{I_{D0}}(t_{in} - t_{TPL}) + t_\gamma^2}, \quad (2.5)$$

where

$$t_\gamma = \frac{1}{2}\left(t_{vmin} - t_{TPL} - C_M \frac{V_{DD} t_{in}}{t_{in}} \frac{t_{in} - t_{TPL}}{I_{D0}}\right). \quad (2.6)$$

In Eqs. (2.5) and (2.6), t_γ is an intermediate parameter, I_{D0} is the drain current of the PMOS when $V_{GS} = V_{DS} = V_{DD}$, t_{TPL} is the time point which is expressed as $t_{TPL} = \frac{|V_{TPL}|}{V_{DD}} t_{in}$ while V_{TPL} is the equivalent threshold voltage.

2.2 Overshooting Effect of CMOS Multiple-Input Gates

With the scaling of CMOS process technology to nanometer scale, the overshooting effect of CMOS inverter is analyzed and modeled in [3][4][45]-[47]. However, the overshooting effect of multiple-input gates is still obvious and the overshooting time of multiple-input gates also has a significant influence on gate delay.

Fig. 2.5 shows a CMOS 2-input NOR gate. The capacitances C_{gd1}, C_{gd2}, C_{gd3}, C_{gd4} and C_{gs4} are all input-to-output coupling capacitances.

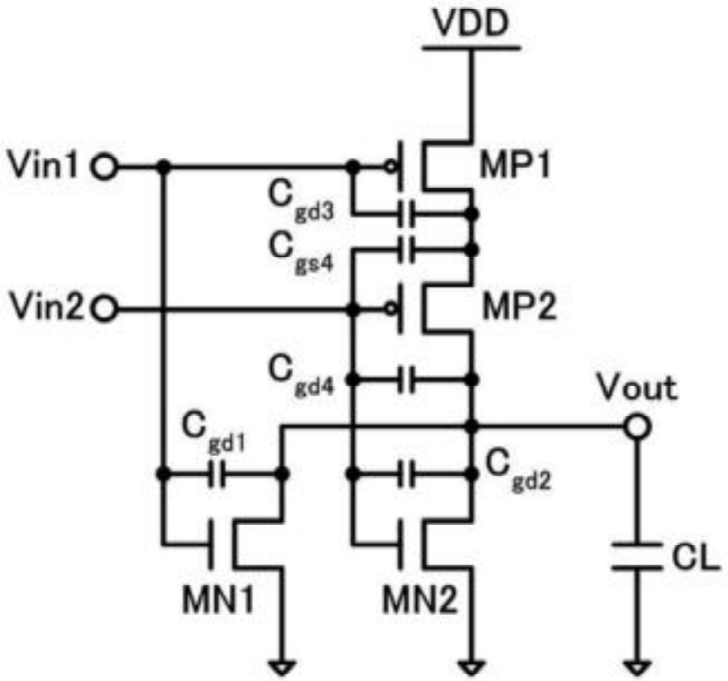

Figure 2.5 2-input NOR gate considering the coupling capacitances.

When a falling signal is connected to the input V_{in2} of 2-input NOR gate in Fig. 2.5, the output waveform of the gate in Fig. 2.5 using 32nm PTM model [43] is shown in Fig. 2.6.

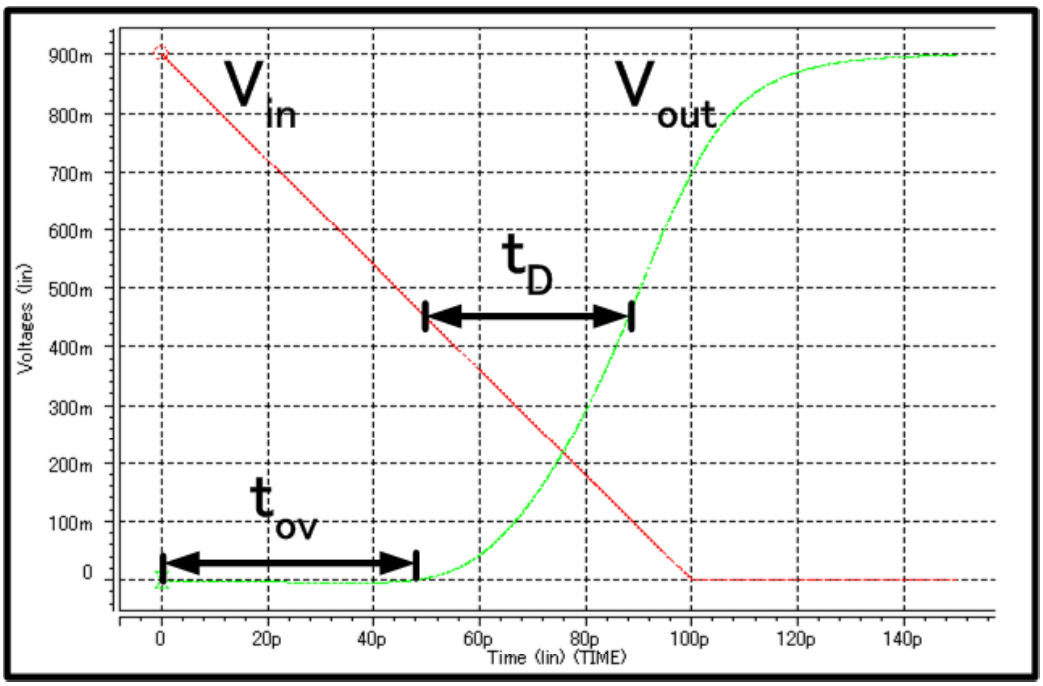

Figure 2.6 Output waveform of 2-input NOR gate when V_{in2} switched.

From the output waveform shown in Fig. 2.6, it can be found that the overshooting effect is very obvious and the overshooting time occupies a large amount of the gate delay.

If the input number of multiple-input gate is increased, the overshooting effect is still obvious. For example, a 3-input NOR gate is shown in Fig. 2.7.

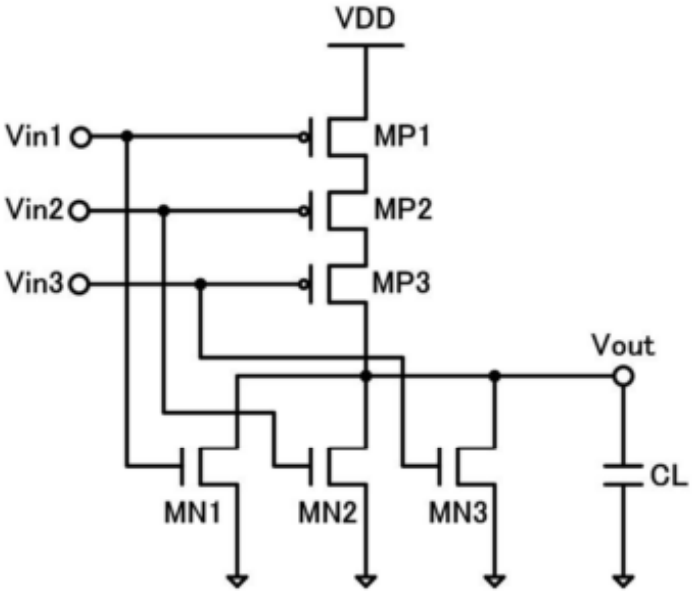

Figure 2.7 CMOS 3-input NOR gate.

If a falling signal is connected to V_{in2}, the output waveform is shown in Fig. 2.8.

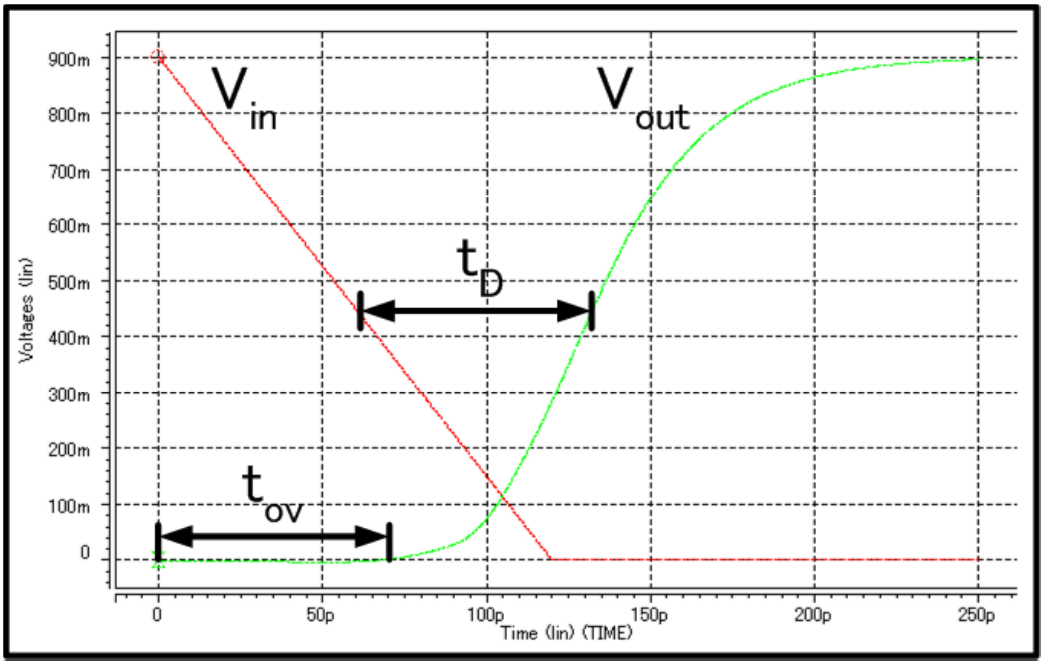

Figure 2.8 Output waveform of 3-input NOR gate when V_{in2} switched.

It can be found that the overshooting effect of 3-input NOR gate is still obvious which is similar to the condition of 2-input NOR gate.

The overshooting effect of 2-input and 3-input NOR gate is shown in Figs. 2.6 and 2.8, respectively. For the complex multiple-input gates in nanometer technology, the overshooting effect is also as obvious as the simple multiple-input gates. An AOI12 gate is shown in Fig. 2.9. When V_{in2} is connected to a falling signal, Vin1 and Vin3 are connected to the ground, the output waveform is shown in Fig. 2.10. The overshooting effect for AOI12 gate is similar as NOR gate and is also obvious.

Therefore, when the CMOS process technology enters nanometer regime, the overshooting effect of multiple-input gates is obvious. The overshooting time of multiple-input gates also occupy a large amount of gate delay which is similar as the inverter. Therefore, the overshooting effect of multiple-input gates should also be considered and paid much more attention.

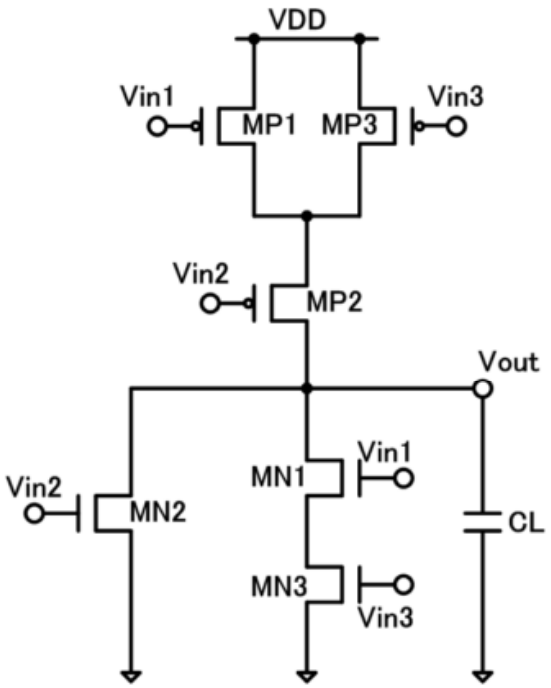

Figure 2.9 CMOS AOI12 gate.

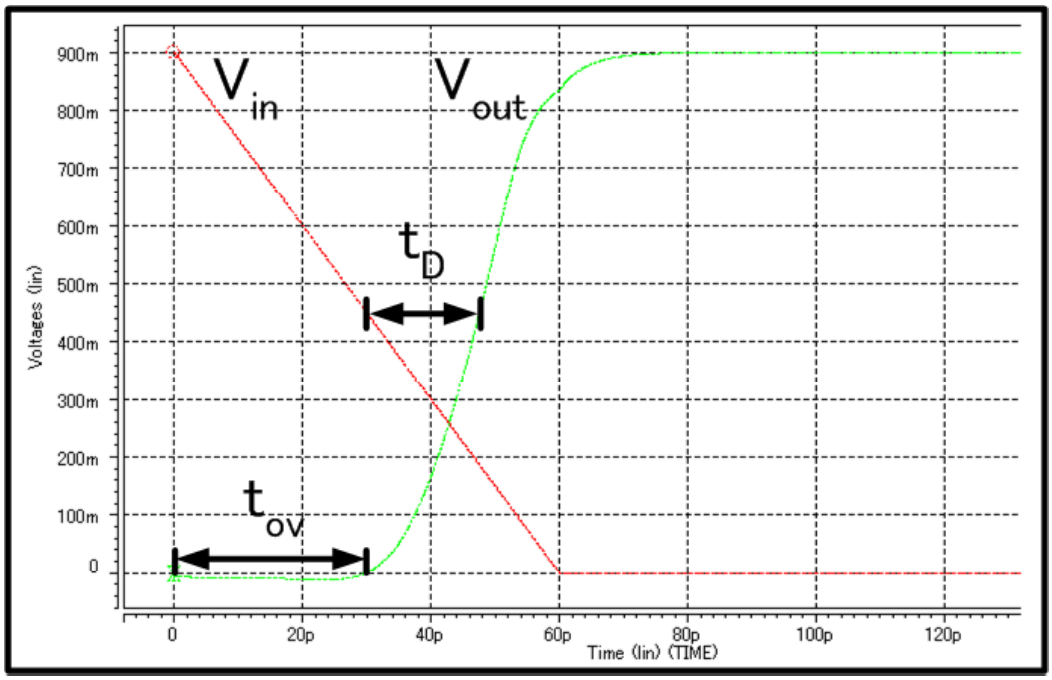

Figure 2.10 Output waveform of AOI12 gate when V_{in2} switched.

2.3 Considering the Influence of the Overshooting Effect for Multiple-Input Gates

In Sect. 2.2, the overshooting effect of multiple-input gate is simply shown and some multiple-input gates are chosen as the research object. How the overshooting effect or the overshooting time of multiple-input gates will affect the gate delay calculation will be discussed in this section.

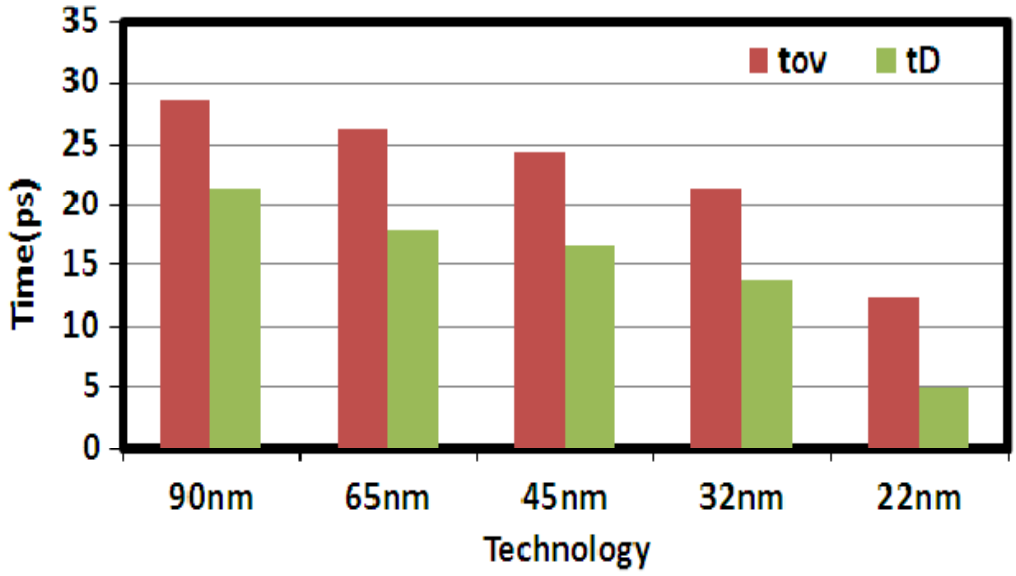

Figure 2.11 Overshooting time t_{ov} and gate delay t_D of CMOS 2-input NOR gate with various process technologies.

Figure 2.11 shows the overshooting time t_{ov} and the gate delay time t_D of the 2-input NOR gate in Fig. 2.5 for various nanometer process technologies from 90-nm technology to 22-nm technology. The input condition is that V_{in2} is connected to a falling signal and V_{in1} is connected to the ground. The transistor length L_n and L_p are the minimum feature size. The PMOS width is $W_p = 10L_p$ and the NMOS width is $W_n = 2W_p$. The load capacitance is $C_L = 0.01\text{pF}$. The input transition time t_{in} of V_{in2} is 60ps. In Fig. 2.11, both the overshooting time t_{ov} and the gate delay time t_D decrease with the scaling of process technology. On the contrary, the ratio value

t_{ov}/t_D increases from 134.7% in 90nm to 249.0% in 22nm. Additionally, although t_{ov}/t_D will become small with the decrease of t_{in}, the overshooting time t_{ov} still occupies a large proportion of delay time t_D.

Figure 2.12 shows the ratio of t_{ov}/t_{50} and t_{ov}/t_D for 3-input NOR gate in Fig. 2.7 when V_{in2} is switched using CMOS 32nm PTM model [43]. The contribution of t_{ov} to t_{50} is about 25%~40%. The overshooting time t_{ov} gives a greater contribution to the gate delay $t_D$which is about 30%~65%.

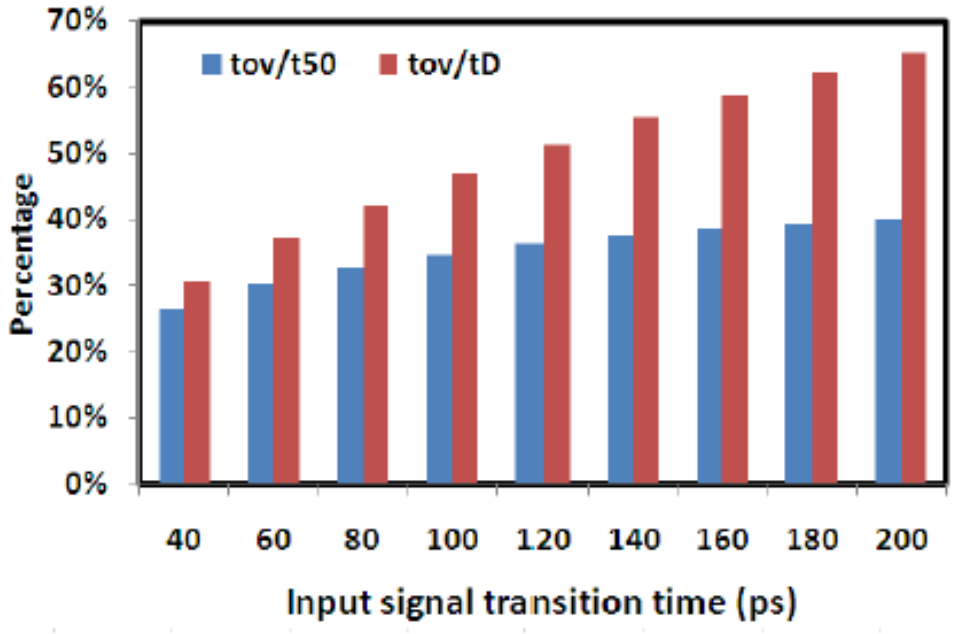

Figure 2.12 The ratio of t_{ov}/t_{50} and t_{ov}/t_D for 3-input NOR gate.

From the histograms shown in Figs. 2.11 and 2.12, it can be concluded that the overshooting time t_{ov} has a significant influence on gate delay t_D for multiple-input gates in nanometer technologies. Therefore, the overshooting effect model for multiple-input gates should be researched carefully. Meanwhile an accurate overshooting effect model for multiple-input gates can improve the accuracy of gate delay model.

2.4 Purpose of Modeling the Overshooting Effect for Multiple-Input Gates

Timing analysis is commonly applied during the verification of digital VLSI designs. Gate delay is an important verification performance when doing timing analysis. Many gate delay models are proposed to predict the delay of digital circuits well. The gate delay model is often improved because the scaling of CMOS process technology.

In micron range for CMOS process technology, gate delay models [24]-[27] do not consider the influence of overshooting effect. Since the advent of submicron range, the second-order effects which include input slope and input-to-output coupling effects become dominant factors. Then the overshooting effect becomes a concern factor in order to improve the accuracy while modeling the gate delay. Nowadays, nanometer technology is so common for digital VLSI, because of which, overshooting effect is specially researched in order to maintain the accuracy of gate delay models. Especially, the overshooting effect of CMOS inverter attracts the concern of researchers. And some overshooting effect models for CMOS inverter [3][4] are proposed with high accuracy.

However, in spite of the significant influence of overshooting time on the gate delay of multiple-input gates, overshooting effect models for multiple-input gates are seldom proposed. In traditional gate delay and power consumption models for multiple-input gates, the method of simplifying the multiple-input gate to an inverter is commonly used. Unfortunately, these simple reduction methods will cause large error while modeling the overshooting effect of multiple-input gates. Furthermore, the conventional overshooting effect models for an inverter [3][4] are not easily extended to calculate the overshooting time of multiple-input gates.

Therefore, modeling the overshooting effect of multiple-input gates is chosen as the research topic in this dissertation which should be helpful for improving the accuracy of gate delay models if considering the overshooting effect.

Chapter3
Modeling the Overshooting Effect of 2-Input Gates in Nanometer Technologies

When the CMOS process technology enters nanometer regime, the overshooting effect of multi-input gate is important for gate delay calculation. However, the model to predict the overshooting effect of multi-input gate is seldom. In this chapter, a overshooting effect model for 2-input gates is proposed.

Firstly, 2-input NOR gate is chosen to be researched. There are two different input conditions for a 2-input NOR gate. Under the first input condition, the overshooting time equations is proposed based on the overshooting effect model for an inverter in [3]. For the second input condition, the proportional coefficient method is used to model the overshooting effect. Moreover, the proposed model for 2-input NOR gate can also be extended to 2-input NAND gate condition. In this chapter, how to extend the overshooting effect model of 2-input NOR gate to 2-input NAND gate is briefly presented.

In order to verify the accuracy of the proposed model, a number of simulations are given. The overshooting times of 2-input NOR gate and 2-input NAND gate are obtained from the proposed model and SPICE simulations using CMOS 32nm PTM model [43]. The error of the results from the proposed model is no more than 3.6% compared with the results from SPICE simulations. Therefore, the proposed model is useful when modeling the overshooting effect for 2-input gates.

3.1 Introduction

With digital integrated circuits entering nanometer age, the overshooting effect which is induced by input-to-output coupling capacitance strongly affects CMOS gate delay analysis, especially the static timing analysis. For traditional long channel transistors, the overshooting time is generally ignored because the coupling capacitance is small and the overshooting effect can usually be neglected [40]. However, with the scaling of gate feature sizes, the overshooting time is becoming equal to gate delay or even larger than that [46]. Therefore, the overshooting effect should be especially considered during the analysis of gate delay, otherwise the expression of gate delay would be inaccurate.

Traditional models of gate delay have been widely studied [24]-[27][48][52][54]. Alpha-power law MOSFET model is applied to derive closed-form equation for evaluating the propagation delay in [25]. An extension to the delay expression of [25] is presented in [26] to deal with the case of very lightly loaded inverter and/or slow input signals. However, neither [25] nor [26] takes consideration of the overshooting effect when analyzing gate delay. In the submicron range, the second-order effect which includes input slope and input-to-output coupling effect becomes the dominant factor. Although the overshooting effect which is induced by the input-to-output coupling effect is taken into account in the form of constant value or very simple expression in [31]-[33][41][42], there still have been few researchers focusing on the analysis of the overshooting effect in the level of nanometer technologies.

A detailed expression of the overshooting time for an inverter in nanometer technology is obtained by complete calculation and reasonable approximation in [3]. However, the overshooting effect of multi-input gate is still not considered too much. Therefore, that effect is analyzed specifically in this chapter. A basic two-input CMOS NOR gate is chosen as the research object and a practical model of CMOS NOR gate considering the overshooting effect is proposed. The specific expression of the overshooting time for the CMOS NOR gate is obtained from some reasonable

calculation and approximation. Moreover, the proposed model is verified by comparing with SPICE simulation results using CMOS 32-nm PTM model [43]. The simulation results turn out that the accuracy of the proposed model is within 3.6% error. Furthermore, the proposed model can be easily extended to CMOS NAND gate according to the same principles.

In this chapter, modeling the overshooting effect of multi-input gates is researched. The rest of this chapter is composed of five sections. First, the overshooting effect of 2-input NOR gate is clarified in Sect. 3.2. Then the model of the overshooting effect for 2-input NOR gate is proposed specifically in Sect. 3.3. After that, the extension method of the proposed model to 2-input NAND gate is presented in Sect. 3.4. Moreover, the simulation results of the proposed model are shown in Sect. 3.5. At last this chapter is concluded in Sect. 3.6.

3.2 Preliminaries

The overshooting time t_{ov} is now a key component of multi-input gate delay in nanometer regime with the scaling of CMOS process technology. Figure 3.1 shows a 2-input CMOS NOR gate taking into account gate-to-drain coupling capacitances and gate-to-source coupling capacitances.

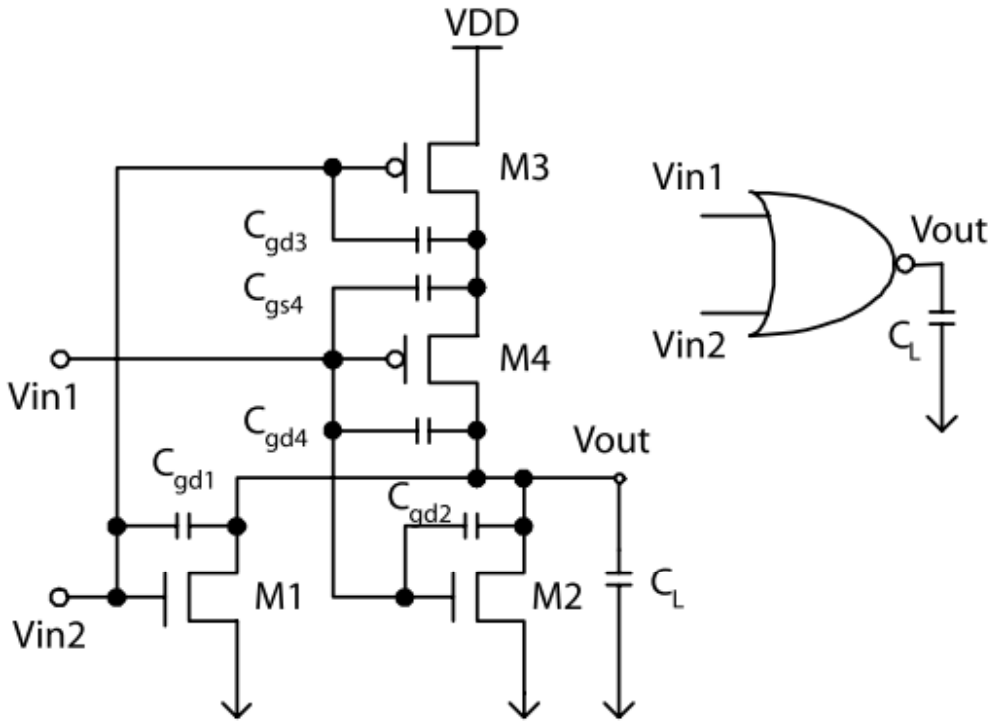

Figure 3.1 CMOS NOR gate considering parasitical coupling capacitance.

Figure 3.2 shows the output voltage V_{out} of the 2-input NOR gate in the case that V_{in2} is connected to a falling signal and V_{in1} is directly connected to the ground by using CMOS 32nm PTM model [43]. In Fig. 3.2, t_D is the gate delay time defined as the time elapses from $V_{in2} = 0.5V_{DD}$ to $V_{out} = 0.5V_{DD}$, t_{ov} is the overshooting time which is time period when the output voltage is below zero, t_r is the output voltage rise time from $t = t_{ov}$ to the time when $V_{out} = 0.5V_{DD}$, t_{in} is the input signal transition time of V_{in2}. Thus, the delay time t_D can be expressed as

$$t_D = t_{ov} + t_r - \frac{t_{in}}{2}. \tag{3.1}$$

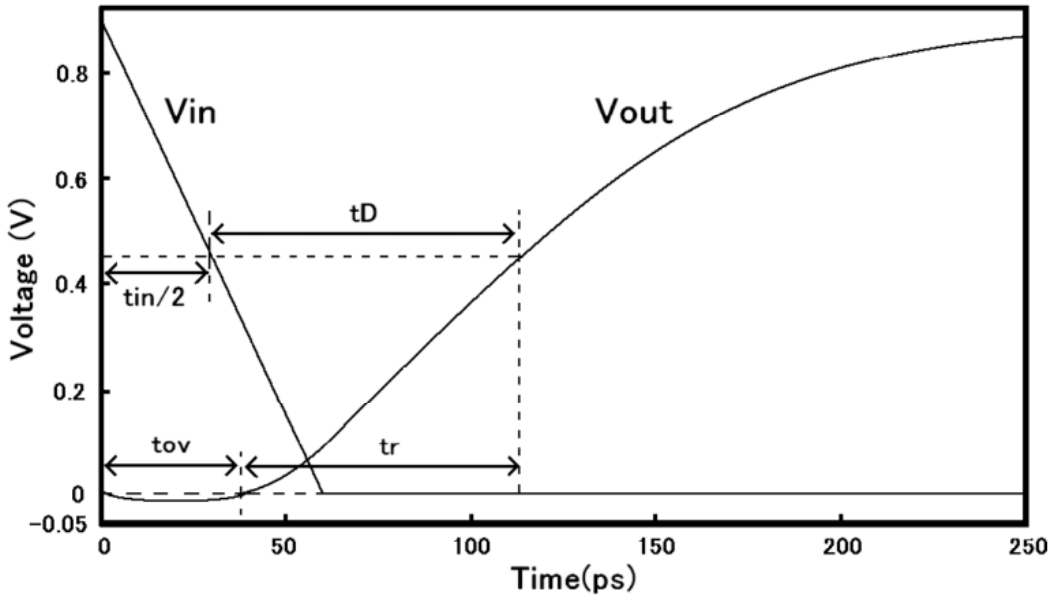

Figure 3.2 Output voltage of CMOS NOR gate.

As introduced in Chapter 2, the overshooting effect of multi-input gates has a significant influence on gate delay calculation. Therefore, modeling the overshooting effect of 2-input gates is proposed in subsequent sections.

3.3 Proposed Model

In this section, the model of calculating the overshooting time for 2-input NOR is proposed. In order to simplify the analysis of modeling the overshooting effect of 2-input NOR gate in Fig. 3.1, we discuss two different input conditions separately. The first input condition is that a falling signal is applied to V_{in1} and V_{in2} is connected to the ground. The second input condition is that $V_{in1} = 0$ and the falling signal is connected to V_{in2}. Similar expressions can be obtained if the falling signals are changed to rising signals. In this chapter, the falling signal is defined as

$$V_{in} = \begin{cases} V_{DD}: t \leq 0 \\ \left(1 - \frac{t}{t_{in}}\right) V_{DD}: 0 < t \leq t_{in} \\ 0: t > t_{in} \end{cases}. \quad (3.2)$$

Moreover, in this research, the condition when two inputs switch together will be not considered because the 2-input NOR gate can be simplified to an inverter after merging the transistors with the same inputs when the two inputs switch simultaneously.

3.3.1 When V_{in1} switched

Firstly, the analysis is given to the case as shown in Fig. 3.3, where the transistor M1 is not considered because the voltage of its four terminals are almost zero during the overshooting period. At the same time, M3 operates almost in the triode region, and is regarded as an active resistance during the overshooting period. The coupling capacitance C_{gd3} is not considered because the voltage between two nodes of the capacitance is almost constant during the overshooting period. Thus, the analysis for the 2-input NOR gate is similar to that for an inverter.

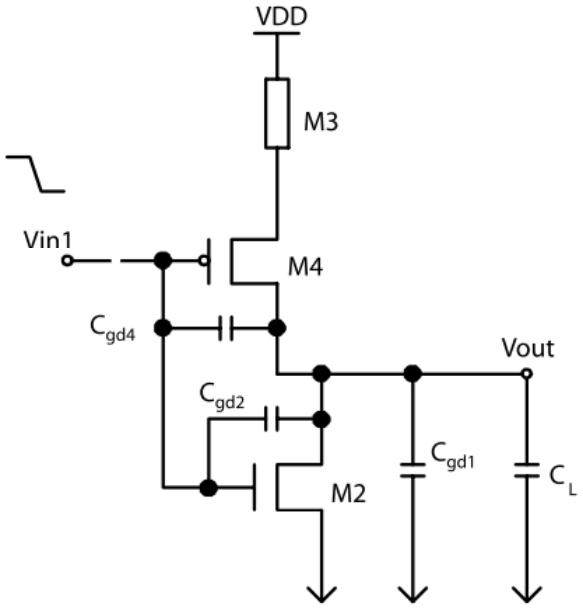

Figure 3.3 CMOS NOR gate under the condition V_{in1}: High-Low V_{in2}: GND.

For the simplified 2-input NOR gate as shown in Fig. 3.3, the α-power MOSFET model [25] is applied to calculate the current of the PMOS transistor. In order to simplify the numerical procedures, the drain current I_P of M4 is expressed with linear approximation as shown below:

$$I_{M4}(t_{ov}) = I_{D0}\left(\frac{|V_{GS}|-|V_{TPL}|}{V_{DD}-|V_{TPL}|}\right), \tag{3.3}$$

where I_{D0} is the drain current of a PMOS in saturation at $V_{GS} = V_{DS} = V_{DD}$(V_{GS} and V_{DS} are the gate-source and drain-source voltages of the PMOS, respectively), V_{TPL} is the equivalent threshold voltage whose value is shown in Fig. 3.4. Actually it is shown in Fig 3.4 that the linear approximation of the drain current for M4 is almost identical as SPICE simulation results. Thus, the linear approximation equation in Eq. (3.3) can be used to reflect the drain current of M4.

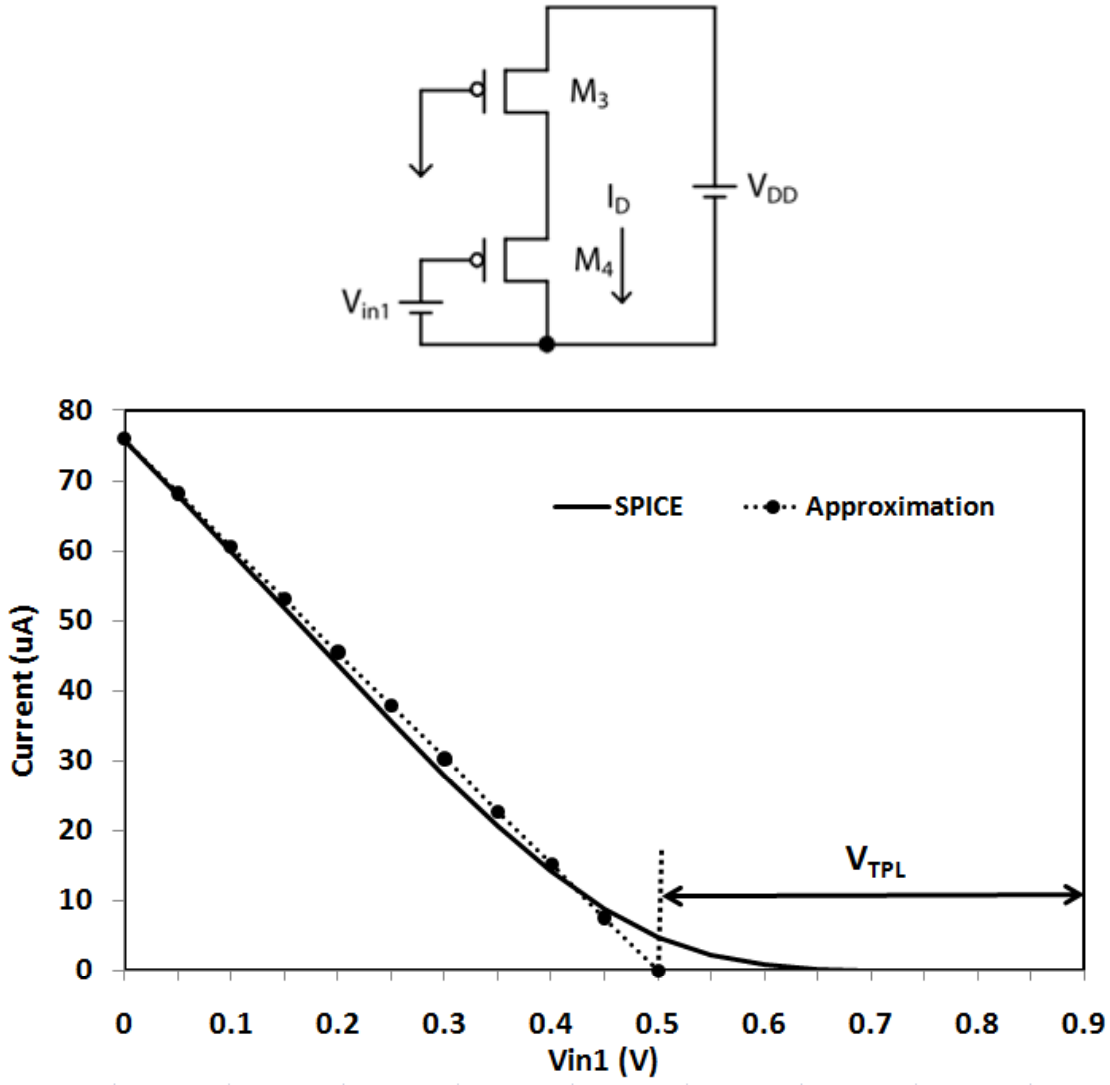

Figure 3.4 The linear approximation for PMOS transistor drain current.

Therefore, the expressions of the overshooting time t_{ov} for the simplified circuit in Fig. 3.3 can be obtained using the method in [3]. Firstly, an initial expression of the overshooting time t_{ov} is calculated using the linear approximation of drain current for M4. The initial t_{ov} is expressed as

$$t_{ov1} = t_{Vmin} - t_{\gamma} + \sqrt{\frac{2Q_1}{I_{D0}}(t_{in} - t_{TPL}) + t_{\gamma}^2}\,, \tag{3.4}$$

where

$$t_{\gamma} = \frac{1}{2}\left[t_{Vmin} - t_{TPL} - C_M \frac{V_{DD}}{t_{in}} \frac{t_{in} - t_{TPL}}{I_{D0}}\right]. \tag{3.5}$$

In Eqs. (3.4) and (3.5), t_{vmin} is the time when the output voltage is at its minimum.

$t_{TPL} = \frac{|V_{TPL}|}{V_{DD}} t_{in}$. Also, Q_1 is the charge flowing out of the load capacitance C_L and C_{gd1}. In this section, the values of t_{vmin} and Q_1 is obtained using the method similar to [3]. Moreover, C_M is the coupling capacitance and in this section C_M is expressed as

$$C_M = C_{gd2} + C_{gd4}\,. \tag{3.6}$$

The value of C_{gd1} will be constant because the transistor M1 is always off. The value of C_{gd4} is also almost constant because the transistor M4 will work in the cut off region or the saturation region during the overshooting period. However, the transistor M2 will change from linear region to the cut off region during the overshooting period. Therefore, the value of C_{gd2} will be not always constant. According to many verifications, we find the change of C_{gd2} is not very large. We use the average capacitance value of C_{gd2} at $V_{in1} = V_{DD}$ and $V_{in1} = 1/2V_{DD}$. In the proposed model, the values of coupling capacitances are obtained from the SPICE simulation results.

The initial value of the overshooting time in the expression (3.4) is not accurate enough. Therefore, the initial t_{ov1} is substituted into the α-power MOSFET model to get a new drain current of M4 $I_P(t_{ov})$. Then the final overshooting time for the first input condition when Vin1 switched is expressed as

$$t_{ov1} = \frac{2Q_1}{C_M \frac{V_{DD}}{t_{in}} + I_P(t_{ov})} + t_{Vmin}\,. \tag{3.7}$$

3.3.2 When V_{in2} Switched

For the second input condition as shown in Fig. 3.5, the analysis becomes more complicated because the influence of the coupling capacitance C_{gs4} should also be considered. However, from $t = t_{ov}$ to $t = t_r$, M4 operates almost in the triode region, and is regarded as an active resistance. Then the 2-input NOR gate in Fig. 3.5 is simplified as shown in Fig. 3.6.

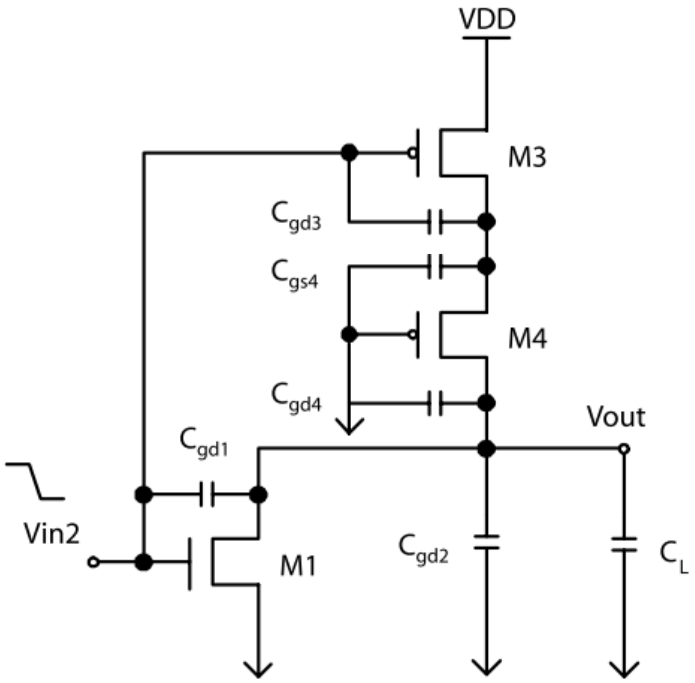

Figure 3.5 CMOS NOR gate under the condition V_{in1}: GND V_{in2}: High-Low.

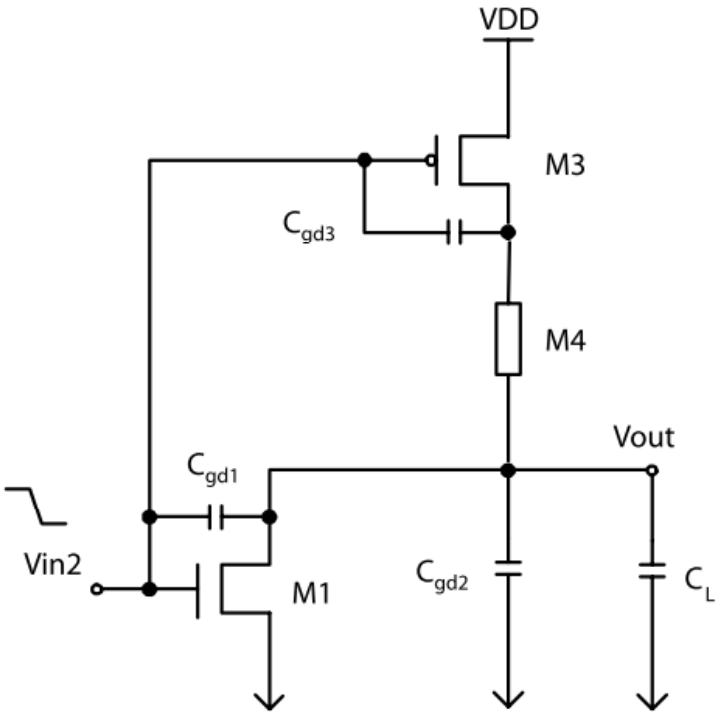

Figure 3.6 Simplified CMOS NOR gate under the condition V_{in1}: GND V_{in2}: High-Low.

Through various simulation verification works under different conditions, we find that the overshooting time t_{ov2} of the simplified NOR gate in Fig. 3.6 is

approximately proportional to the overshooting time t_{ov1} of the simplified circuit in Fig. 3.3 as shown in Fig. 3.7.

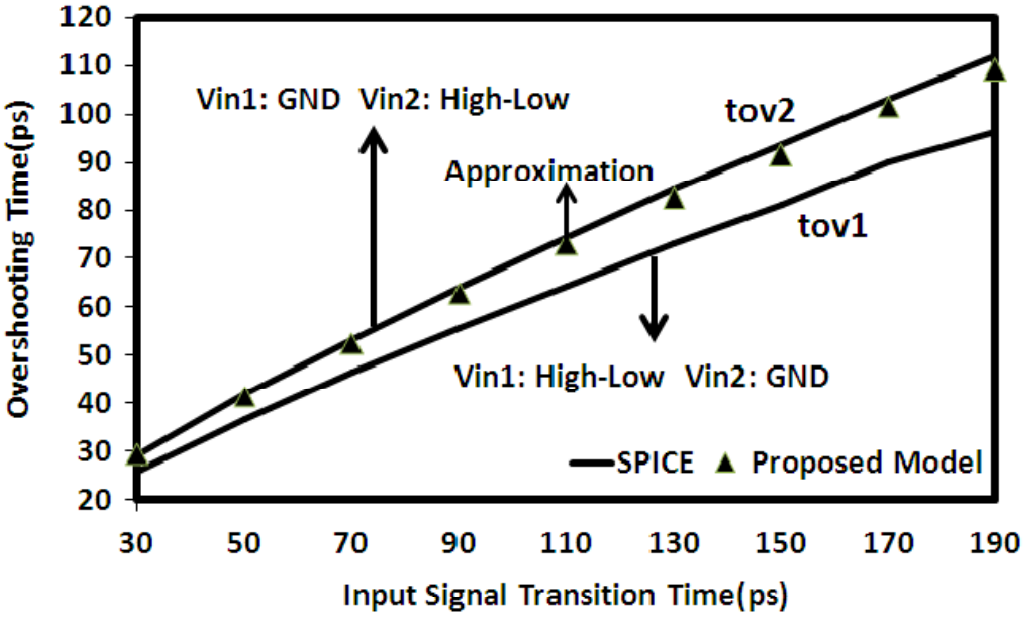

Figure 3.7 The linear approximation for the overshooting time.

In Fig. 3.7, the overshooting time of 2-input NOR gate in Fig. 3.3 obtained from the SPICE simulations is shown by the lower line. The upper line shows the overshooting time of 2-input NOR gate in Fig. 3.6 whose value is obtained from the SPICE simulations. The triangle in Fig. 3.7 shows the overshooting time of the 2-input NOR gate in Fig. 3.6 using the proportional coefficient method. We can find the triangles almost overlap the upper line. That means the proportional coefficient method can predict the overshooting time of the 2-input NOR gate in Fig. 3.6. Therefore, we can obtain t_{ov2} referring to the value of t_{ov1} as shown below:

$$t_{ov2} = \lambda t_{ov1} . \tag{3.8}$$

Figures 3.8-3.10 are the simulation verifications of the Eq. (3.8) under different input signal transition times, transistor sizes and load capacitances. All these results are obtained from SPICE simulations. The length of NMOS and PMOS are $L_N = L_P = 40\text{nm}$.

Figure 3.8 shows the ratio of t_{ov2} to t_{ov1} under different input signal transition times. The load capacitance is $C_L = 0.01\text{pF}$ and the transistor size is $W_P = W_N =$

0.8um/0.4um. It can be seen that the ratio has little change with the increase of input signal transition times.

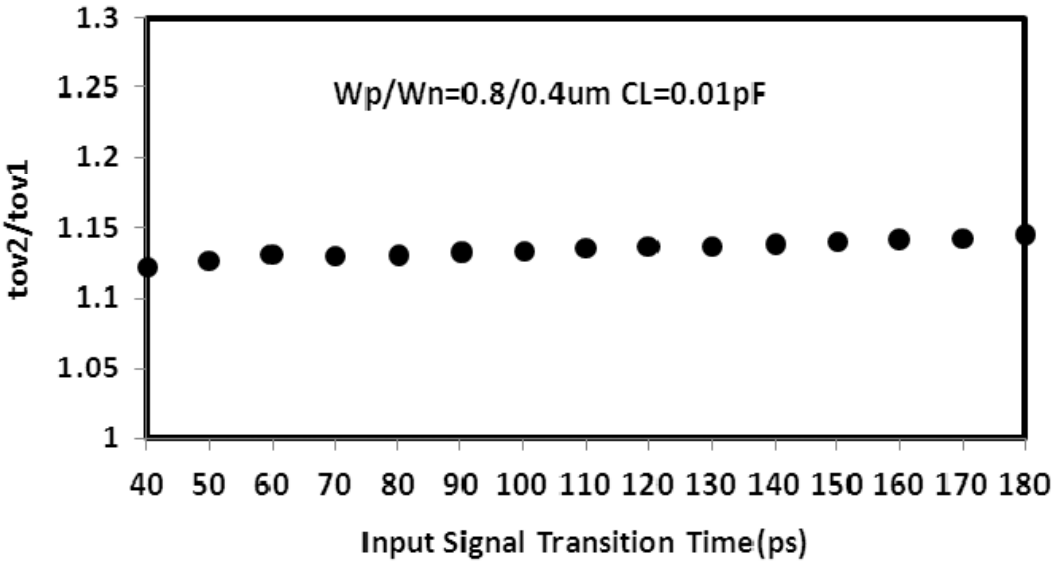

Figure 3.8 t_{ov2}/t_{ov1} versus different input signal transition time.

Figure 3.9 show the ratio of t_{ov2} to t_{ov1} under different NMOS widths. The PMOS' width is two times of NMOS' width. The input signal transition time is $t_{in} = 100ps$ and the load capacitance is $C_L = 0.02pF$. When the transistor size changes, the ratio almost remains a constant value.

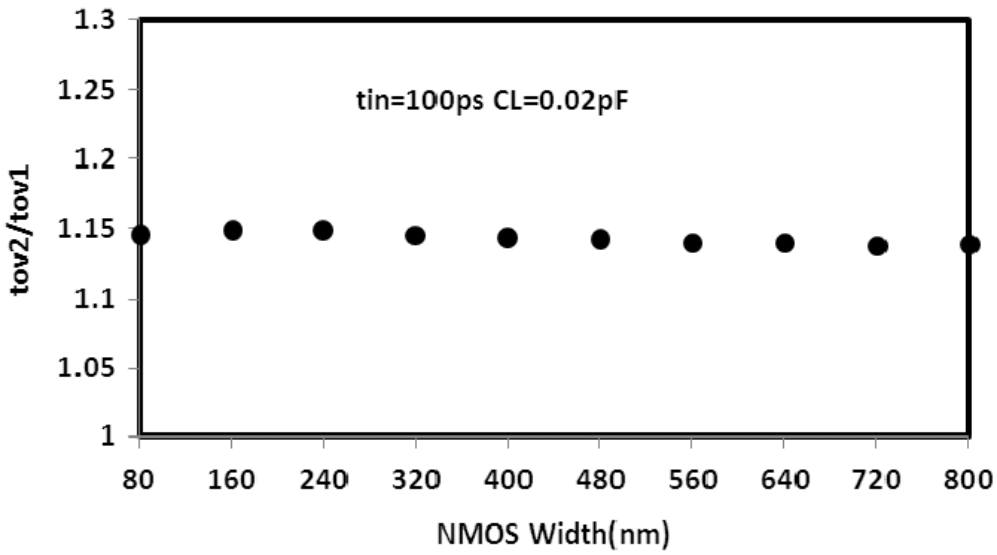

Figure 3.9 t_{ov2}/t_{ov1} versus different gate sizes.

Figure 3.10 shows the ratio of t_{ov2} to t_{ov1} under different load capacitances. The input signal transition time is $t_{in} = 140ps$ and the transistor size is $W_P = W_N = 2.4um/1.2um$. When the load capacitances change, the ratio varies little.

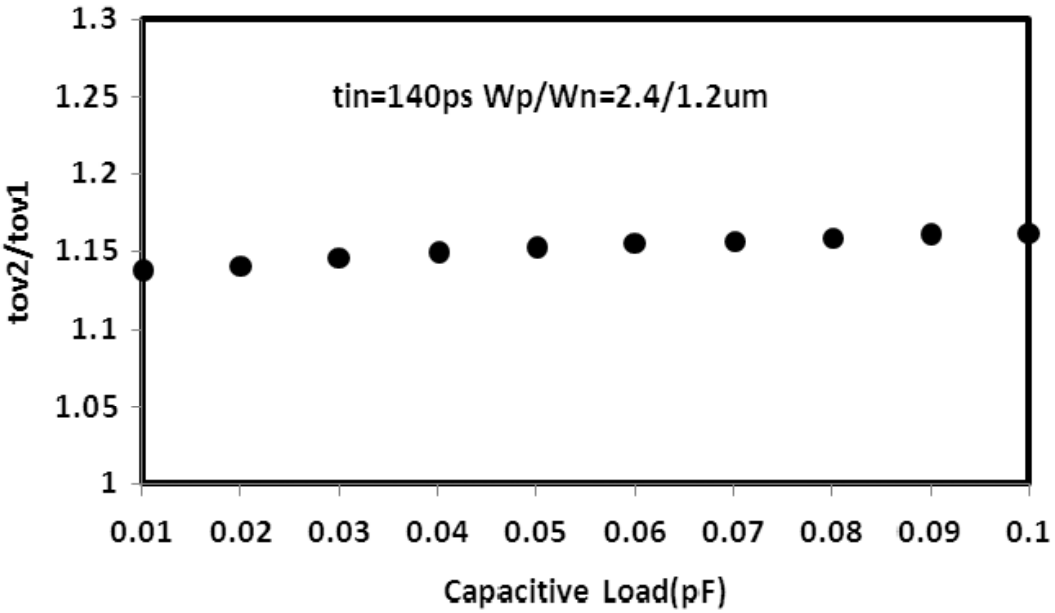

Figure 3.10 t_{ov2}/t_{ov1} versus different capacitive loads.

Through the verification results as shown in Figs.3.8-3.10, we can find that the ratio is almost constant and the value is approximately equal to 1.14. Therefore λ is about 1.14 for the 32nm PTM model [43]. Based on other numerous simulation verification works under various conditions, it is demonstrated that λ makes little change with the variation of input signal transition times, transistor sizes and load capacitances. Additionally, λ for different process technology can be obtained in the similar way.

3.4 Extension to 2-input NAND Gate

The proposed model in Sect. 3.3 can also be extended to 2-input NAND gate. In this section, the overshooting effect model for 2-input NAND gate is briefly presented.

A CMOS 2-input NAND gate considering the coupling capacitances are shown in Fig. 3.11.

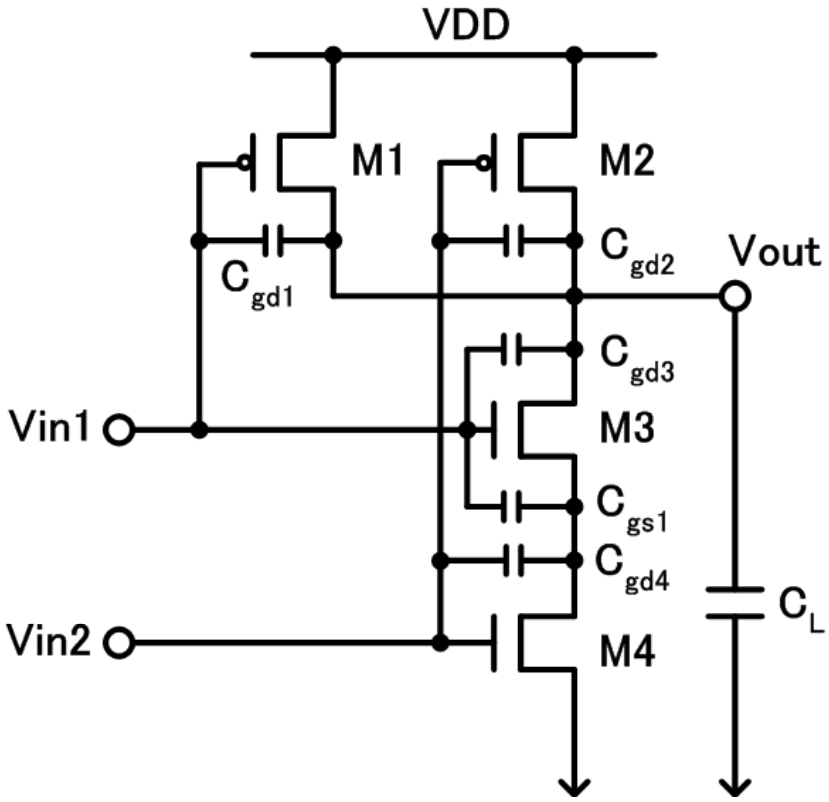

Figure 3.11 2-input NAND gate considering the coupling capacitances

C_{gd1}, C_{gd2}, C_{gd3}, C_{gd4} and C_{gs1} are coupling capacitances. C_L is the load capacitance. In order to simplify the analysis, two different input conditions are considered. The first condition is V_{in1} connected to a falling signal and V_{in2} is connected to V_{DD}. The second condition is $V_{in1} = V_{DD}$ and V_{in2} is connected to a falling signal.

Under the first input condition, the 2-input NAND gate can be simplified to the circuit as shown in Fig. 3.12. Because M2 is always cut off, it is not considered.

Meanwhile, the transistor M4 works in the linear region during the overshooting period, it can be regarded as a resistor.

After the simplification, the circuit in Fig. 3.12 is similar as the circuit in Fig. 3.3. The principle in Sect. 3.3.1 is verified still useful to calculate the overshooting time of the circuit in Fig. 3.12. The overshooting time of the circuit in Fig. 3.12 can be expressed as

$$t_{ov1} = t_{Vmin} - t_{\gamma} + \sqrt{\frac{2Q_1}{I_{D0}}(t_{in} - t_{TPL}) + t_{\gamma}^2}\,, \tag{3.9}$$

where

$$t_{\gamma} = \frac{1}{2}\left[t_{Vmin} - t_{TPL} - (C_{gd1} + C_{gd3})\frac{V_{DD}}{t_{in}}\frac{t_{in} - t_{TPL}}{I_{D0}}\right]. \tag{3.10}$$

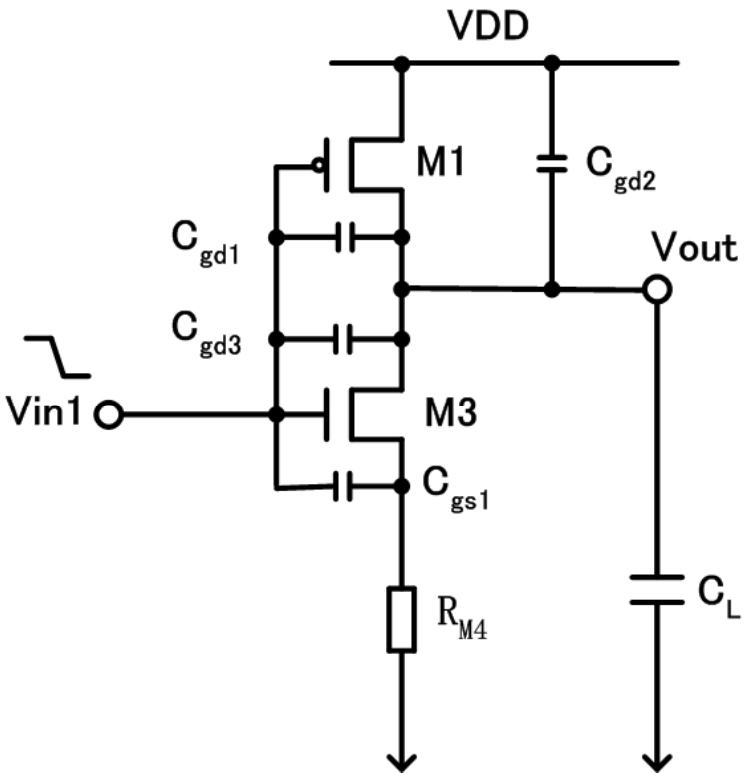

Figure 3.12 2-input NAND gate when V_{in1} switched.

Although the structure of Eqs. (3.9) and (3.10) are same as Eqs. (3.4) and (3.5), the parameters Q_1 and t_{vmin} are different. In Eqs. (3.4) and (3.5), Q_1 and t_{vmin} are same as the parameters for the inverter model of [3] which is shown in Eqs. (2.12), (2.13) and (2.18). However, for the circuit in Fig. 3.12, the parameter $V_{out}(t_{TP})$ which is the component of Q_1 has the different expression:

$$V_{out}(t_{TP}) = \frac{(C_{gd1}+C_{gd3})\frac{dV_{in}}{dt}}{\beta_n(V_{DD}-|V_{TP}|-V_{TN})}\left[1 - e^{-\frac{\beta_n(V_{DD}-|V_{TP}|-V_{TN})}{C_{gd1}+C_{gd2}+C_{gd3}+C_L}\frac{t_{in}|V_{TP}|}{V_{DD}}}\right]. \quad (3.11)$$

The parameter t_{vmin} in Eqs. (3.9) and (3.10) is expressed as

$$t_{vmin} = t_{TP} + (t_{in} - t_{TP})\left[\frac{(C_{gd1}+C_{gd3})V_{DD}}{I_{D0}t_{in}} e^{-\frac{\beta_n(V_{DD}-|V_{TP}|-V_{TN})}{C_{gd1}+C_{gd2}+C_{gd3}+C_L}\frac{t_{in}|V_{TP}|}{V_{DD}}}\right]^{\frac{1}{\alpha}}. \quad (3.12)$$

After these calculations, the second time calculation for the overshooting time used in Sect. 3.3.1 is also applied to obtain the final accurate overshooting time of the circuit in Fig. 3.12.

Under the second input condition when V_{in2} is switched, the 2-input NAND gate is simplified to the circuit as shown in Fig. 3.13. The transistor M1 is not considered because it is always cut off. The transistor M3 is replaced with a resistor.

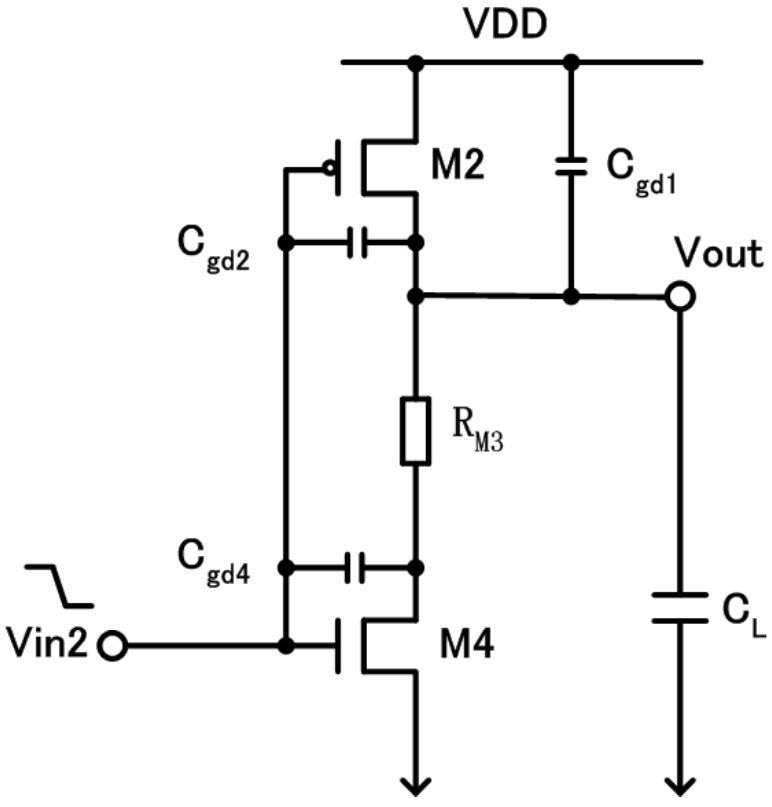

Figure 3.13 2-input NAND gate when V_{in2} switched

For this condition, the proportional coefficient method used in Sect. 3.3.2 is still useful for the circuit in Fig. 3.13. Then the overshooting time of the 2-input NAND

gate in Fig. 3.13 can be expressed as

$$t_{ov2} = \lambda' t_{ov1} \,. \tag{3.13}$$

According to various verification works, λ' is approximately equal to 0.94 for CMOS 32nm PTM model.

3.5 Simulation Results

The overshooting effect model of 2-input NOR gate is proposed in Sect. 3.3. The proposed model can also be extended to 2-input NAND gate which is simply presented in Sect. 3.4. In order to verify the accuracy of the proposed model, some simulation works are done. The overshooting time of the gates obtained from the proposed model and SPICE simulations using 32nm PTM model is shown in this section. Firstly, the simulation results for 2-input NOR gate is given. Then the condition of the 2-input NAND gate will be considered.

3.5.1 t_{ov} for 2-input NOR Gate

Figures 3.14−3.16 show the overshooting time obtained from the proposed model and SPICE simulations for the 2-input NOR gate in Fig. 3.3 with respect to various input signal transition times, transistor sizes and load capacitances using 32nm PTM model [43].

In Fig. 3.14, the overshooting time of 2-input NOR gate when V_{in1} switched obtained from the proposed model in Sect. 3.3.1 and SPICE simulations are shown. The input signal transition time t_{in} varies from 40 to 120ps. The length of MOS transistors is $L_p = L_n = 40\text{nm}$. Three kinds of width and load capacitances are considered. It can be seen from the simulation results that the overshooting time will increase with the increase of input signal transition time. Meanwhile, the error of the overshooting time obtained from the proposed model is no more than 3.5% compared with SPICE simulation results.

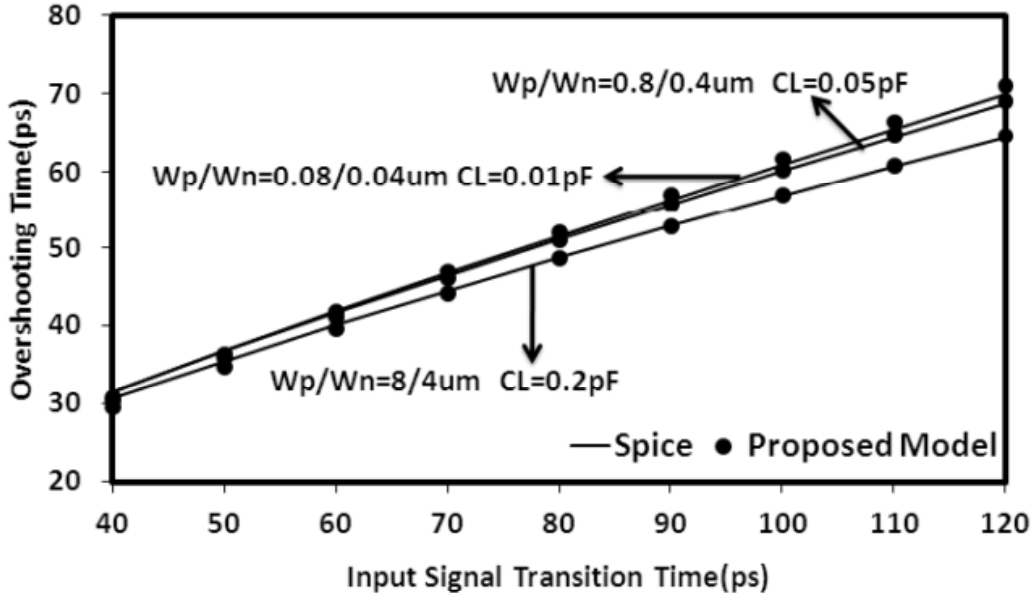

Figure 3.14 The overshooting time obtained from the proposed model and SPICE for CMOS NOR gate (Fig. 3.3) versus different input signal transition times.

Figure 3.15 shows the overshooting times of 2-input NOR gate in Fig. 3.3 obtained from the proposed model and SPICE simulations. There are three kinds of input signal transition times and load capacitances considered which is versus different CMOS sizes. The length of MOS transistors is $L_p = L_n = 40\text{nm}$ and the width of MOS transistors is $W_p = 2W_n$. The error of the proposed model is less than 3.1%. From the results shown in Fig. 3.15, it can be concluded that the overshooting time will decrease with the increase of the ratio W/L.

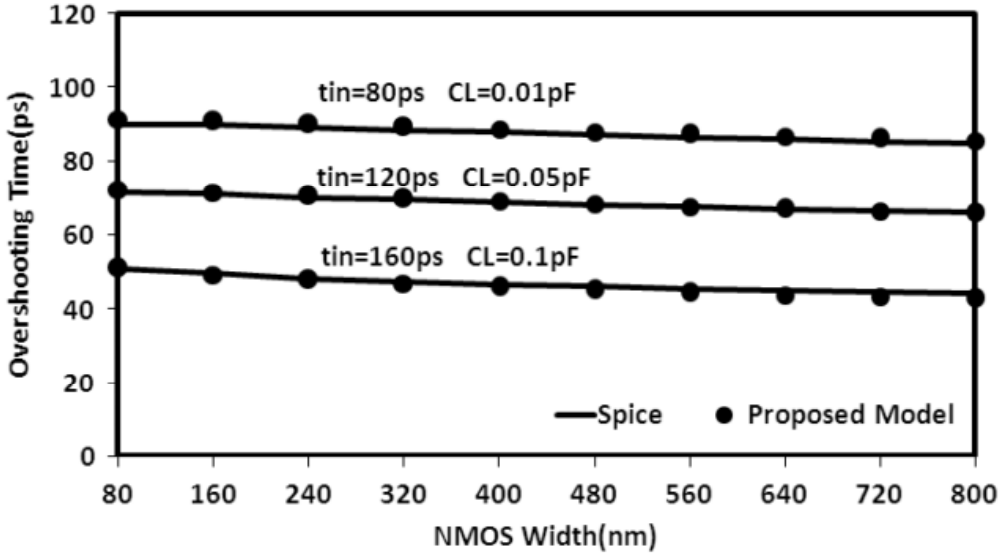

Figure 3.15 The overshooting time obtained from the proposed model and SPICE for CMOS NOR gate (Fig. 3.3) versus different transistors' sizes.

The overshooting time obtained from the proposed model in Sect. 3.3.1 and SPICE simulations versus different load capacitances are shown in Fig. 3.16. During these results, different input signal transition times and transistor sizes are considered. The error of the proposed model under this condition is below 2.5%. We can also find the overshooting time will increase with the increase of load capacitances.

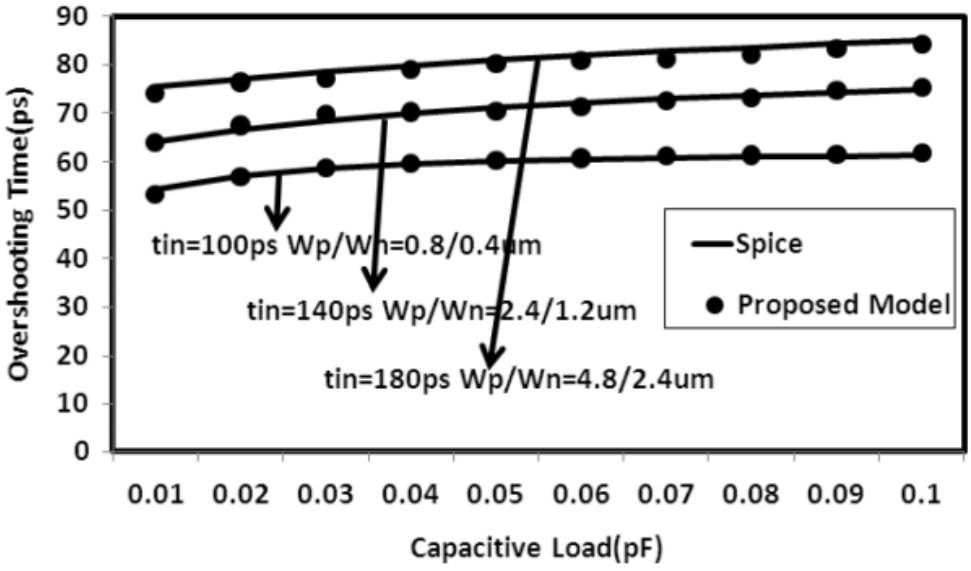

Figure 3.16 The overshooting time of the proposed model and SPICE simulations for CMOS NOR gate (Fig. 3.3) with respect to various load capacitances.

When V_{in2} of 2-input NOR gate in Fig. 3.1 is switched, the overshooting effect model is proposed in Sect. 3.3.2. Figures 3.17−3.19 show the overshooting time obtained from the proposed model in Sect. 3.3.2 and SPICE simulations using 32nm PTM model [43].

Figure 3.17 shows the overshooting time obtained from the proposed model in Sect. 3.3.2 and SPICE simulations versus different input signal transition times. The error is no more than 3.22%

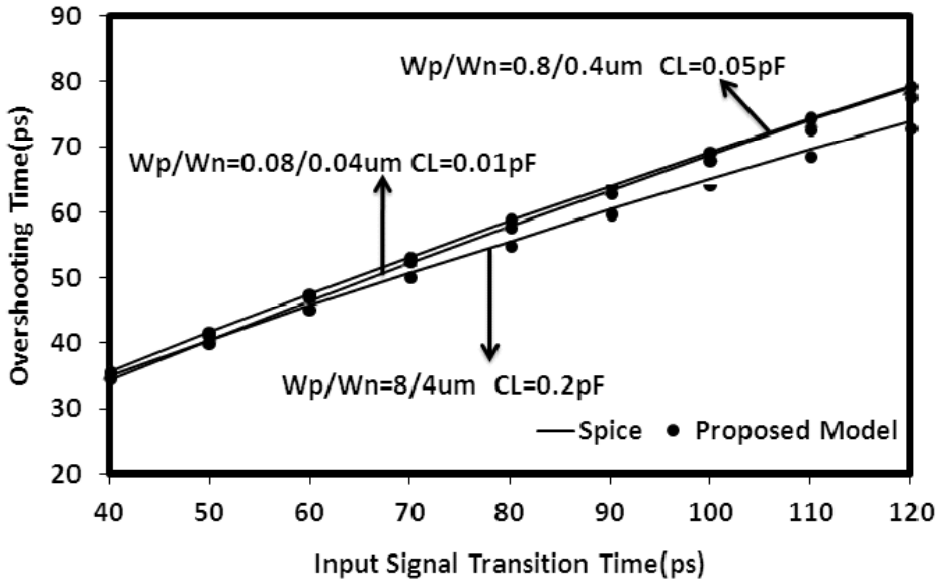

Figure 3.17 The overshooting time obtained from the proposed model and SPICE for CMOS NOR gate (Fig. 3.6) versus different input signal transition times.

The overshooting time obtained from the proposed model in Sect. 3.3.2 and SPICE simulations versus different transistor sizes are shown in Fig. 3.18. The error of the proposed model is less than 2.8%.

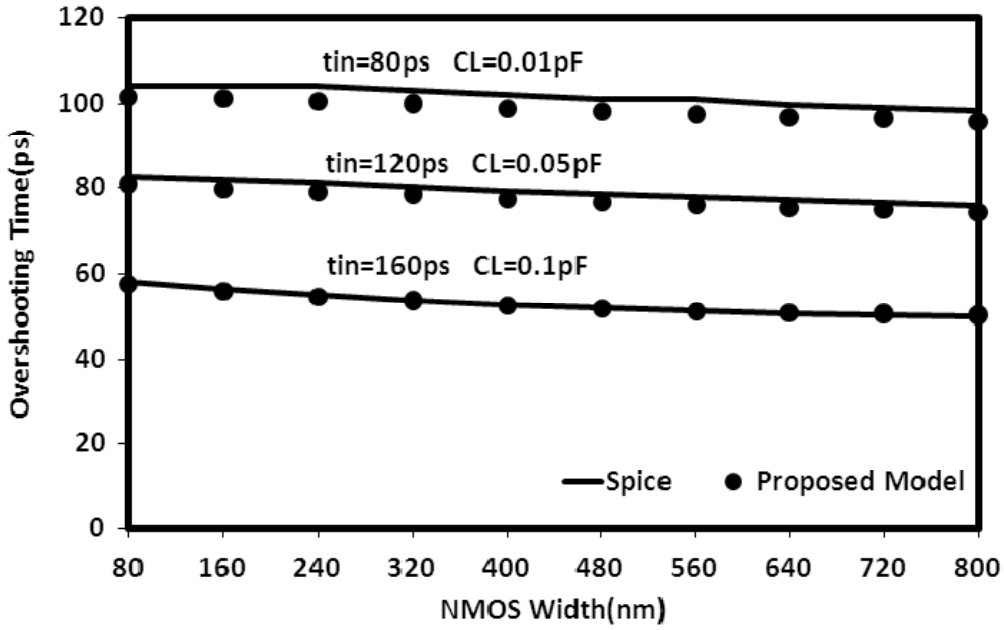

Figure 3.18 The overshooting time of the proposed model and SPICE simulations for CMOS NOR gate (Fig. 3.6) with respect to various transistors' sizes.

In Fig. 3.19, we consider the overshooting time obtained from the proposed model in Sect. 3.3.2 and SPICE simulations versus different load capacitances. The error is below 2.9%.

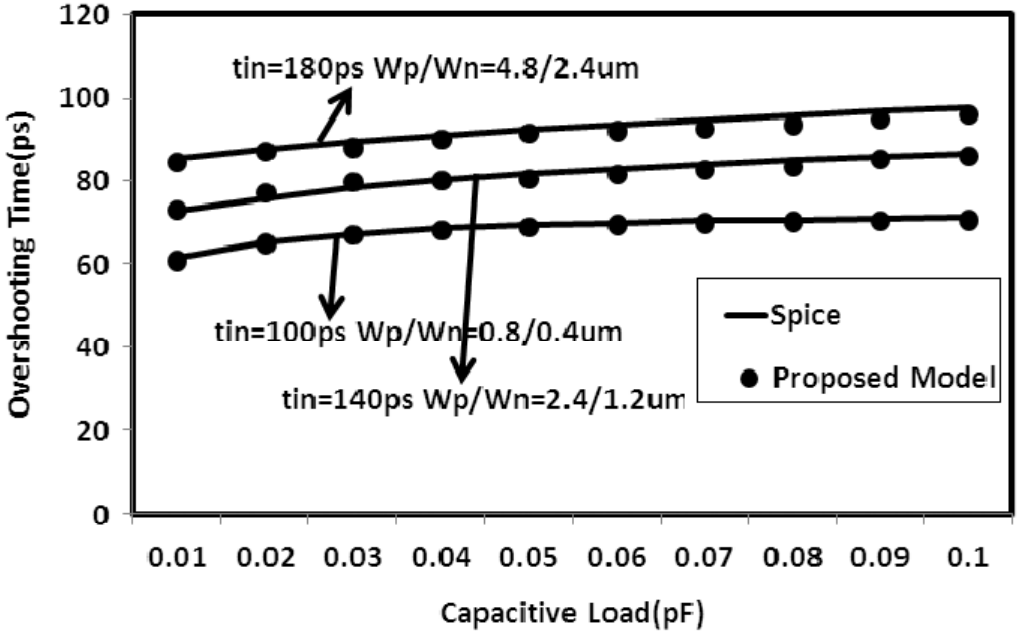

Figure 3.19 The overshooting time of the proposed model and SPICE simulations for CMOS NOR gate (Fig. 3.6) with respect to various load capacitances.

3.5.2 t_{ov} for 2-Input NAND Gate

In Sect. 3.3, the overshooting effect model for 2-input NOR gate is proposed. Based on the principles of the model in Sect. 3.3, the extension method to 2-input NAND gate is presented in Sect. 3.4. Therefore, verification works of Sect. 3.4 is given below.

Figures 3.20-3.22 shows the overshooting time of 2-input NAND gate in Fig. 3.11 under the condition when V_{in1} is switched. The overshooting time of the gate in Fig. 3.12 versus different input signal transition times, transistors' sizes and load capacitances are considered. The simulation conditions in Figs. 3.20-3.22 are same as the condition for the 2-input NOR gate in Sect. 3.5.1.

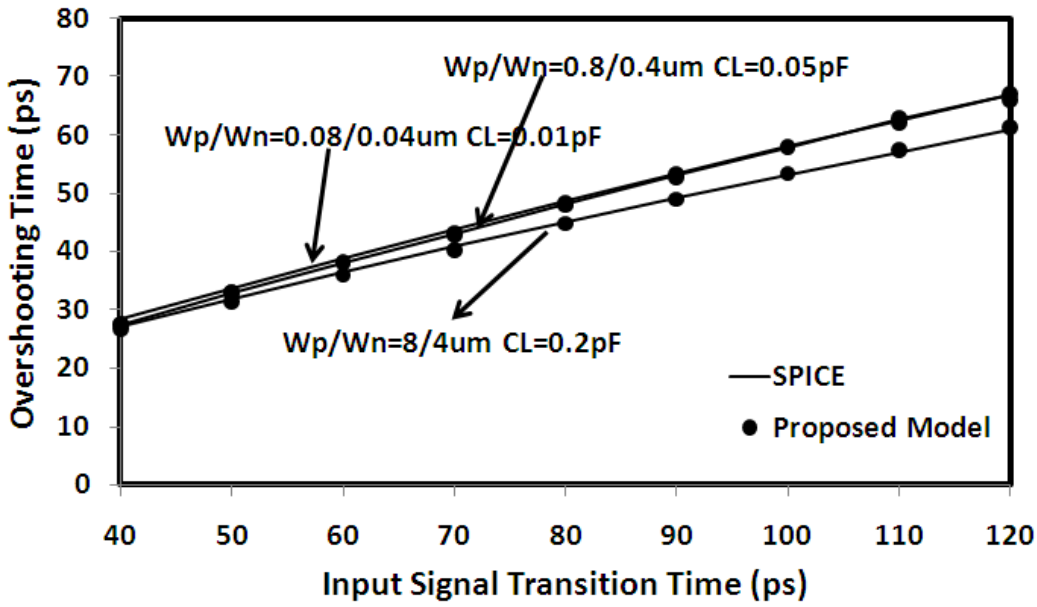

Figure 3.20 The overshooting time obtained from the proposed model and SPICE for CMOS NAND gate (Fig. 3.12) versus different input signal transition times.

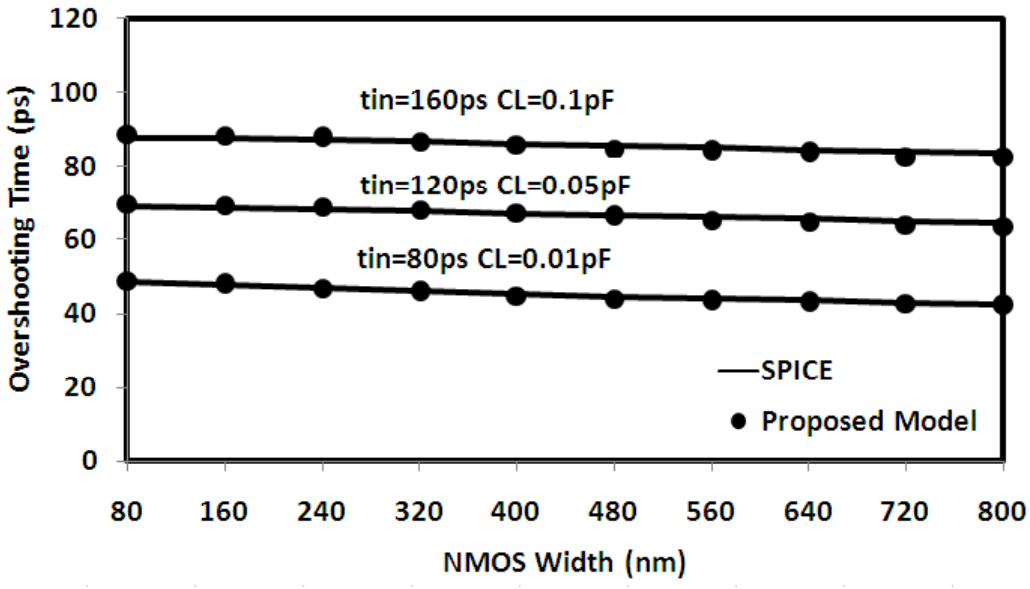

Figure 3.21 The overshooting time obtained from the proposed model and SPICE for CMOS NAND gate (Fig. 3.12) versus different transistors' sizes.

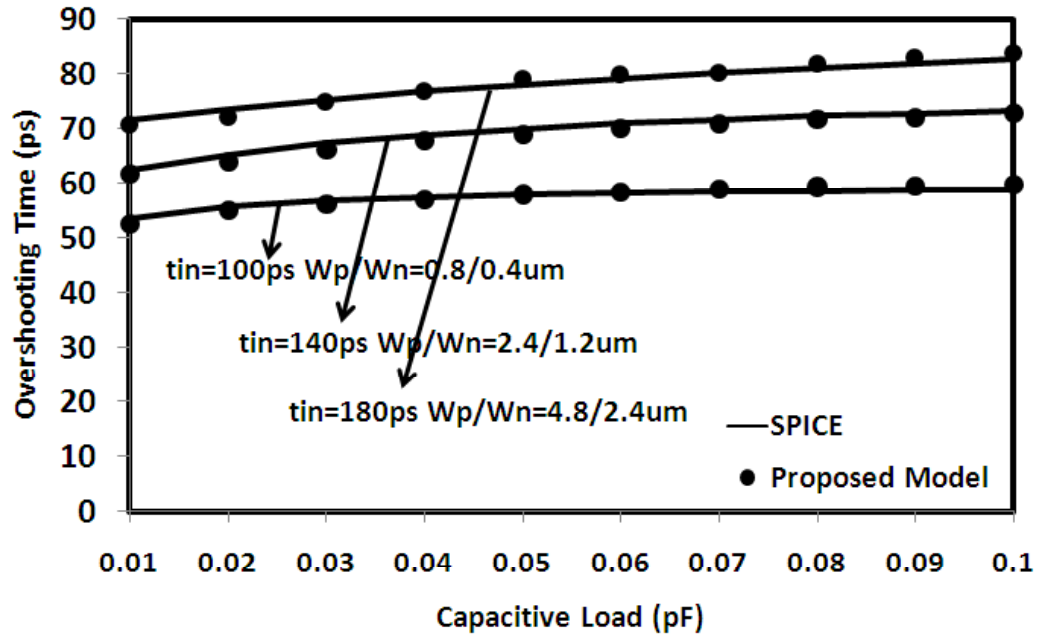

Figure 3.22 The overshooting time obtained from the proposed model and SPICE for CMOS NAND gate (Fig. 3.12) versus different load capacitances.

The maximum error of the proposed model in Figs. 3.20-3.22 is 2.64%, 1.41% and 2.14%, respectively.

The proportional coefficient method in Sect. 3.3.2 is also available when applied to 2-input NAND gate when V_{in2} switched as shown in Fig. 3.13. Verification of this condition is shown in Figs. 3.21 and 3.22.

Figures 3.23-3.25 shows the overshooting time obtained from the proposed model and SPICE simulations for the 2-input NAND gate in Fig. 3.13. Different input signal transition time, transistors' sizes and load capacitances are considered in Fig. 3.23-3.25. Meanwhile, the simulation conditions are absolutely same as the simulation for 2-input NOR gate in Sect. 3.5.1

The maximum error of the proposed model in Figs. 3.23-3.25 is 2.71%, 2.46% and 3.24%, respectively.

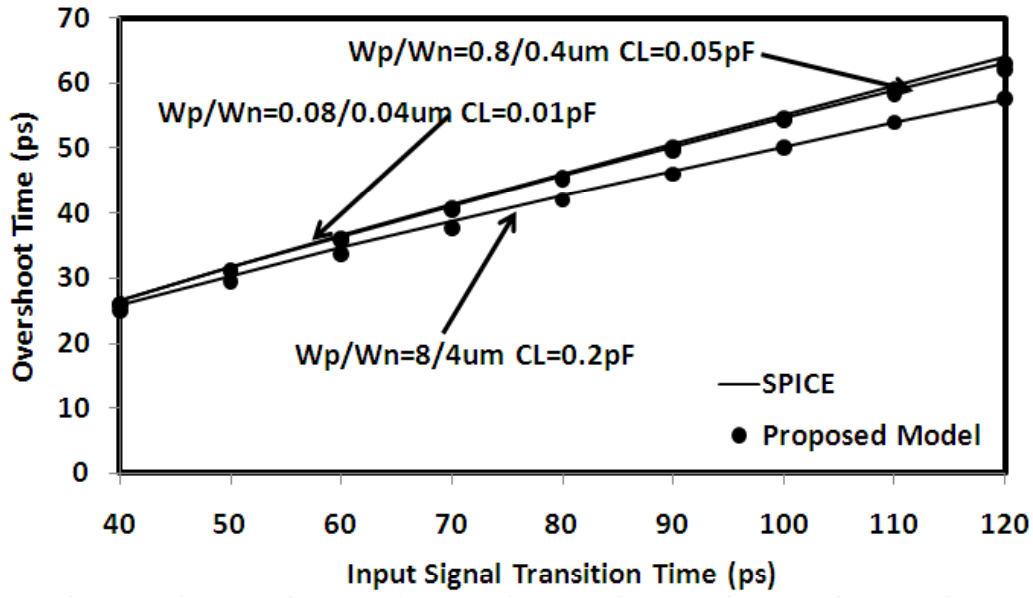

Figure 3.23 The overshooting time obtained from the proposed model and SPICE for CMOS NAND gate (Fig. 3.13) versus different input signal transition times.

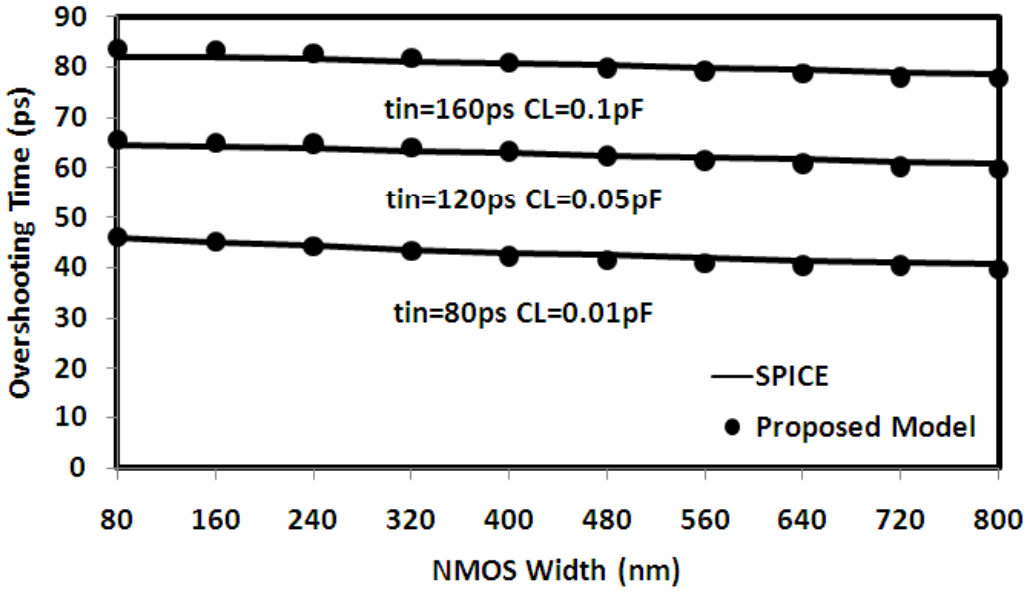

Figure 3.24 The overshooting time obtained from the proposed model and SPICE for CMOS NAND gate (Fig. 3.13) versus different transistors' sizes.

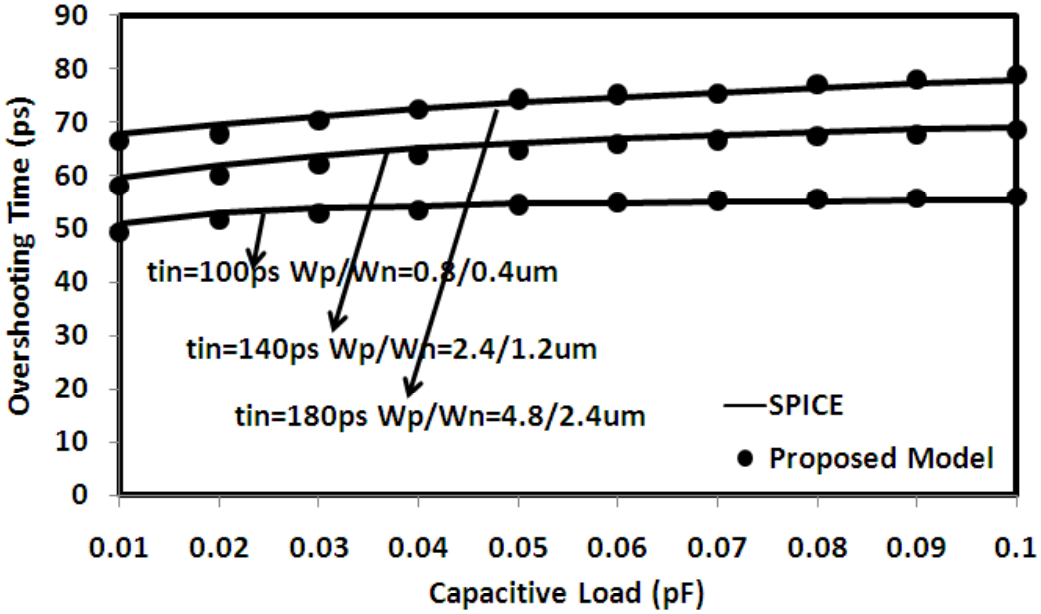

Figure 3.25 The overshooting time obtained from the proposed model and SPICE for CMOS NAND gate (Fig. 3.13) versus different load capacitances.

The simulation results in Sect. 5 shows that the overshooting time of 2-input NOR gate and 2-input NAND gate obtained from the proposed model is accurate compared with the results obtained from SPICE simulations. That means, the proposed model can accurately model the overshooting effect of multi-input gates.

3.6 Conclusions

When the CMOS process enters nanometer regime, the overshooting effect of multi-input gates is obvious and has a significant influence on gate delay calculation, modeling the overshooting effect of 2-input gates is researched in this Chapter.

Based on the overshooting effect model [3] for an inverter, the overshooting effect model for 2-input NOR gate when V_{in1} switched is presented. Subsequently, the proportional coefficient method is found useful to model the overshooting effect of 2-input NOR gate when V_{in2} switched. After proposing the overshooting effect model for 2-input NOR gate, it is extended to 2-input NAND gate. The overshooting effect model for 2-input NOR gate is found still available when applied to 2-input NAND gate.

In order to verify the accuracy of the proposed overshooting effect model, verification works are done. The overshooting time of 2-input NOR gate and 2-input NAND obtained from the proposed model and SPICE simulations are compared. When doing verification works, different input signal transition time, transistors' sizes and load capacitances are considered. The comparison results reflect that the overshooting time obtained from the proposed model is within 3.6% error. That means, the proposed overshooting effect model can predict the overshooting time of multi-input gates accurately.

Chapter4
An Effective Model of the Overshooting Effect for Multiple-Input Gates in Nanometer Technologies

In Chapter 3, the overshooting effect model for 2-input gates is proposed which can model the overshooting effect of 2-input NOR gates. The proposed model in Chapter 3 can also be extended to 2-input NAND gate. However, the model in Chapter 3 is not available if applied to multiple-input gates with more than two inputs. Moreover, when the CMOS process technology enters nanometer range, the overshooting effect of multiple-input gates is still obvious and the overshooting time of multiple-input gates also has an important influence on gate delay calculation. Therefore, an effective model of the overshooting effect for multiple-input gates is proposed in this Chapter.

In this Chapter, the formula-based overshooting effect model for 2-input gate is presented firstly. Based on the formula-based model, the method to calculate the overshooting time of 3-input gate is proposed. These proposed models can be easily extended to other multiple-input gates.

The verification work of the proposed model is also paid much attention in order to make sure the accuracy of the proposed model. Meanwhile, the application of the proposed overshooting effect model for multiple-input gates is also introduced.

4.1 Introduction

The overshooting effect, caused by the existence of input to-output coupling capacitances, is the phenomenon that the output signal of CMOS logics gets out of power supply at the beginning of transition [47]. When CMOS technology decreases to nanometer scale, the overshooting effect is much more obvious and the overshooting time becomes equal to gate delay or even larger than that. Therefore, it is necessary to develop an effective model of the overshooting effect for CMOS gates in order to avoid inaccuracies in estimating the gate delay and short circuit energy dissipation [3][4][47][55]. Traditionally, the gate delay models of CMOS logics [24]-[27][48] are related to transistors' sizes, input signal transition times, and output loads while the overshooting effect is not considered. Since the advent of submicron range, the second-order effects which include input slope and input-to-output coupling effects become dominant factors. Then the overshooting effect becomes a concern factor in order to improve the accuracy while modeling the gate delay or power consumption for CMOS logics [31][32][41][42]. Along with the further research, simple expressions describing the overshooting times of an inverter are given in the gate delay model and power consumption model in [33] and [39], respectively.

With the obviousness of the overshooting effect for CMOS gates in a nanometer regime, more and more attention has been paid to the research about modeling the overshooting effect for CMOS gates. Recently, accurate overshooting effect models for CMOS inverter are specially presented in [3][4][47]. For multiple-input gates, the overshooting effect is also obvious and has the same influence to gate delay and power consumption as an inverter. However, less work has been done to develop an effective overshooting effect model for multiple-input gates until now.

Therefore, modeling the overshooting effect for multiple-input gates in nanometer technologies is proposed in this paper. Firstly, specific expressions of the overshooting

time for 2-input NOR gate are given. Subsequently, the method to model the overshooting effect of 3-input NOR gate is proposed. Meanwhile how to extend the proposed model to other multiple-input gates is analyzed in detail. Finally, the overshooting times of different multiple-input gates calculated from the proposed model are verified within 3.4% error compared with SPICE simulation results using CMOS32nm PTM model [43].

The rest of this chapter is composed of five sections as follows. In Sect. 4.2, the background and advantage of the proposed model are analyzed. Section 4.3 presents the model of the overshooting effect for multiple-input gates. The experimental results are shown in Sect. 4.4. The application of the proposed model is discussed in Sect. 5. Finally, this chapter is concluded in Sect. 4.6

4.2 Preliminaries

Delay is a main performance metric for digital LSI. Predicting gate delay of CMOS logics is vitally important for Static Timing Analysis (STA). An accurate gate delay model will be very helpful for further analysis of digital LSI systems. Therefore, accuracy is an important criteria for gate delay models. Before submicron range, gate delay models of CMOS logics are still accurate enough without considering the overshooting effect. After entering the submicron range, the overshooting effect cannot be neglected again in order to obtain an accurate delay model.

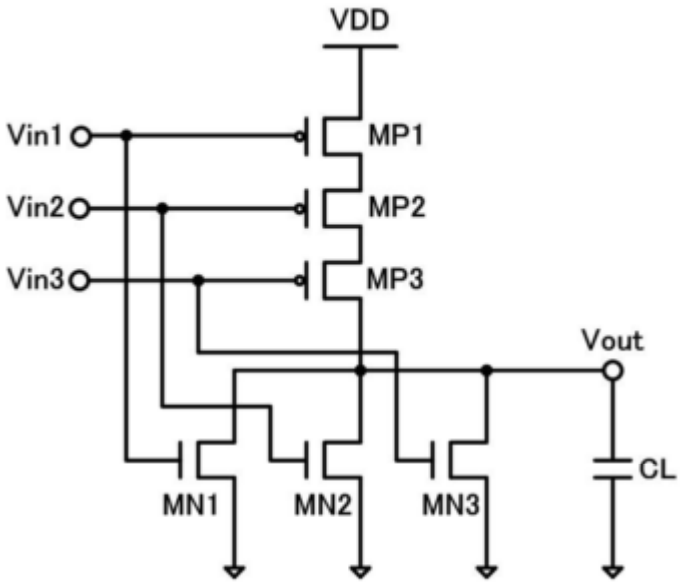

Figure 4.1 3-input NOR gate.

With the popularity of nanometer technologies in digital LSI, the overshooting effect is much more obvious and researchers begin to model this effect in detail. In recent research publications [3][4][47], only the overshooting effect of an inverter is analyzed. However, the overshooting effect of multiple-input gates is still obvious and has great influence to gate delay as an inverter. For example, a 3-input NOR gate is shown in Fig. 4.1 and a falling signal is connected to one of the three inputs. The falling signal is defined as

$$V_{in} = \begin{cases} V_{DD}: t \le 0 \\ \left(1 - \frac{t}{t_{in}}\right) V_{DD}: 0 < t \le t_{in} \\ 0: t > t_{in} \end{cases} \quad (1)$$

where V_{DD} is the supply voltage and tin is the input signal transition time. The output waveform is shown in Fig. 4.2 and the gate delay is expressed as

$$t_D = t_{50} - \frac{t_{in}}{2} \quad (4.2)$$

where t_{50} is the time period for the output voltage to reach 50% of the supply voltage. The time period t_{50} is composed of two parts and expressed as

$$t_{50} = t_{ov} + t_{rise} \quad (4.3)$$

where t_{ov} is the overshooting time and t_{rise} is the time period for the output voltage to reach 50% of the supply voltage from $t = t_{ov}$.

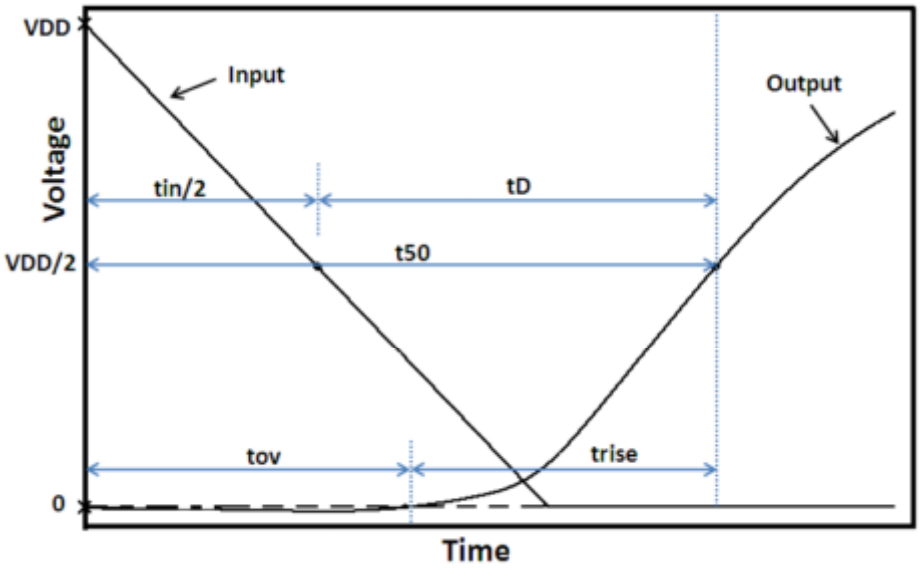

Figure 4.2 Output waveform of 3-input gate.

In a nanometer regime, the overshooting time of multiple-input gates becomes a great component of the gate delay. As shown in Sect. 2.2, the overshooting time contributes greatly to the gate delay of multiple-input gates. Thus, modeling the overshooting effect of multiple-input gates accurately will be helpful for the analysis of gate delay.

In traditional gate delay and power consumption models for multiple-input gates,

the method of simplifying the multiple-input gate to an inverter is commonly used [56]-[58]. However, these simple reduction methods will cause large error while modeling the overshooting effect of multiple-input gates. Furthermore, the conventional models of the overshooting effect for an inverter [3][4][47] are not easily extended to calculate the overshooting time of multiple-input gates.

In our previous research [55], a simple method with a proportional coefficient is proposed to calculate the overshooting time of 2-input NOR gate, which is based on the model in [3]. However, limitations still exist in [55]. Firstly, the proportional coefficient needs to be extracted every time when process technology varies which is not convenient for practical application. Secondly, the accuracy will decrease much when the input signal transition time decreases for 2-input gates. Thirdly, the error will increase further for the multiple-input gates with more than two inputs. As discussed in Section 4, the error can be 18.15% for the 3-input gate and 24.75% for 4-input gate when the method in [55] is used to estimate the overshooting time. Meanwhile, the errors of the proposed model are only 2.38% and 1.98%, respectively.

Table 4.1 shows the proportional coefficient of t_{ov1}/t_{ov3} for different input conditions. t_{ov1} is the overshooting time of 3-input NOR gate in Fig. 4.1 when the input V_{in1} is switched, and t_{ov3} is the overshooting time when V_{in3} is switched. It is demonstrated from Table 4.1 that the proportional coefficient of 3-input NOR gate for different input conditions varies significantly. Thus, the method using a constant proportional coefficient in [55] is not available for modeling the overshooting effect for multiple-input gates with more than two inputs.

Based on the descriptions before, it can be concluded that the overshooting effect of multiple-input gates should be specially modeled in a nanometer regime. In this paper, an effective model of the overshooting effect for multiple-input gates in nanometer technologies is proposed. The main contributions of the proposed model in this chapter are shown as:

Table 4.1 The ratio of t_{ov1}/t_{ov3} for 3-input NOR gate.

	$L_n = L_p = 40nm$ $W_p/W_n = 0.16um/0.08um$ $C_L = 1fF$	$L_n = L_p = 40nm$ $W_p/W_n = 1.2um/0.6um$ $C_L = 0.1fF$
$t_{in}(ps)$	t_{ov1}/t_{ov3}	t_{ov1}/t_{ov3}
20	1.33	1.35
40	1.36	1.47
60	1.39	1.49
80	1.41	1.50
100	1.42	1.48
120	1.43	1.46

1. An formula-based model is proposed for 2-input CMOS gates, which is useful for further analysis of the overshooting time and gate delay.

2. The extension methods are proposed to calculate the overshooting time of other multiple-input gates in this paper.

3. The proposed models are verified within 3.4% error compared with SPICE simulation results using CMOS 32nm PTM model [43].

4. The application of the proposed model is discussed to predicting the CMOS delay and improve the Thevenin model for the CMOS gate driving interconnect loads.

4.3 Proposed model

In this section, the expressions of the overshooting time for 2-input NOR gate is presented firstly. Based on the proposed model for 2-input NOR gate, the method to calculate the overshooting time of 3-input NOR gate is given subsequently. Meanwhile, we also analyzed how to extend the proposed model to other multiple-input gates.

4.3.1 Modeling the Overshooting Effect of 2-input NOR Gate

The 2-input gate is one of the most simple multiple-input gates. In this subsection, expressions of the overshooting time for 2-input NOR gate shown in Fig. 4.3 is proposed. In Fig. 4.3, the gates of MN1 and MP1 are connected to the input terminal V_{in1}, while the gates of MN2 and MP2 are connected to the other input terminal V_{in2}. Similarly, each transistor of other multiple-input gates is denoted MNi or MPi whose gate is connected to the i-th input terminal in this paper. In order to simplify the analysis of modeling the overshooting effect for 2-input NOR gate in Fig. 4.3, two different input conditions are considered. One input condition is that a falling signal in Eq. (4.1) is applied to V_{in1} and V_{in2} is directly connected to the ground. The other input condition is that the same falling signal is connected to V_{in2} and $V_{in1} = 0$. Meanwhile, the similar expressions can be obtained if the falling signal is replaced by a rising signal. In Fig. 4.3, the capacitances Cgd1, Cgd2, Cgd3, Cgd4 and Cgs4 are all input-to-output coupling capacitances.

The expression of the overshooting time for an inverter has been proposed in [2] which is expressed as

$$t_{ov} = t_{vmin} - t_{\gamma} + \sqrt{\frac{2Q_1}{I_{D0}}(t_{in} - t_{TPL}) + t_{\gamma}^2} \tag{4.4}$$

where t_{vmin} is the time when the output voltage is at its minimum, t_{γ} is an intermediate parameter which is given later, Q_1 is the charge flowing out of load capacitance, I_{D0} is the drain current in saturation at $V_{GS} = V_{DS} = V_{DD}$ for the

PMOS, $t_{TPL} = \frac{|V_{TPL}|}{V_{DD}} t_{in}$ and V_{TPL} is the equivalent threshold voltage which is extracted from α-power approximation [25] for PMOS transistor drain current.

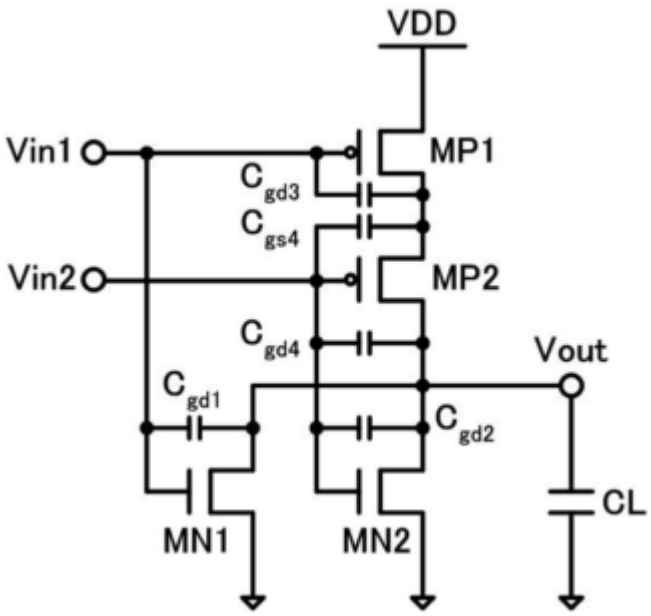

Figure 4.3 2-input NOR gate considering input-to-output coupling capacitances

The equation (4.4) is verified still being effective to calculate the overshooting time of 2-input NOR gate in Fig. 4.3. When $V_{in2} = 0$ and V_{in1} is connected to the falling signal, the transistor MN2 is cut off and 2-input NOR gate is simplified as shown in Fig. 4.4

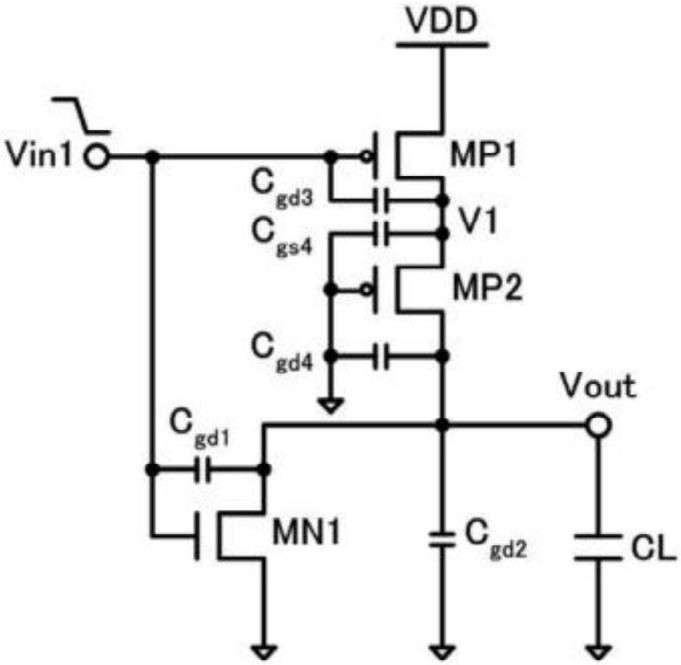

Figure 4.4 2-input NOR gate when V_{in1} is switched.

The intermediate parameter in this condition is expressed as

$$t_{\gamma 1} = \frac{1}{2}\left[t_{vmin} - t_{TPL} - (C_{gd1} + 0.5C_{gs4} + 1.5C_{gd3})\frac{V_{DD}}{I_{D0}}\frac{t_{in}-t_{TPL}}{t_{in}}\right]. \tag{4.5}$$

Since the derivation of parameters in Eqs. (4.4) and (4.5) is very long, it is shown in the Appendix A. In Fig. 4.4, the node between MP1 and MP2 is identified as V_1. Compared with an inverter, the value of V_1 as well as the coupling capacitances will be specially considered in the Appendix A.

When $V_{in1} = 0$ and V_{in2} is connected to the falling signal, MN1 always cuts off and MP1 operates almost in the triode region during the overshooting period. Therefore, the drain current of MN1 is almost zero and MP1 can be regarded as a resistance. Thus, the 2-input NOR gate in Fig. 4.3 can be simplified as shown in Fig. 4.5 which is almost similar as an inverter. The derivation method in the Appendix A is still useful for this condition and the intermediate parameter can be expressed as

$$t_{\gamma 2} = \frac{1}{2}\left[t_{vmin} - t_{TPL} - (C_{gd2} + C_{gd4})\frac{V_{DD}}{I_{D0}}\frac{t_{in}-t_{TPL}}{t_{in}}\right]. \tag{4.6}$$

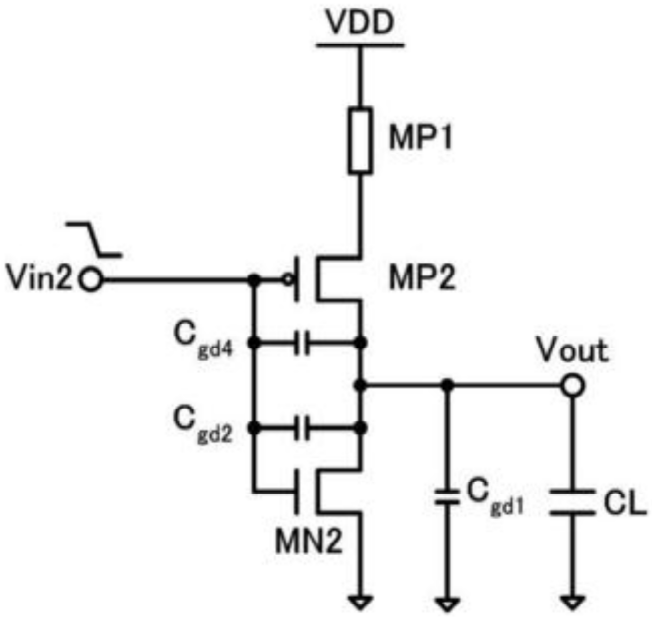

Figure 4.5 2-input NOR gate when V_{in2} is switched.

After obtaining the expressions of intermediate parameters for 2-input NOR gate under two input conditions, the initial overshooting times can be calculated using Eq. (4.4). However, the second step calculation is needed to improve the accuracy as explained in [3].

4.3.2 Modeling the Overshooting Effect of 3-Input NOR Gate

Modeling the overshooting effect of 3-input NOR gate is more complicated than 2-input NOR gate. In this subsection, the method to model the overshooting effect of 3-input NOR gate is proposed. The analysis is composed of three parts according to three different input conditions.

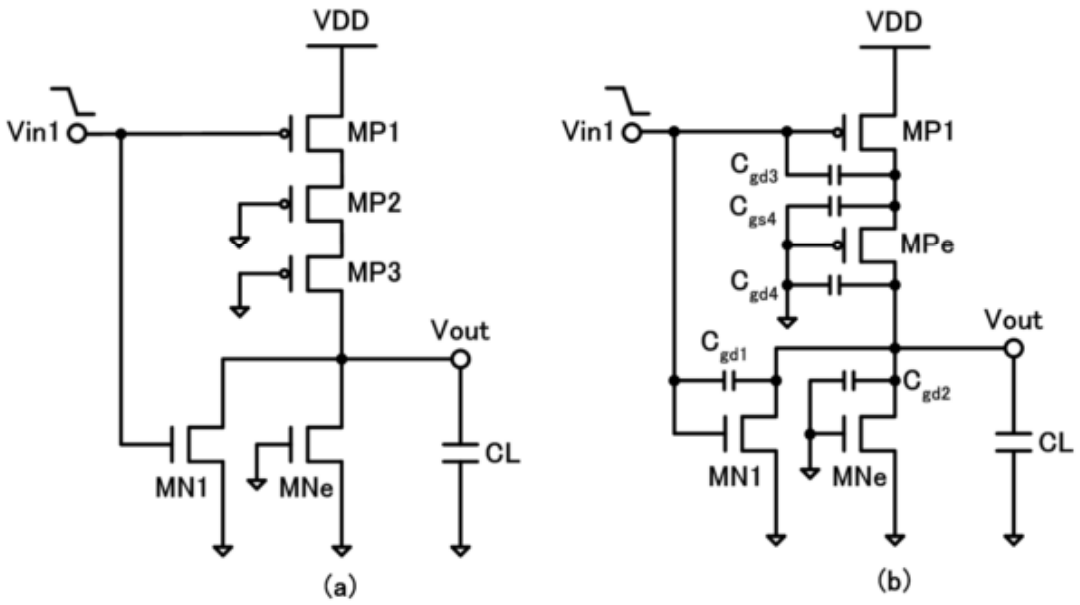

Figure 4.6 Simplified 3-input NOR gate when V_{in1} is switched.

A) Vin1 Switching

When V_{in1} is switched and connected to a falling signal, V_{in2} and V_{in3} are connected to the ground simultaneously. Then MN2 and MN3 are always cut off which are merged to an equivalent transistor MNe. The size of MNe is $L_{MNe} = L_{MN2} = L_{MN3}$ and $W_{MNe} = 2W_{MN2} = 2W_{MN3}$. The 3-input NOR gate is transferred to a circuit as shown in Fig. 4.6 (a). In order to simplify the circuit in Fig. 4.6 (a) further, MP2 and MP3 are also merged to an equivalent transistor MPe. The size of MPe is assumed as $L_{MPe} = 2L_{MP2} = 2L_{MP3}$ and $W_{MPe} = W_{MP2} = W_{MP3}$. After merging transistors with the same inputs simply, the 3-input NOR gate in Fig. 6 (a) is transferred to a 2-input NOR gate as shown in Fig. 4.6 (b). The capacitances Cgd1, Cgd2, Cgd3, Cgd4 and Cgs4 are all input-to-output coupling capacitances in Fig. 4.6 (b).

Figure 4.7 shows the overshooting times of the 3-input NOR gate and simplified 3-input NOR gate when V_{in1} is switched. Here, t_{ov} and t_{ove} are the overshooting times of 3-input NOR gate in Fig. 4.6 (a) and the simplified circuit in Fig. 4.6 (b), respectively. It can be seen that t_{ov} increases almost linearly with t_{ove} rises. Thus, it can be expressed as

$$t_{ov} \propto t_{ove}. \tag{4.7}$$

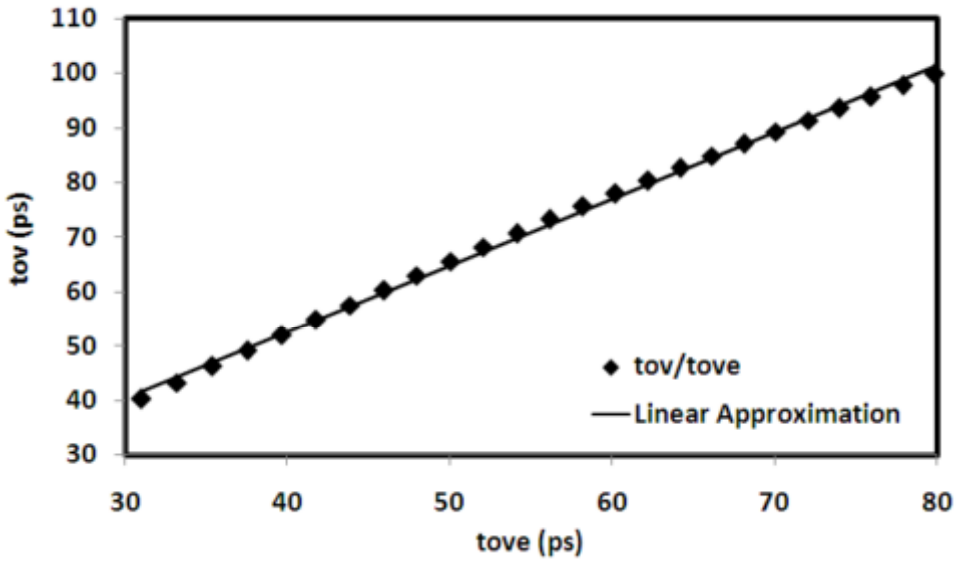

Figure 4.7 The overshooting times of the 3-input NOR gate and simplified 3-input NOR gate when V_{in1} is switched.

Through a number of verification works under different conditions, it is demonstrated that the overshooting time of 3-input NOR gate in Fig. 4.6 (a) can be empirically expressed as

$$t_{ov} \approx t_{ove} \times \frac{t_{ove}}{t_{vmine}} \quad , \tag{4.8}$$

where t_{vmine} is the minimum output voltage of the simplified circuit in Fig. 7 (b). Table 2 shows the verification results for Eq. (4.8) with different conditions. The maximum error of the simulation results in Table 2 is 2.1%. Therefore, the overshooting time of 3-input NOR gate when V_{in1} switched can be obtained using Eq. (4.8). Besides, the parameters t_{ove} and t_{vmine} for the simplified circuit in Fig. 7 (b) can be obtained using the expressions for 2-input NOR gate of Fig. 4.4 proposed in Sect. 3.1 easily. However, the values of the coupling capacitances in Fig. 4.6 (b) are different from the 2-inputNOR gate in Fig. 4.4 due to transistor merging.

Table 2 Verification works of the equation (4.8).

	$W_p/W_n(um)$	$t_{ov}(ps)$	$t_{ove}^2/t_{vmine}(ps)$
$L_n = L_p = 40nm$ $t_{in} = 60ps$ $C_L = 0.1fF$	0.2/0.1	51.4	50.7
	0.4/0.2	51.5	50.4
	0.8/0.4	51.5	50.7
	1.6/0.8	51.2	50.3
	3.2/1.6	50.8	50.2
	$t_{in}(ps)$	$t_{ov}(ps)$	$t_{ove}^2/t_{vmine}(ps)$
$L_n = L_p = 40nm$ $W_p/W_n = 0.8um/0.4um$ $C_L = 0.5fF$	40	40.1	41.2
	80	62.9	62
	120	82.3	82.4
	160	99.4	101.2
	200	115.9	117.3
	$C_L(fF)$	$t_{ov}(ps)$	$t_{ove}^2/t_{vmine}(ps)$
$L_n = L_p = 40nm$ $W_p/W_n = 1.2um/0.6um$ $t_{in} = 80ps$	0.1	62.1	61
	0.3	62.3	61.4
	0.5	62.5	61.7
	0.7	62.7	61.9
	0.9	62.9	62.3

B) Vin2 Switching

When V_{in2} is connected to a falling signal, V_{in1} and V_{in3} are connected to the ground. Because MN1 and MN3 are always cut off, they can be merged to an equivalent transistor MNe. The transistor size is $L_{MNe} = L_{MN1} = L_{MN3}$ and $W_{MNe} = 2W_{MN1} = 2W_{MN3}$. Then the 3-input NOR gate can be simplified to a circuit as shown in Fig. 4.8 (a). The node between MP1 and MP2 is identified as 1. During the overshooting period, MP1 always works on the triode region. There is a small voltage drop away from V_{DD} in node 1.

Without considering the effect of MP1, the 3-input NOR gate in Fig. 4.8 (a) can be

simplified to a simple 2-input NOR gate as shown in Fig. 4.8 (b). The capacitances C_{gd1}, C_{gd2}, C_{gd3}, C_{gd4} and C_{gs4} are all input-to-output coupling capacitances. Due to the existence of voltage drop in node 1, the overshooting time of 2-input NOR gate in Fig. 4.8 (b) is a little away from the overshooting time of 3-input NOR gate in Fig. 4.8 (a). Therefore, a method with three steps is proposed to obtain the accurate overshooting time of 3-input NOR gate in Fig. 4.8 (a).

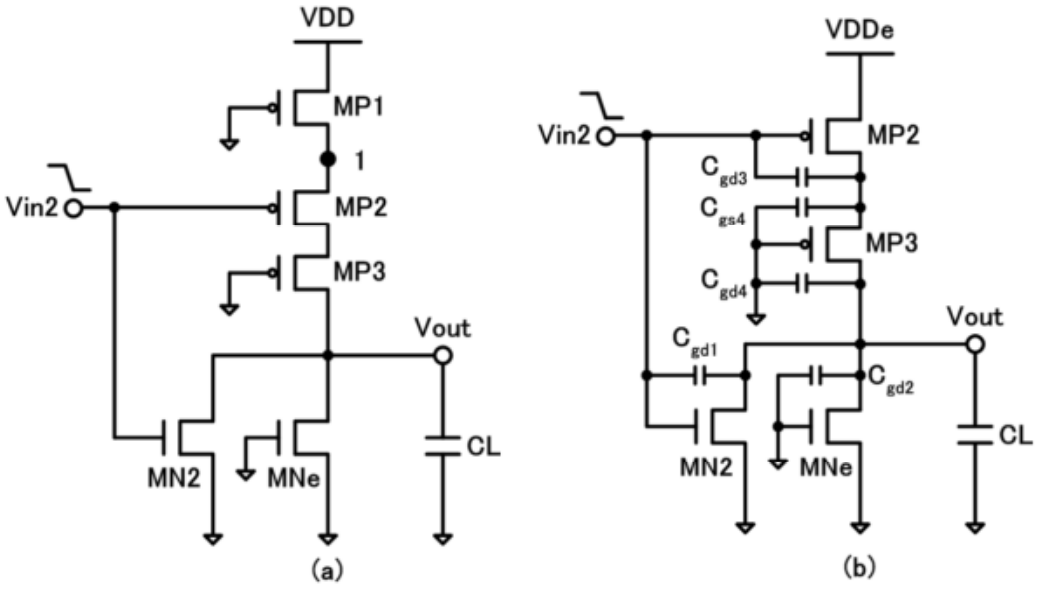

Figure 4.8 Simplified 3-input NOR gate when V_{in2} is switched.

Step 1: Calculate the overshooting time of 2-input NOR gate in Fig. 4.8 (b) with the condition $V_{DDe} = V_{DD}$ and the result is marked as t_{ov0}.

Step 2: Obtain the voltage of node 1 $V_1(t_{ov0})$ at $t = t_{ov0}$ for 3-input NOR gate in Fig. 4.8 (a).

Step 3: Calculate the overshooting time of 2-input NOR gate in Fig. 4.8 (b) again with the condition $V_{DDe} = V_1(t_{ov0})$ and the result is marked as t_{ov}.

Through these three steps, the final result tov is almost the same as the overshooting time of 3-input NOR gate in Fig. 4.8 (a). In Steps 1 and 3, the overshooting time calculation for 2-input NOR gate in Fig. 4.8 (b) is same as the proposed method for 2-input NOR gate in Fig. 3.4. Due to transistor merging, the coupling capacitances in Fig. 4.8 (b) are different from 2-input NOR gate in Fig. 4.4

which needs to be extracted. Moreover, the parameter $V_1(t_{ov0})$ in Step 2 should be considered specially. The voltage waveform of the node 1 for the 3-input NOR gate in Fig. 4.8 (a) is shown in Fig. 4.9.

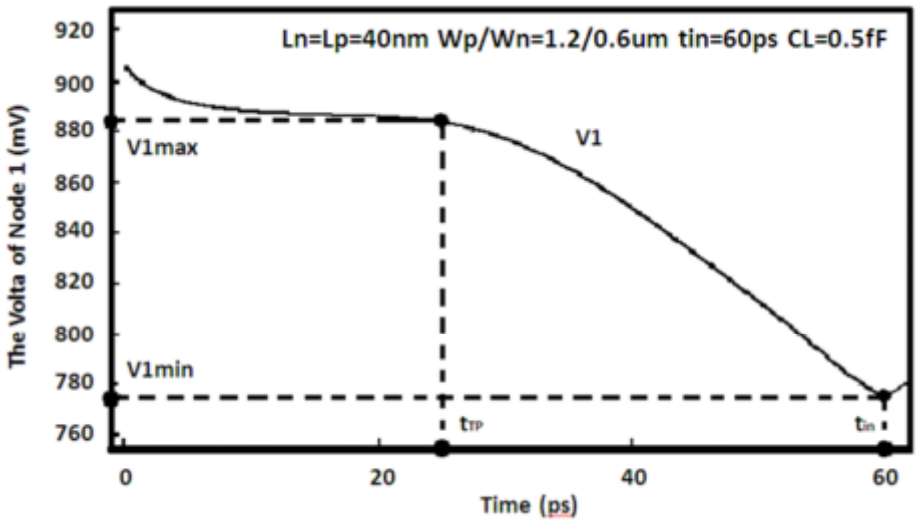

Figure 4.9 The voltage of node 1 versus different input signal transition times.

From the time $t = t_{TP}$ to the time $t = t_{in}$, the voltage of node 1 will decrease almost linearly. t_{TP} is the time when MP2 is switched on and $t_{TP} \approx t_{in}|V_{thP}|/V_{DD}$, where V_{thP} is the threshold voltage of MP2. In Fig. 10, the voltage of the node 1 at $t = t_{TP}$ is defined as V_{1max} and the voltage of node 1 at $t = t_{in}$ is defined as V_{1min}. Therefore, the value of $V_1(t_{ov0})$ can be approximately expressed as

$$V_1(t_{ov0}) = \frac{V_{1min}-V_{1max}}{t_{in}-t_{TP}} t_{ov0} + \left(V_{1min} - \frac{V_{1min}-V_{1max}}{1-t_{TP}/t_{in}}\right) . \quad (4.9)$$

For a specific CMOS technology, the parameters V_{1min} and V_{1max} almost remain constant with the change of transistor sizes and load capacitances. The value of V_{1min} and V_{1max} will become a little larger with the increase of input signal transition time. Through various verifications, we find that V_{1min} and V_{1max} can be regarded as constant value approximately and this approximation will not affect the accuracy of further calculation. In Table 3, the value of V_{1min} and V_{1max} versus different transistor sizes, load capacitances and input signal transition times are shown using CMOS 32nm PTM model. Except the results shown in Table 3, other verifications are done and the values of V_{1min} and V_{1max} for CMOS 32nm PTM model are finally

determined. In the proposed model, V_{1min} equals to 0.78V and V_{1max} is assumed as 0.88V for CMOS 32nm PTM model.

Table 3 V_{1min} and V_{1max} under different conditions

	W_p/W_n(um)	V_{1min}(V)	V_{1max}(V)
$L_n = L_p = 40nm$ $t_{in} = 60ps$ $C_L = 0.5fF$	0.2/0.1	0.777	0.884
	0.4/0.2	0.777	0.884
	0.8/0.4	0.777	0.884
	1.6/0.8	0.777	0.884
	3.2/1.6	0.777	0.884
	t_{in}(ps)	V_{1min}(V)	V_{1max}(V)
$L_n = L_p = 40nm$ $W_p/W_n = 1.2um/0.6um$ $C_L = 1fF$	40	0.762	0.878
	60	0.777	0.884
	80	0.787	0.887
	100	0.794	0.889
	120	0.796	0.890
	C_L(fF)	V_{1min}(V)	V_{1max}(V)
$L_n = L_p = 40nm$ $W_p/W_n = 2.4um/1.2um$ $t_{in} = 60ps$	0.1	0.778	0.884
	0.3	0.777	0.884
	0.5	0.777	0.884
	0.7	0.777	0.884
	0.9	0.777	0.884

To sum up, when V_{in2} of 3-input NOR gate is switched, the overshooting time is calculated through three steps based on the proposed model for 2-input NOR gate as shown in Fig. 3.4 of Sect. 3.1.

C) Vin3 Switching

In this part, the situation when V_{in3} switched is analyzed. The input V_{in3} in Fig.

4.1 is connected to the falling signal and the other two inputs are connected to the ground. Then MP1 and MP2 work in the triode region during the overshooting period. MN1 and MN2 always cut off. Therefore, MP1 and MP2 can be merged to an equivalent PMOS transistor MPe. The width of MPe is the same as MP1 and MP2. The length of MPe is two times of MP1 and MP2 [56]. MN1 and MN2 can also be merged to an equivalent NMOS transistor MNe. The length of MNe is the same as MN1 and MN2, while the width of MNe is two times of MN1 and MN2. Thus, the 3-input NOR gate is simplified as shown in Fig. 3.10 where the capacitances C_{gd1}, C_{gd2} and C_{gd4} are all input-to-output coupling capacitances. The calculation of this condition is absolutely same as the 2-input NOR gate when V_{in2} switched which is shown in Fig. 4.5. The only difference is the values of coupling capacitances due to transistor merging. Therefore, the model in Sect. 3.1 can be used to calculate the overshooting time directly.

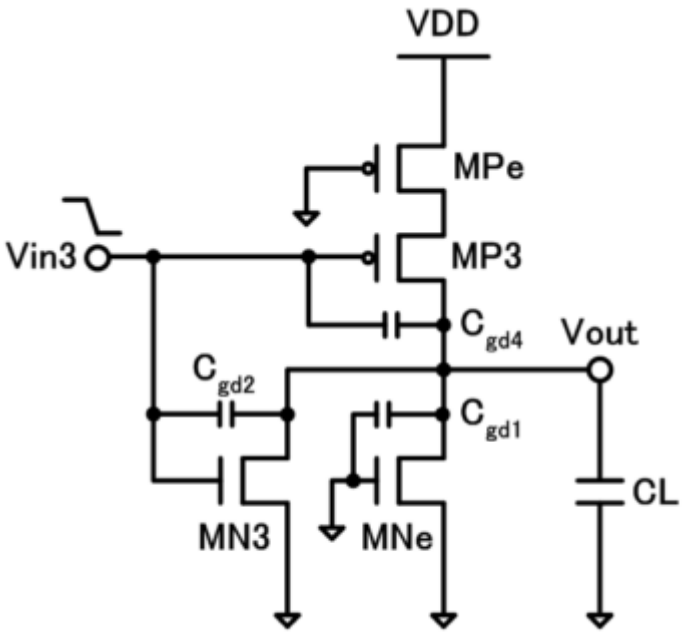

Figure 4.10 Simplified 3-input NOR gate when V_{in3} is switched.

In conclusion, the overshooting time of 3-input NOR gate is calculated using three different methods according to the switching conditions of inputs. When V_{in1} is switched, the overshooting time of 3-input NOR gate can be calculated using the parameters of 2-input NOR gate shown in Fig. 4.4 of Sect. 4.3.1. WhenV_{in2} is

switched, the supply voltage V_{DD} is changed to obtain final accurate value where the proposed model for 2-input NOR gate in Fig. 3.4 of Sect. 4.3.1 is also used. When V_{in3} is switched, the 3-input NOR gate is simplified to 2-input NOR gate and the calculation method is absolutely same as the overshooting time calculation method for 2-input NOR gate in Fig. 4.5 of Sect. 4.3.1.

4.3.3 Extension to Other Multiple-Input Gates

In Sect. 4.3.1, expressions of the overshooting time for 2-input NOR gate is proposed. Based on the 2-input NOR gate model, the overshooting time of 3-input NOR gate is calculated in detail in Sect. 4.3.2. These proposed models can also be extended to many other multiple-input gates.

For 2-input NAND gate as shown in Fig. 4.11, the overshooting time can be obtained using the similar method as 2-input NOR gate. In Fig. 4.11, the capacitances C_{gd1}, C_{gd2}, C_{gd3}, C_{gd4} and C_{gs1} are all input-to-output coupling capacitances. The Equation (3.4) can still be used to calculate the overshooting time of 2-input NAND gate. Meanwhile, the derivation method explained in the Appendix A to obtain the parameters of Eq. (3.4) is also useful for 2-input NAND gate.

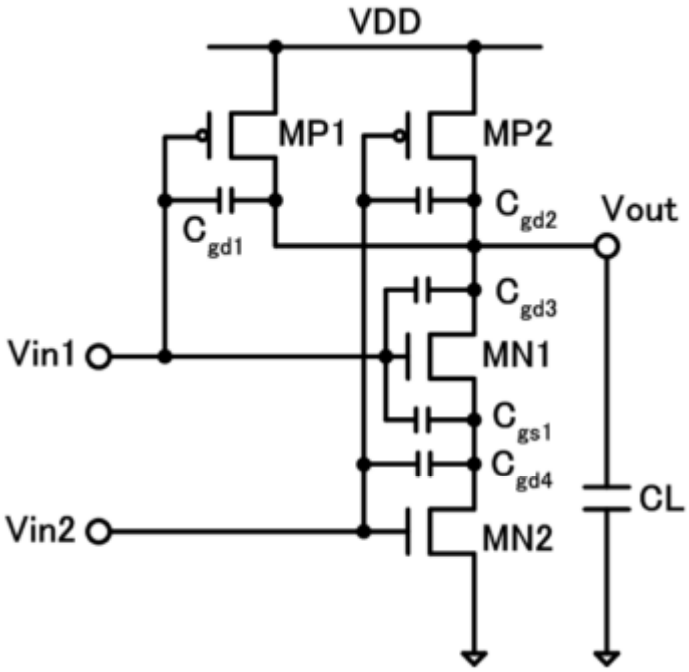

Figure 4.11 2-input NAND gate considering input-to-output coupling

capacitances.

After obtaining the overshooting time expressions for 2-input NAND gate, 3-input NAND gate shown in Fig. 4.12 is tried to be simplified.

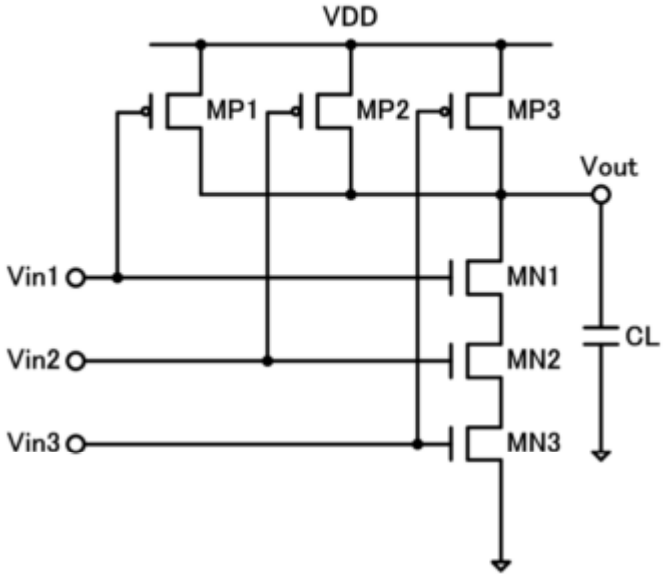

Figure 4.12 3-input NAND gate.

When only V_{in1} is switched, V_{in1} is connected to a falling signal, V_{in2} and V_{in3} are connected to V_{DD}. MP2 and MP3 are always cut off which are merged to an equivalent transistor with the size $L_{MPe} = L_{MP2} = L_{MP3}$ and $W_{MPe} = 2W_{MP2} = 2W_{MP3}$. MN2 and MN3 are merged to an equivalent transistor with the size $L_{MNe} = 2L_{MN2} = 2L_{MN3}$ and $W_{MNe} = W_{MN2} = W_{MN3}$. The simplified circuit is shown in Fig. 13 (a). In Fig. 13 (a), the capacitances C_{gd1}, C_{gd2}, C_{gd3}, C_{gd4} and C_{gs1} are all input-to-output coupling capacitances. In this way, the simplified circuit is almost same as a 2-input NAND gate and expressions of the overshooting time for primitive 2-input NAND gate in Fig. 4.11 can be applied directly. However, only the value of input-to-output coupling capacitances in Fig. 13 (a) needs to be extracted due to transistor size change compared with primitive 2-input NAND gate in Fig. 4.11.

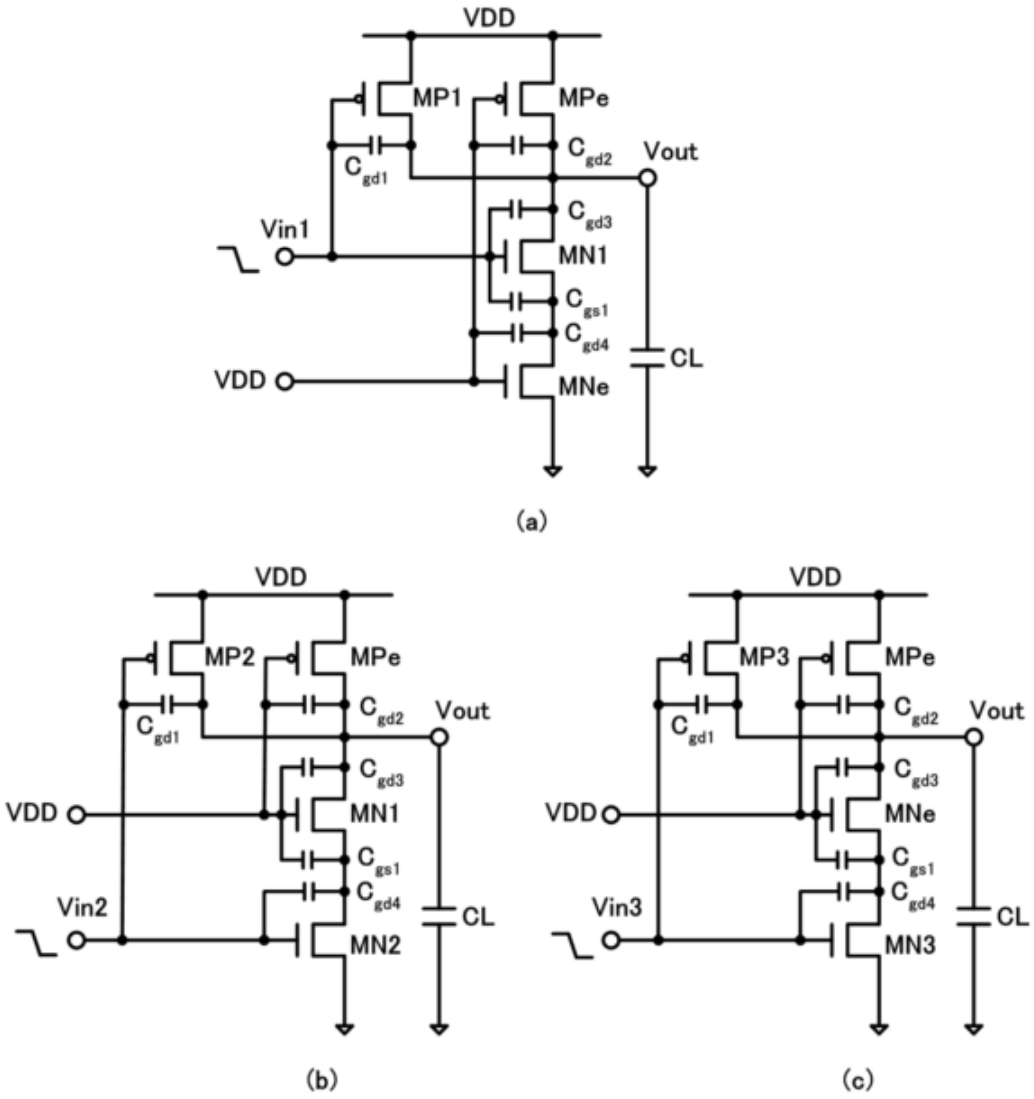

Figure 4.13 3-input NAND gate under different switching conditions.

When V_{in2} is switched, the transistors with the same inputs are merged to an equivalent transistor and the transistor MN3 is omitted in order to simplify the gate. Then, the 3input NAND gate is transferred to a 2-input NAND gate as shown in Fig. 13 (b) where the coupling capacitances are considered. According to various verifications, it is found that the simplified circuit in Fig. 13 (b) can accurately represent the overshooting time of 3-input NAND gate when V_{in2} is switched. Similarly, when V_{in3} is switched, the 3-input NAND gate can also be simplified to a 2-input NAND gate as shown in Fig. 4.13 (c) after merging the transistors with the same inputs. After the merge operations, the overshooting times of NAND gates in

Fig. 4.13 (b) and Fig. 4.13 (c) can be calculated using the overshooting time expressions for 2-input NAND gates conveniently and only the values of coupling capacitances need to be changed due to the merge operations.

Although 2-input and 3-input gate is analyzed in the proposed models, multiple-input gates with more than three inputs can still use the proposed model. For example, the calculation methods to obtain the overshooting time of 4-input NOR gate can be easily presented, based on the proposed models. In Fig. 4.14, a 4-input NOR gate is shown.

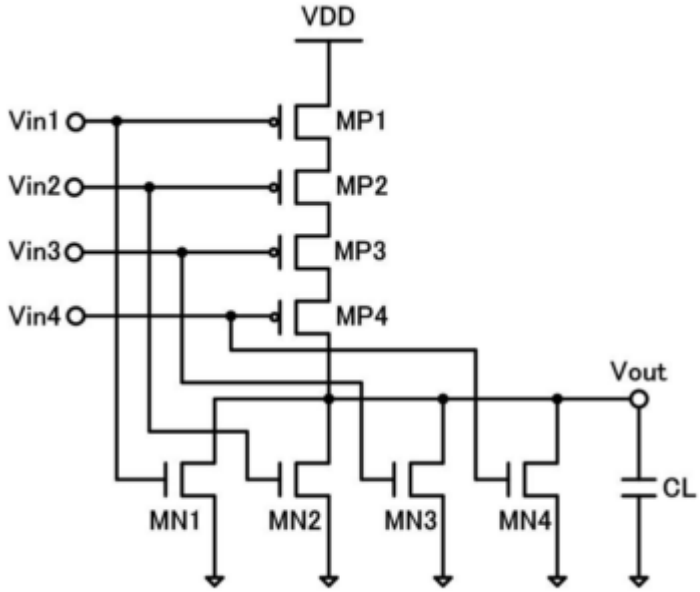

Figure 4.14 4-input NOR gate.

When V_{in1} is switched, MP2, MP3 and MP4 are merged to an equivalent transistor MPe, whereas MN2, MN3 and MN4 are merged to an equivalent transistor MNe. The transistor size of MPe is $L_{MPe} = 3L_{MP2} = 3L_{MP3} = 3L_{MP4}$ and $W_{MPe} = W_{MP2} = W_{MP3} = W_{MP4}$. The size of MNe is $L_{MNe} = L_{MN2} = L_{MN3} = L_{MN4}$ and $W_{MNe} = 3W_{MN2} = 3W_{MN3} = 3W_{MN4}$. After the merge operation, the 4-input NOR gate is transferred to a similar 2-input NOR gate as shown in Fig. 4.15 (a) where the coupling capacitances are considered. And then the overshooting time calculation is absolutely same as the proposed method in Sect. 3.2.1 where Eq. (4.8) is used to obtain the final overshooting time. When the equation (4.8) is applied to this condition, t_{ove} and t_{vmine} are the parameters of 2-input NOR gate in Fig. 4.15 (a) which need to be

extracted. The values of these two parameters can be calculated using the proposed model for 2-input NOR gate in Fig. 4.4 of Sect. 4.3.1.

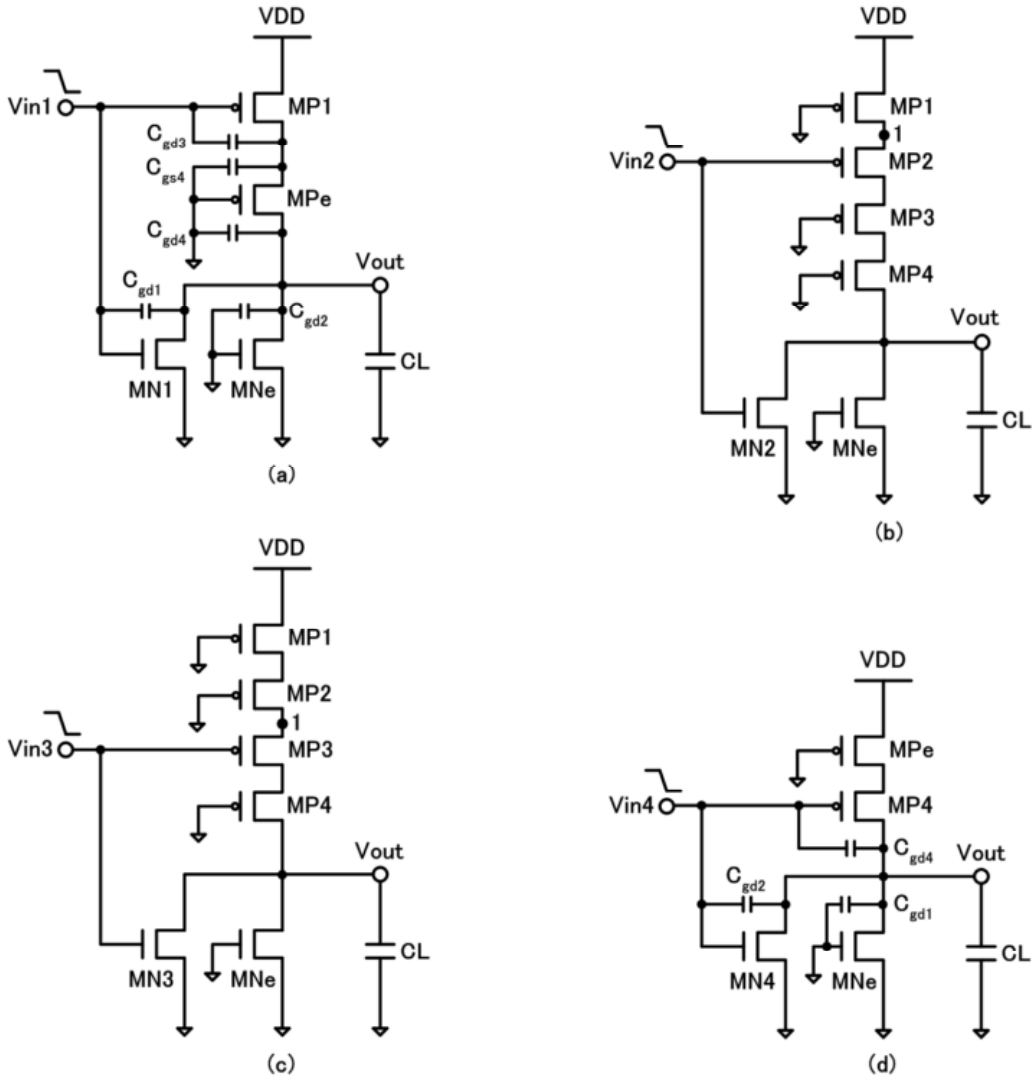

Figure 4.15 4-input NOR gate under different switching conditions.

When V_{in2} is switched, the 4-input NOR gate is transferred to a simple circuit after merging the NMOS transistor with the same inputs as shown in Fig. 4.15 (b). According to various verifications, the proposed model in Sect. 4.3.2 B) as well as the model in Sect. 4.3.2 A) can be used together to calculate the overshooting time of Fig. 4.15 (b). In Sect. 4.3.2 B), the gate in Fig. 4.8 (a) can be regarded as the primitive gate and the gate in Fig. 4.8 (b) can be regarded as the simplified gate. For the condition when V_{in2} of 4-input NOR gate is switched, the gate in Fig. 4.15 (b) is regarded as

the primitive gate and the gate in Fig. 4.15 (b) after omitting MP1 is regarded as the simplified gate. Then three steps proposed in Sect. 4.3.2 B) can be applied similarly to calculate the overshooting time of the gate in Fig. 4.15 (b). The only difference is about calculating the overshooting time for the simplified gate in Step 1 and Step 3. In Sect. 4.3.2 B), the simplified gate shown in Fig. 4.8 (b) is similar as a 2-input NOR gate while the simplified gate of Fig. 4.15 (b) is similar as a 3-input NOR gate which is same as the gate shown in Fig. 4.6 (a). Therefore, when calculating the overshooting time of the simplified gate of Fig. 4.15 (b), the proposed model in S Sect. 4.3.2 A) will be directly used. Finally, when calculating the overshooting time of the gate in Fig. 4.15 (b), the parameters which need to be extracted are same as the parameters used in Sect. 4.3.2 A) and Sect. 4.3.2 B) except changing some values of coupling capacitances due to merge operations.

When V_{in3} is switched, the 4-input NOR gate can be transferred to the circuit shown in Fig. 4.15 (c). In this condition whenVin3 is switched for 4-input NOR gate, the gate in Fig. 4.15 (c) can be regarded as the primitive gate which is similar as the gate in Fig. 9 (a) and the gate in Fig. 16 (c) after omitting the transistors MP1 and MP2 can be regarded as the simplified gate which is same as the gate in Fig. 4.8 (b). Then the proposed model in Sect. 4.3.2 B) is verified to be able to calculate the overshooting time of the gate in Fig. 4.15 (c) accurately. The parameters need to be extracted are also same as the parameters used in Sect. 4.3.2 B) and the value of some coupling capacitances used in Sect. 4.3.2 B) need to be changed because of the merge operation in Fig. 4.15 (c).

When V_{in4} is switched, the 4-input NOR gate is simplified to the circuit as shown in Fig. 4.15 (d) after merging the transistors with the same inputs. The calculation method is the same as the proposed model in Sect. 4.3.2 C) and the parameters need to be used are also same as the model in Sect. 4.3.2 C) while the value of some coupling capacitances need to be changed due to merge operation.

The proposed models in Sects. 4.3.1 and 4.3.2 are effective not only for NOR and NAND gate, they are still useful when applied to some other complex multiple-input gates. For example, the AOI12 gate [60] shown in Fig. 4.16 still has overshooting effect and needs a model to calculate the overshooting time.

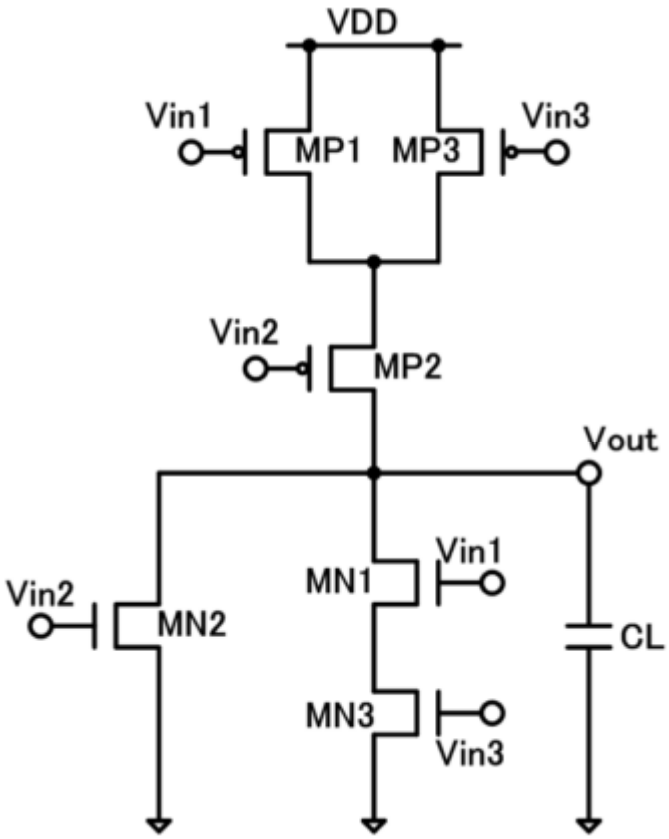

Figure 4.16 AOI12 gate.

When V_{in2} is connected to the falling signal, V_{in1} and V_{in3} are connected to the ground, the AOI12 can be simplified to a circuit as shown in Fig. 4.17 (a) after merging transistors with same inputs where the coupling capacitances are considered. The simplified circuit in Fig. 4.17 (a) is almost same as a 2-input NOR gate. Therefore, the proposed model for 2-input NOR gate in Fig. 4.5 of Sect. 4.3.1 can be directly used to calculate the overshooting time of the circuit in Fig. 4.16 (a).

When V_{in2} is connected to the falling signal, V_{in1} is connected to the ground and V_{in3} is connected to V_{DD}, MP3 and MN1 are always cut off. The AOI12 gate is simplified to the circuit as shown in Fig. 4.17 (b). This simplified circuit is also almost same as 2-input NOR gate shown in Fig. 4.5. Thus, the final overshooting time can be obtained using the method in Sect. 4.3.1.

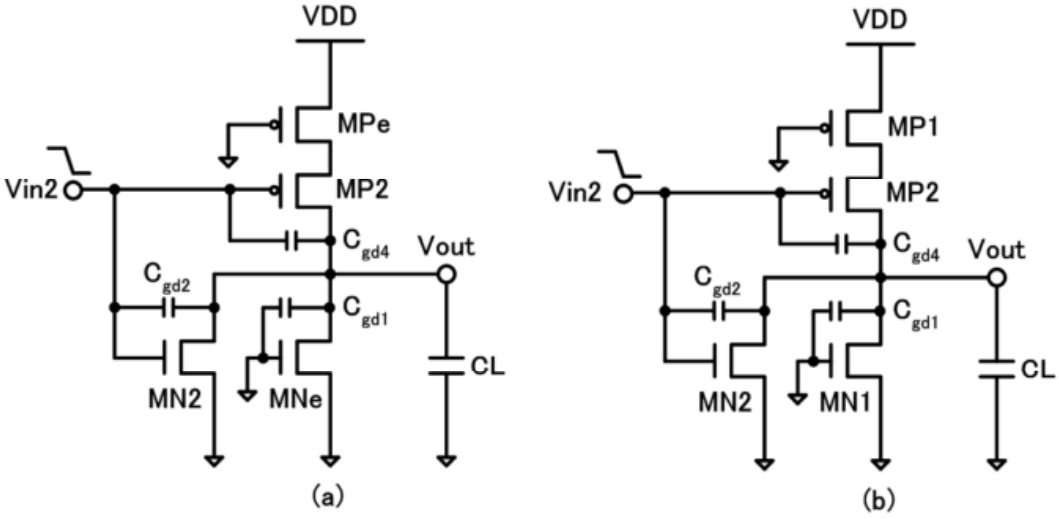

Figure 4.17 AOI12 gate under different switching conditions.

In summary, the proposed model in Sects. 4.3.1 and 4.3.2 can be applied to calculate the overshooting time of multiple-input gates effectively and conveniently. When extending the proposed models to other multiple-input gates, the basic principle is similar to the method proposed in Sects. 4.3.1 and 4.3.2. Firstly, the overshooting time expressions for 2-input gate is obtained using the method proposed in Sect. 4.3.1. Secondly, for the multiple-input gate with more than two inputs, it is simplified to the circuit with less inputs. The main idea of simplifying the gate is to merge inactive transistors in serial/parallel connection to generate more simple circuit whose overshooting time can be calculated using the proposed formula-based model for 2-input gate in Sect. 4.3.1 or the model in Sect. 4.3.2. The only difference is that the coupling capacitances need to be changed due to some merge operations.

4.4 Experimental Results

In this section, simulation results of different multiple-input gates obtained from the proposed model will be shown. In order to verify the accuracy of the proposed model completely, the simulations will include the consideration of different input signal transition times, transistor sizes and load capacitances using CMOS 32nm PTM model [43].

Firstly, the simulation results of the overshooting time for 2-input NOR gate versus different input signal transition times are shown in Fig. 4.18. Two switching conditions are all considered and the input signal transition time covers a wide range which is from 40ps to 200ps. Compared with SPICE simulation results, the error of the overshooting time obtained from the proposed model is no more than 2.83%.

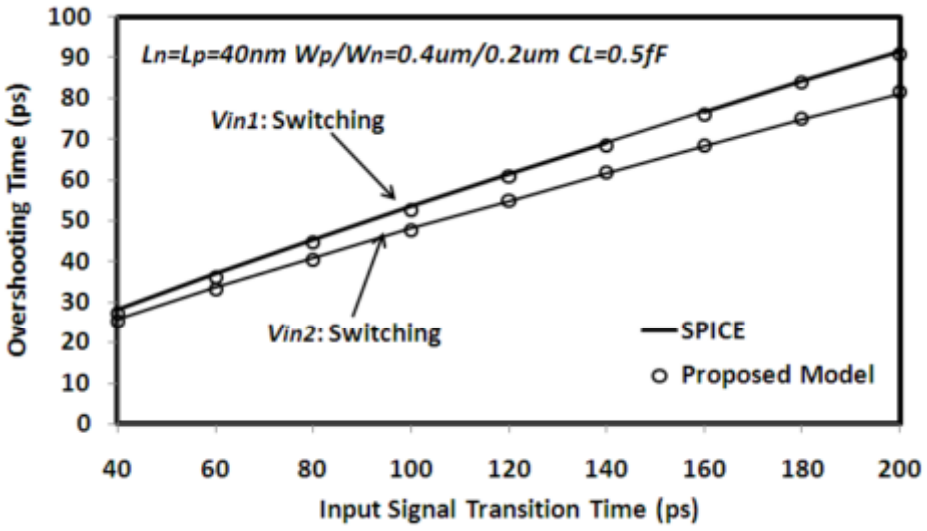

Figure 4.18 Simulation results of 2-input NOR gate.

An approximate method is proposed to model the overshooting effect of 2-input NOR gate in [55]. However, it will be not accurate when the input signal transition time is small. For example, when the input Vin1 is switched for 2-input NOR gate as shown in Fig. 4.4, the overshooting times versus different small input signal transition times are shown in Table 4. The transistor size is $L_n = L_p = 40\text{nm}$ and $W_p = 2W_n = 0.4\text{um}$. The load capacitance is $C_L = 0.5\text{fF}$. The results in Table 4 are

obtained from the SPICE simulations, the proposed model and the model in [3], respectively. Through comparisons, the overshooting time obtained from the proposed model is found at most 3.31% away from the SPICE simulation results. While the error of the overshooting time obtained from the model in [55] is from 6.36% to 9.62%.

Table 4 Overshooting time of 2-input NOR gate when V_{in1} is switched.

t_{in}(ps)	Overshooting Time (ps)			Error (%)	
	SPICE	[55]	Proposed	[55]	Proposed
15	15.6	17.1	16.1	9.62	3.21
20	18.6	20.1	19.2	8.06	3.23
25	21.1	22.6	21.8	7.11	3.31
30	23.6	25.1	24.2	6.36	2.54

The model in [55] will result in large error if applied to the gate with more than two inputs. Meanwhile, the existing method to simplify multiple-input gates to inverters is also not useful when extended to model the overshooting effect for multiple-input gates. Figure 20 shows four different results of the overshooting time for 3-input NOR gate when Vin1 is switched. The four results are obtained from SPICE simulations, the proposed model, the model in [55] and the simplification method in [56]. From the results shown in Fig. 4.19, it is demonstrated that the proposed model is the most accurate within 2.58% error, while the error of the model in [55] is from 5.23% to 9.31%, and the error of [56] is more than 17.7%.

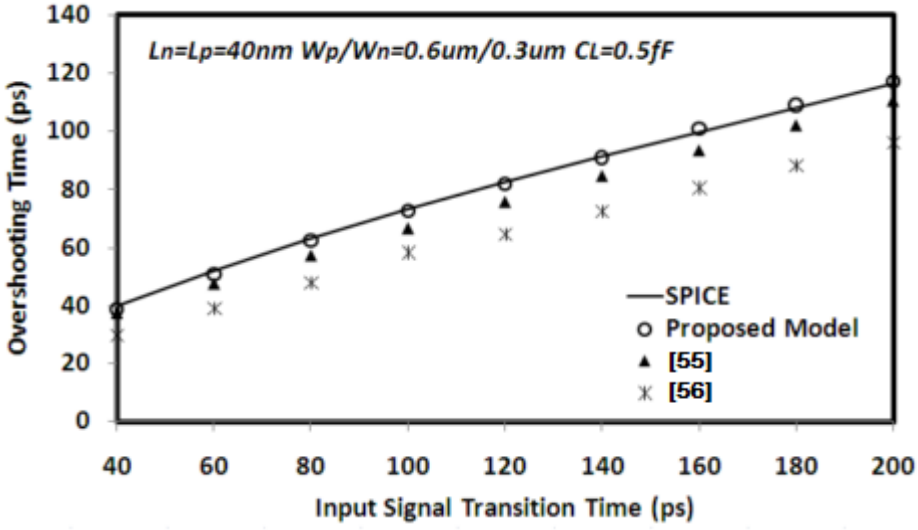

Figure 4.19 Simulation results of 3-input NOR gate when V_{in1} switched.

Table 5 shows the experimental results when applying the proposed model and the model of [55] into multiple-input gates.

Table 5 Overshooting time of multiple-input gates.

NOR Gate	Overshooting Time (ps)			Error (%)	
	SPICE	[55]	Proposed	[55]	Proposed
2-input (Condition1)	15.0	17.2	15.5	14.67	3.34
3-input (Condition2)	33.6	39.7	34.4	18.15	2.38
4-input (Condition3)	50.5	63.0	49.5	24.75	1.98

In Table 5, the overshooting times are obtained for 2-input NOR gate, 3-input NOR gate and 4-input NOR gate when V_{in1} is switched. Condition1 is $L_n = L_p = 40nm$, $W_p = 2W_n = 0.2um$, $t_{in} = 15ps$, $C_L = 0.05fF$. Condition2 is $L_n = L_p = 40nm$, $W_p = 2W_n = 0.2um$, $t_{in} = 30ps$, $C_L = 0.5fF$. Condition3 is $L_n = L_p = 40nm$, $W_p = 2W_n = 1.2um$, $t_{in} = 40ps$, $C_L = 1fF$. According to experimental results shown in Table 5, the error of the overshooting time when applying the model of [55] to 2-input NOR gate is 14.67% while the error using the proposed model is only 3.34%. When the input terminal increases, the error of [55] will increase further. As shown in Table 5, the error when the model of [55] is used for 3-input NOR gate and 4-input NOR gate will be 18.15% and 24.75%, respectively. However, if using the

proposed model to calculate the overshooting time for 3-input and 4input NOR gate, the errors are only 2.38% and 1.98%, respectively. Therefore, the method of [55] is not available if applied to model the overshooting effect of multiple-input gates.

The overshooting times of 3-input NOR gate obtained from the proposed model and SPICE simulation are shown in Fig. 4.20 under different load capacitances. The overshooting times, which include three different switching conditions, are calculated using the method in Sect. 4.3.2. Compared with SPICE simulation results, the error of the overshooting times calculated using the proposed model is below 2.48%. It is demonstrated that the proposed model can predict the overshooting time of 3-input NOR gate accurately.

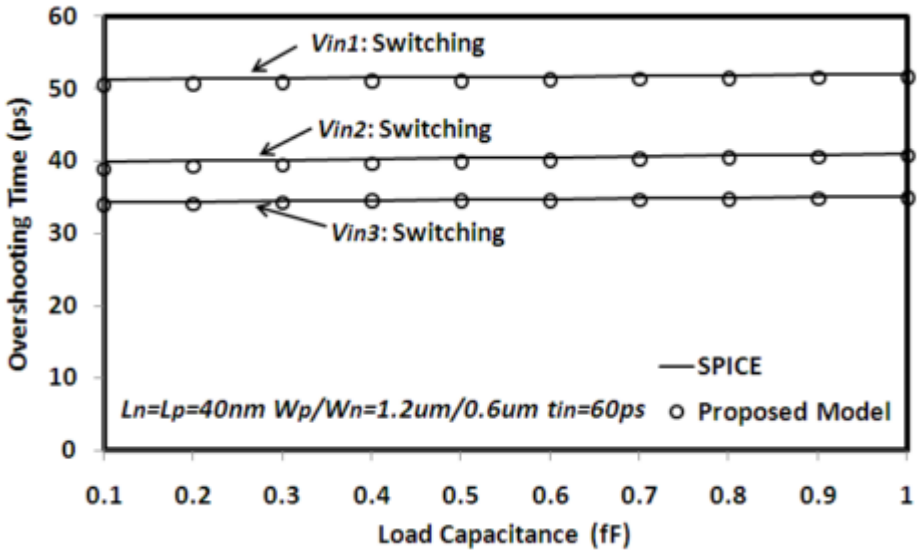

Figure 4.20 Simulation results of 3-input NOR gate.

Although the 2-input and 3-input NOR gates are chosen as an example in this paper, the proposed model can also be extended to other multiple-input gates. Figure 4.21 shows the overshooting time of 3-input NAND gate obtained from the proposed model and SPICE simulations versus different input signal transition times. The error of the results calculated using the proposed model does not exceed 2.32% compared with SPICE simulation results.

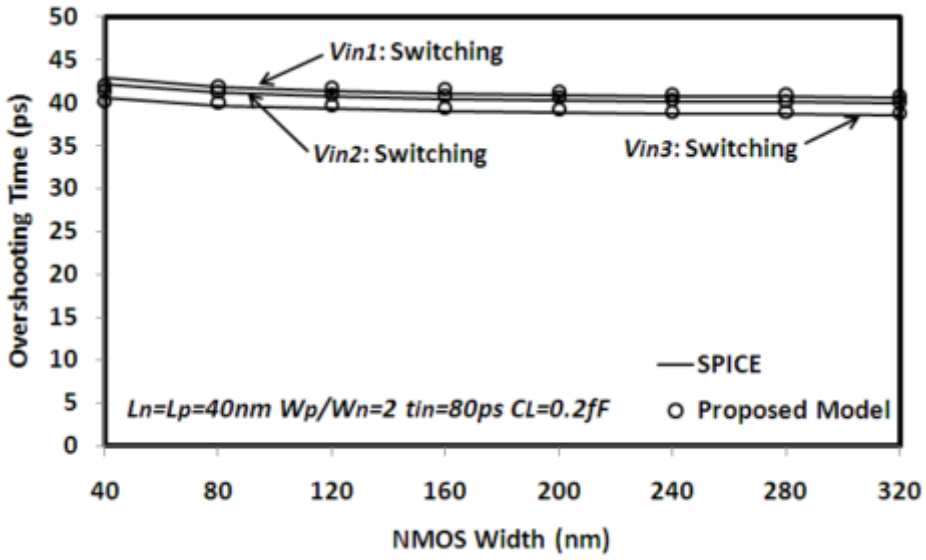

Figure 4.21 Simulation results of 3-input NAND gate.

Furthermore, the proposed model is found still useful when extended to the CMOS gates with more than three inputs according to many other verifications. The overshooting times of 4-input NOR gate obtained from the proposed model and SPICE simulations are shown in Fig. 4.22. The input signal transition time changes from 40ps to 200ps. It is represented from Fig. 4.22 that the error of the proposed model is no more than 2.31% compared with SPICE simulations. Therefore, the proposed model can be regarded as an accurate analytical overshooting effect model for multiple-input gates in nanometer technologies.

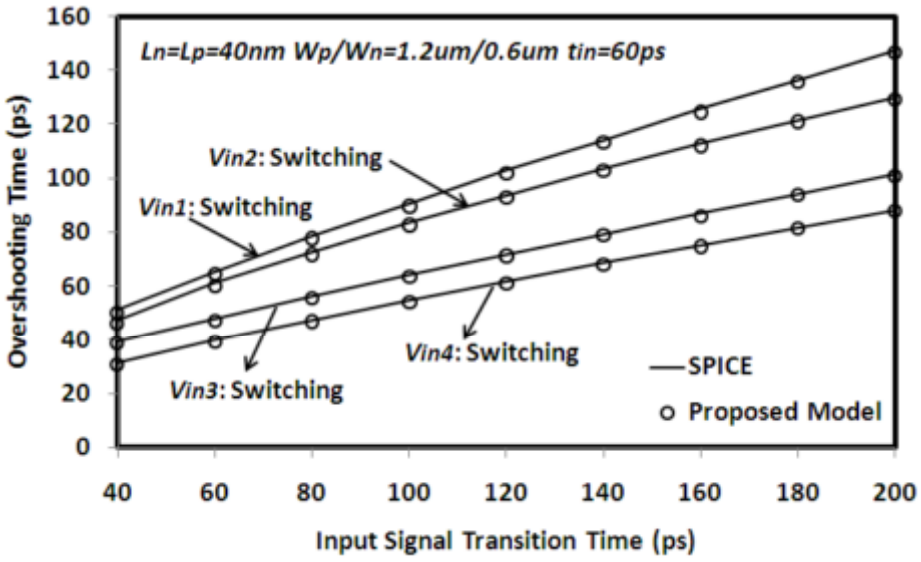

Figure 4.22 Simulation results of 4-input NOR gate.

The proposed model is not only useful for NOR and NAND gate, it is still accurate when applied to other complicated multiple-input gates. The overshooting times of AOI12 gate in Fig. 4.16 obtained from the proposed model and the SPICE simulations are shown in Fig. 4.23. Two different switching conditions are considered and the result obtained from the prosed model is no more than 1.62% compared with SPICE simulation results.

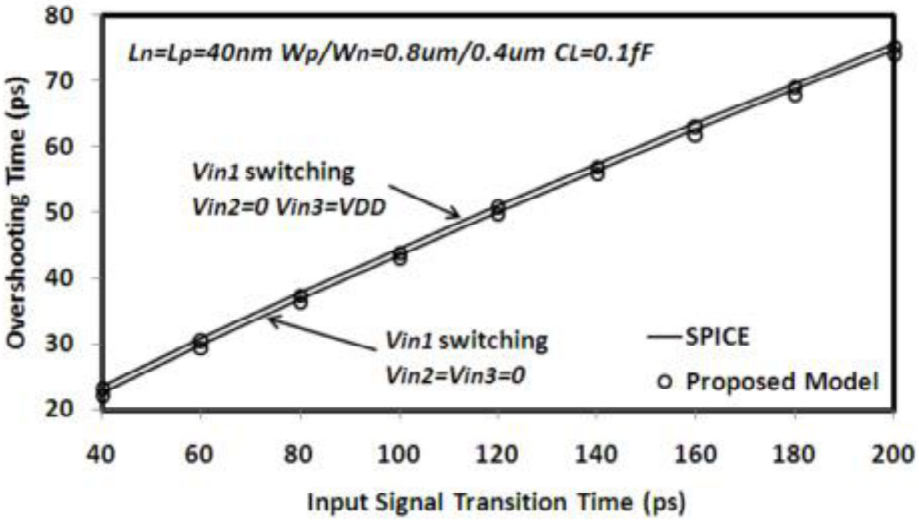

Figure 4.23 Simulation results of AOI12 gate.

It is demonstrated from the simulation results that the proposed model can be applied to model the overshooting effect of multiple-input gate and the overshooting times obtained from the proposed model are accurate compared with SPICE simulation results.

4.5 Application of the Proposed Model

Section 4.3 presents the model of the overshooting effect for multiple-input gates and the accuracy of the proposed model is verified in Sect. 4.4. In this section, the application of the proposed model is discussed.

4.5.1 Gate Delay Calculation

The application of the proposed model in the field of delay analysis of CMOS digital circuits is firstly considered. Static timing analysis (STA) is one of the main technique to verify the timing of a digital design [2]. It usually uses timing libraries with delay (or current) table data which already include the overshooting effect. The calculation from table data needs interpolation between data points. And effect of each parameter on delay is not understood easily. Meanwhile, the proposed model in this paper is formula-based approach which is convenient to easily obtain the overshooting time in evaluating the characteristic of the circuit.

As shown in Eqs. (4.2) and (4.3), delay is related with the input signal transition times t_{in}, the overshooting time t_{ov} and the output voltage rise time t_{rise}. The parameter t_{in} can be easily obtained and the parameter rise is directly extracted from the SPICE simulation results. The parameter t_{ov} can be obtained from overshooting effect models. In [24] and [28], the authors assumed the output waveform of an inverter rises/falls at the time $t = t_P / t = t_N$, where t_P and t_N are the time when PMOS and NMOS turn on respectively. In this paper, the simple method in [24] and [28] is assumed as a simple model to reflect the overshooting time. Thus, in the assumed simple model, the overshooting time of 3-input NOR gate is the time when the switched PMOS turns on.

For 3-input NOR gate, gate delay can be calculated using Eqs. (4.2) and (4.3). The overshooting time t_{ov} can be obtained from the proposed model in this paper and the simple model. Gate delay obtained from SPICE simulations, the proposed model and the simple model is shown in Table 6 for 3-input NOR gate when V_{in1} is switched.

The transistor size is $L_n = L_p = 40nm$ and $W_p = 2W_n = 0.8um$. The load capacitance is $C_L = 0.5fF$. As shown in Table 6, when using Eqs. (4.2) and (4.3) to calculate the gate delay, obtaining t_{ov} from the proposed model is much more accurate than t_{ov} from the simple model.

Table 6 Gate delay of 3-input NOR gate obtained from Eqs. (4.2) and (4.3).

t_{in} (ps)	Gate Delay (ps)			Error (%)	
	SPICE	Proposed	Simple	Proposed	Simple
30	41	40	20.2	2.44	50.7
50	45.9	44.8	20.1	2.4	56.2
70	50.5	49.8	21.4	1.39	57.6
90	54.8	53.8	23.2	1.82	57.7
110	58.9	57.7	25.7	2.04	56.4

4.5.2 Improvement of Thevenin Equivalent Model

Figure 4.24 (a) shows a 3-input NOR gate driving a RC interconnect load. Traditionally, the Thevenin equivalent model is used widely in delay analysis of the gate with interconnect load [59]. As shown in Fig. 25 (b), the 3-input NOR gate is replaced by an equivalent voltage source V_{inTH} in series connection with an equivalent resistance R_{TH}. With some value for R_{TH}, it is necessary to search for the Thevenin voltage V_{inTH} which will produce an accurate gate-output waveform and delay as the actual gate [59]. Therefore, an additional time period is added to the Thevenin equivalent voltage source due to the obviousness of the overshooting effect in nananometer regime. As shown in Fig. 4.24 (b), the equivalent voltage source V_{inTH} will holds in zero from the beginning to $t = t_{ov}$. Figure 4.25 shows the output waveforms of the 3-input NOR gate in Fig. 4.24 (a) and the Thevenin equivalent model in Fig. 4.24 (b), where $L_n = L_p = 40nm$, $W_p = 2W_n = 1.2um$, $t_{in} = 40ps$, $C1 = 0.2fF$, $R1 = 200\Omega$, $C1 = 0.5fF$. Also, the overshooting time tov is obtained from the proposed model.

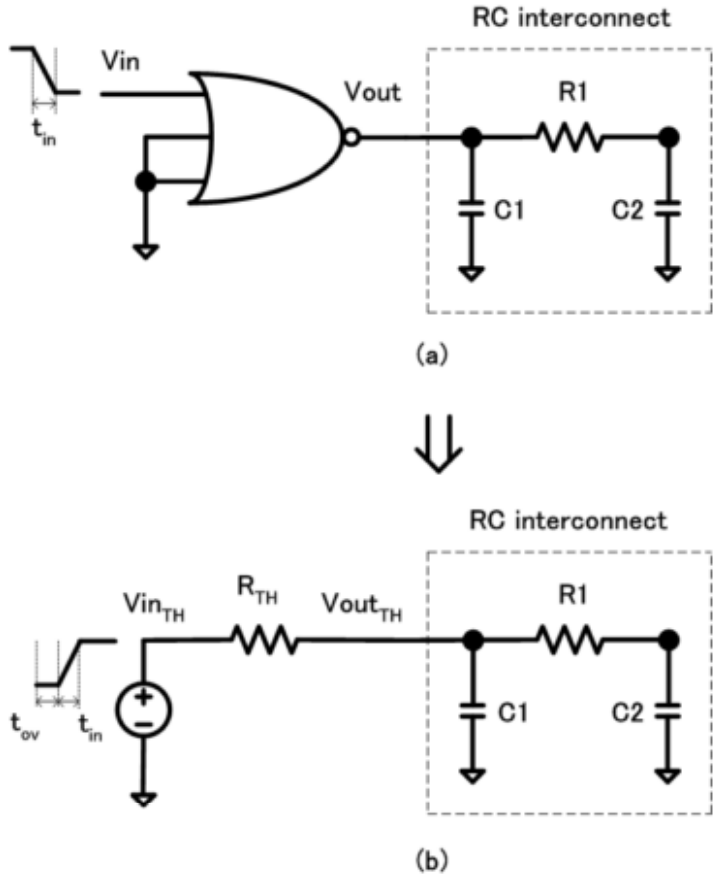

Figure 4.24 3-input NOR gate driving an RC interconnect load and its Thevenin equivalent model.

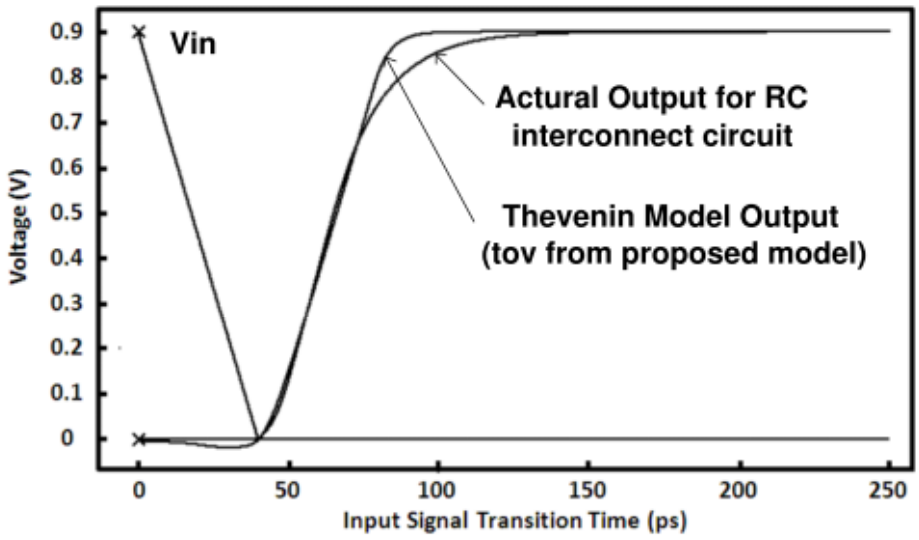

Figure 4.25 Output waveform from RC interconnect circuit in Fig. 4.24 (a) and Thevenin equivalent circuit in Fig. 4.24 (b).

It is clearly demonstrated from Fig. 4.25 that the output waveform of the improved Thevenin equivalent circuit is close to the actual gate with interconnect loads very much. That means, the proposed overshooting effect model is useful for improving the accuracy of Thevenin equivalent model.

Except for the application in the field of delay analysis, the overshooting time is also an important parameter in the short-circuit energy dissipation estimation [4]. Therefore, in order to improve the accuracy of modeling the CMOS gate delay and short-circuit energy dissipation, it is meaningful to develop an accurate and effective model for the overshooting effect of multiple-input gates.

From the discussion in this section, it can be known that the proposed overshooting effect model for multiple-input gate is meaningful and helpful for digital LSI.

4.6 Conclusions

With CMOS technology entering into nanometer regime, the overshooting effect of multiple-input gates cannot be neglected while considering the gate delay and power consumption. The overshooting effect models for an inverter which have been proposed cannot be extended to model the overshooting effect for multiple-input gates. Moreover, the simplification methods using in conventional gate delay models are also not available to simplify the multiple-input gates when model the overshooting effect. Therefore, an effective model of the overshooting effect for multiple-input gates is proposed in this chapter.

In this chapter, the overshooting time expressions for 2-input NOR gate is firstly proposed. It is formula-based overshooting effect model. Based on the overshooting effect model for 2-input NOR gate, the method to model the overshooting effect for 3-input NOR gate is presented. The proposed model is not only available for 2-input and 3-input conditions, it can be also extended to many other multiple-input gates. Therefore, how to extend the proposed model to multiple-input gates is introduced in this chapter.

The overshooting time of multiple-input gates obtained from the proposed model and SPICE simulations are given in the verification works. Experimental results show that the proposed model can calculate the overshooting time of multiple-input gates accurately. And the accuracy is also higher than the model in Sect. 3 when applied to 2-input gate under some conditions.

The application of the proposed model is also researched. The proposed overshooting effect model can be used to increase the accuracy of gate delay model and improve the accuracy of Thevenin equivalent model.

Appendix A: Calculation of t_{ov} for 2-Input NOR Gate

In the Appendix, the calculation method to obtain the overshooting time of 2-input NOR gate is explicitly presented. When V_{in1} is switched, the condition is more complicated than the condition when V_{in2} is switched. Therefore, the analysis in the Appendix focuses on the condition when V_{in1} is switched. For the condition when V_{in2} is switched, the analysis method is almost the same.

Modeling the overshooting effect for an inverter has been researched in [3] where the overshooting time expressions are proposed. For a 2-input NOR gate, the overshooting time expressions are similar to an inverter which has been already given in Eq. (4.4). However, the parameters in Eq. (4.4) have some differences for 2-input NOR gate compared with an inverter. Compared with [3], the different parts of the 2-input NOR gate in Fig. 4.4 are the point of V_1 due to the appearance of MP2 and the coupling capacitances. Therefore, the aim of the Appendix is to handle the node voltage V_1 in Fig. 4.4 and add the influence of input-to-output coupling capacitances in Fig. 4.4 to the overshooting time expressions explicitly. Moreover, the method in the Appendix is also true when analyzing the 2-input NOR gate in Fig. 4.5.

Applying KCL at the output node, the differential equation for the NOR gate in Fig. 4.4 can be expressed as

$$I_{MP2} - I_{MN1} + C_{gd1}\frac{d(V_{in1}-V_{out})}{dt} = \left(C_{gd2} + C_{gd4} + C_L\right)\frac{dV_{out}}{dt}, \quad (A.1)$$

where I_{MN1} and I_{MP2} are the drain currents of transistors MN1 and MP2 respectively. C_{gd1}, C_{gd2} and C_{gd4} are all coupling capacitances whose values are obtained directly from SPICE simulation results in this proposed model. C_L is the load capacitance.

The overshooting time tov can be expressed as [3]

$$t_{ov} = \frac{2Q_1}{I_{CL}(t_{ov})} + t_{vmin}, \quad (A.2)$$

where Q_1 is the charge flowing out of C_L, $I_{CL}(t_{ov})$ is the current of load capacitance at the time $t = t_{ov}$. From Eq. (A.2), we can find the overshooting time

tov is determined by Q_1, $I_{CL}(t_{ov})$ and t_{vmin}. In the followings, the calculation of these three items will be described in detail.

A) Calculation of Q_1

When $t \le t_{TP}$, the PMOS transistor MP2 is cut off, then the drain current of MP2 is almost 0. Since the drain-to-source voltage V_{DS} and the gate-to-source voltage V_{GS} of MN1 have the relationship that $V_{DS} \ll V_{GS}$ when $t \le t_{TP}$, the drain current of MN1 can be simply expressed as [3]

$$I_{MN1} \approx \beta_n (V_{GS} - V_{TN}) V_{DS}, \qquad \text{(A.3)}$$

where $\beta_n = K'W/L$, K' is the transconductance parameter, V_{GS} is the gate-to-source voltage, V_{DS} is the drain-to-source voltage and V_{TN} is the threshold voltage of MN1. Then Eq. (A.3) can be expressed as

$$\left(C_{gd1} + C_{gd2} + C_{gd4} + C_L\right)\frac{dV_{out}}{dt} + \beta_n (V_{GS} - V_{TN}) V_{out} = C_{gd1}\frac{dV_{in1}}{dt}. \qquad \text{(A.4)}$$

The solution of Eq. (A.4) at the time $t = t_{TP}$ is given as

$$V_{out}(t_{TP}) = \frac{C_{gd1}\frac{dV_{in1}}{dt}}{\beta_n (V_{DD} - |V_{TP}| - V_{TN})} \times \left[1 - e^{-\frac{\beta_n (V_{DD} - |V_{TP}| - V_{TN})}{C_{gd1} + C_{gd2} + C_{gd4} + C_L}\frac{t_{in}|V_{TP}|}{V_{DD}}}\right], \qquad \text{(A.5)}$$

where V_{TP} is the threshold voltage of MP1.

Because the output voltages at the time $t = t_{vmin}$ and $t = t_{TP}$ have the relationship $V_{out}(t_{vmin}) \approx V_{out}(t_{TP})$ [3], the charge Q_1 can be expressed as

$$Q_1 \approx C_L V_{out}(t_{TP}). \qquad \text{(A.6)}$$

B) Calculation of t_{vmin}

When $t = t_{vmin}$, the output voltage is at its minimum and $\frac{dV_{out}}{dt} = 0$. Then Eq. (A.1) can be expressed as

$$I_{MN1}(t_{vmin}) = I_{MP2}(t_{vmin}) + C_{gd1}\frac{dV_{in1}}{dt}. \quad (A.7)$$

Meanwhile, the valueof I_{MP2} can also be expressed as

$$I_{MP2} = I_{MP1} + C_{gd3}\frac{d(V_{in1}-V_1)}{dt} + C_{gs4}\frac{d(V_{in2}-V_1)}{dt}, \quad (A.8)$$

where I_{MP1} is the drain current of MP1, C_{gd3} and C_{gs4} are the coupling capacitances, V_1 is the voltage of the node between MP1 and MP2 as shown in Fig. 4.4. When $t = t_{vmin}$, $\left|\frac{dV_1}{dt}\right| \ll \left|\frac{V_{in1}}{dt}\right|$ is established according to various verifications results under different conditions. Therefore, $\frac{dV_1}{dt}$ can be regarded as 0 and Eq. (A.7) is transferred to

$$I_{MN1}(t_{vmin}) = I_{MP1}(t_{vmin}) + \left(C_{gd1} + C_{gd3}\right)\frac{dV_{in1}}{dt}. \quad (A.9)$$

Since $V_{out}(t_{vmin}) \approx V_{out}(t_{TP})$, $I_{MN1}(t_{vmin}) \approx I_{MN1}(t_{TP})$ is established. At the time $t = t_{vmin}$, the drain-to-source voltage of MN1 V_{DS} is equal to the output voltage V_{out}. Then substituting (A.5) into (A.3), we obtain

$$I_{MN1}(t_{vmin}) = C_{gd1}\frac{dV_{in1}}{dt} \times \left[1 - e^{-\frac{\beta_n(V_{DD}-|V_{TP}|-V_{TN})}{C_{gd1}+C_{gd2}+C_{gd4}+C_L}\frac{t_{in}|V_{TP}|}{V_{DD}}}\right]. \quad (A.10)$$

As shown in Fig. 4.4, the approximate drain currents of PMOS MP1 obtained using α-power MOSFET model are very close to the results simulated from SPICE BSIM3 model. Thus, the α-power MOSFET model [25] is used to calculate $I_{MP1}(t_{vmin})$ and the drain current of MP1 when $t = t_{vmin}$ is expressed as

$$I_{MP1}(t_{vmin}) = I_{D0}\left(\frac{|V_{GS}(t_{vmin})|-|V_{TP}|}{V_{DD}-|V_{TP}|}\right)^{\alpha}, \quad (A.11)$$

where I_{D0} is the drain current of MP1 in the saturation region when $V_{GS} = V_{DS} = V_{DD}$, α is the velocity saturation index and $|V_{GS}(t_{vmin})| = V_{DD}t_{vmin}/t_{in}$.

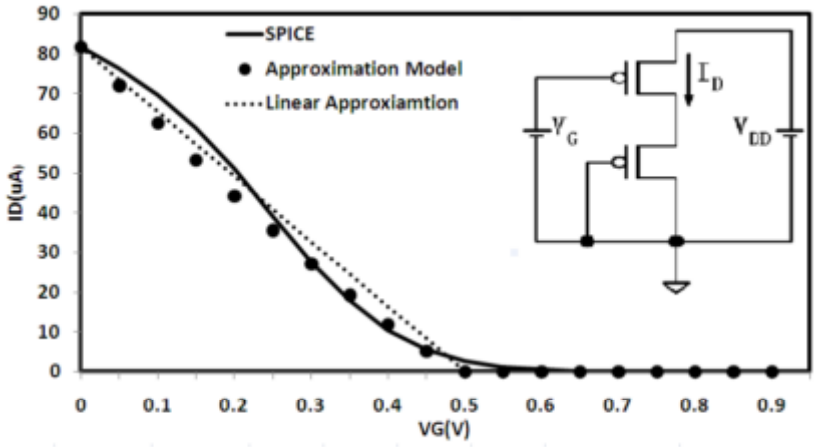

Figure A.1 α-power approximation for PMOS transistor drain current.

After substituting Eqs. (A.10) and (A.11) into Eq. (A.9), the equation can be obtained as

$$C_{gd1}\frac{-V_{DD}}{t_{in}}\left[1-e^{-\frac{\beta_n(V_{DD}-|V_{TP}|-V_{TN})}{C_{gd1}+C_{gd2}+C_{gd4}+C_L}\frac{t_{in}|V_{TP}|}{V_{DD}}}\right]=I_{D0}\left(\frac{t_{vmin}-t_{TP}}{t_{in}-t_{TP}}\right)^{\alpha}+\left(C_{gd1}+C_{gd3}\right)\frac{-V_{DD}}{t_{in}}, \quad (A.12)$$

where t_{TP} is the time when PMOS transistor MP1 is switched on and $t_{TP}=\frac{|V_{TP}|}{V_{DD}}t_{in}$.

Through solving the equation (A.12), we obtain the expression for t_{vmin}

$$t_{vmin}=t_{TP}+(t_{in}-t_{TP})\times\left[\frac{V_{DD}}{I_{D0}t_{in}}\left(C_{gd1}e^{-\frac{\beta_n(V_{DD}-|V_{TP}|-V_{TN})}{C_{gd1}+C_{gd2}+C_{gd4}+C_L}\frac{t_{in}|V_{TP}|}{V_{DD}}}+C_{gd3}\right)\right]^{\frac{1}{\alpha}}. \quad (A.13)$$

C) Calculation of $I_{CL}(t_{ov})$

When $t=t_{ov}$, the output voltage is 0 so that $I_{MN1}=0$. Meanwhile since $\left|\frac{dV_{in1}}{dt}\right| \gg \left|\frac{dV_{out}}{dt}\right|$, $\frac{dV_{out}}{dt}$ can be regarded as 0. Thus, the current of load capacitance can be obtained through simplifying Eq. (A.1)

$$I_{CL}(t_{ov}) = I_{MP2}(t_{ov}) + C_{gd1}\frac{dV_{in1}}{dt}. \quad (A.14)$$

When $t = t_{ov}$, the approximate expression $\left|\frac{dV_1}{dt}\right| \approx \frac{1}{2}\left|\frac{dV_{in1}}{dt}\right|$ is established due to numerous simulations under different input conditions, transistor sizes and load capacitances. Thus, $I_{MP2}(t_{ov})$ can be expressed

$$I_{MP2}(t_{ov}) = I_{MP1}(t_{ov}) + \left(1.5C_{gd3} + 0.5C_{gs4}\right)\frac{dV_{in1}}{dt}. \quad (A.15)$$

Therefore, in order to simplify the calculation process the value of α in α-power MOSFET model is set as 1, then the linear transistor drain current model for MP1 as shown in Fig. 4.4 is used. The drain current of MP1 when $t = t_{ov}$ is approximately described as

$$I_{MP1}(t_{ov}) = I_{D0}\left(\frac{|V_{GS}(t_{ov})| - |V_{TP}|}{V_{DD} - |V_{TP}|}\right), \quad (A.16)$$

where V_{TPL} is the equivalent threshold voltage obtained from the intersection of the dotted line and horizontal axis in Fig. 4.4.

D) Calculation of t_{ov}

After substituting (A.14) into (A.2), we obtain an expression for t_{ov}

$$t_{ov} = \frac{2Q_1}{\frac{t_{ov} - t_{TPL}}{t_{in} - t_{TPL}} I_{D0} + (C_{gd1} + 0.5C_{gs4} + 1.5C_{gd3})} + t_{vmin}, \quad (A.17)$$

where $t_{TPL} = \frac{|V_{TPL}|}{V_{DD}} t_{in}$. Then by solving (A.17), we can get the initial solution of t_{ov} which is expressed as

$$t_{ov} = t_{vmin} - t_{\gamma 1} + \sqrt{\frac{2Q_1}{I_{D0}}(t_{in} - t_{TPL}) + t_{\gamma 1}^2}, \quad (A.18)$$

where

$$t_{\gamma 1} = \frac{1}{2}\left[t_{vmin} - t_{TPL} - (C_{gd1} + 0.5C_{gs4} + 1.5C_{gd3})\frac{V_{DD}}{I_{D0}}\frac{t_{in} - t_{TPL}}{t_{in}}\right]. \quad (A.19)$$

Chapter5
Conclusions

5.1 Dissertation Conclusions

Timing analysis is a useful verification method in modern VLSI design. It can be used to verify the timing characteristics of complicated digital VLSI systems. Gate delay is an important performance parameter in timing analysis.

The overshooting effect, which will affect the gate delay calculation, is much more obvious with the scaling of CMOS process technology. Especially, when CMOS process technology enters nanometer regime, the overshooting effect cannot be neglected again. Researchers have already given the overshooting effect models for an inverter. However, the overshooting effect model for multiple-input gates is seldom presented. Simplification method is used in conventional gate delay models of multiple-input gates whose principle is simplifying the multiple-input gates to an inverter. This simplification method will cause large error if used to model the overshooting effect of multiple-input gates. And the conventional overshooting effect model of an inverter cannot be extended to multiple-input gates directly. Therefore, modeling the overshooting effect of multiple-input gates is researched in this dissertation. There are two overshooting effect model for multiple-input gates are proposed. The first model is simple and accurate when calculating the overshooting time of 2-input gates. The second model is formula-based and can be extended to many multiple-input gates.

In the first chapter of this dissertation, the background and motivation of this dissertation is given. Subsequently, the overshooting effect of an inverter and multiple-input gates are introduced in Chapter 2, where the phenomenon and influence of overshooting effect are analyzed. The main part of this dissertation is about the proposed model in Chapter 3 and Chapter 4. In Chapter 3, the overshooting effect model which can be applied to 2-input gate is presented. There are two different input conditions for 2-input gate. The proposed model can be used to calculate the overshooting time of 2-input gate using equations and proportional coefficient method. Simulation results in Chapter 3 reflect that the proposed model can model the

overshooting effect of 2-input gate within 3.6% error. In Chapter 4, the proposed overshooting effect model can predict the overshooting time of many multiple-input gates. Formula-based overshooting effect model for 2-input gate and overshooting effect model for 3-input gate is proposed in Chapter 4. Meanwhile, how to extend the proposed model to the condition of other multiple-input gates is also analyzed. Many verification works represent that the proposed model is accurate whose maximum error is only 3.4%. Moreover, the application of the proposed overshooting effect model is talked about in Chapter 4.

Finally, the conclusions and future work are given in Chapter 5.

5.2 Future Work

When CMOS process enters nanometer regime, the overshooting effect is important and cannot be neglected when calculate the gate delay. In this dissertation, the overshooting effect models of multiple-input gates are proposed. The proposed model can predict the overshooting time of multiple-input gates accurately.

In the future, how to extend the proposed model to other multiple-input gates will be verified verified. Meanwhile, giving a common rule to calculate the overshooting time of multiple-input gates is also meaningful.

The overshooting time is an important component for gate delay in nanometer technologies. As we know, process variation will affect the gate delay. However, in this dissertation, we just give a method to calculate the overshooting time. How the overshooting time of multiple-input gates varies due to the variations of electrical parameters induced by process variation is not considered. Therefore, the overshooting effect will be researched again considering about the process variation.

Moreover, the proposed overshooting effect model is a little complicated. Empirical gate delay models are widely used in industry due to its convenience. We will also focus on the improvement of the overshooting effect model to give a more simple overshooting effect model with high efficiency.

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