Waseda University Doctoral Dissertation

Research on Ultra-low-power Voltage References with Body Biasing Technologies

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Abstract

In recent years, the research of analog circuit design pays more attention on the design of ultra-low-power VLSI circuits. Voltage scaling is the most effective solution to stringent power requirements and has been practically demonstrated in a number of designs in scaled CMOS technology. Hence, ultra-low-power design translates into ultra-low-voltage design. All kinds of subthrehold integrated circuits have be developed because the weak inversion biasing of MOS transistors allows minimum energy consumption when the voltage is scaled below the device threshold voltage, which is an energy-efficient design. Voltage reference, as an important analog building block, plays a critical function in determining the performance of these subthreshold integrated circuits. Therefore, a reference voltage below the threshold voltage (V_{th}) and a nano-power dissipation consumed by the circuit are essential to ensure the operation of these subthreshold designs.

Voltage references can supply a fixed dc voltage of known amplitude that does not change with temperature, supply voltage and process variations. The most important performances of a voltage reference are represented by temperature behavior, power supply rejection ratio, transient response, and power dissipation. The voltage reference circuits are fundamentally implemented in bipolar and CMOS technology. Some elementary voltages, e.g., base-emitter voltage, gate-source voltage or threshold voltage, thermal voltage, or their linear combinations are used for realizing a reference voltage with zero temperature coefficient. The conversional method for designing voltage references using bipolar transistors is not suitable for low-voltage applications because of the silicon bandgap energy (1.2 V). The designs using MOS

transistors are recently explored for the ultra-low-power voltage reference, and the reference voltages are less than 1 V. However, the disadvantages of these designs are the values of their outputs are above the threshold voltage because the threshold voltage is used as the absolute reference source. The low output can be obtained by using the components networks (resistors or capacitors). However, a trade-off between the power dissipation and chip area cannot be avoided because low current requires large resistor, and the capacitive networks occupy more chip area because more capacitors and large subdivision are required. Several designs make use of the difference in the threshold voltage between two distinct devices, e.g. depletion transistor, or native transistor, or low-threshold-voltage transistor and standard transistor. Such approach requires multiple-V_{th} CMOS technology for fabrication, and the actual value of the reference is difficult to determine accurately because of the process sensitivity of the difference between threshold voltage levels from two distinct transistors. In the dissertation, the design and development of novel circuit architectures and design techniques to implement voltage references for application in subthreshold LSI are originally explored, the low output under threshold voltage can be directly achieved without using any component dividers, and the circuits consume nano-power dissipation can be implemented in standard CMOS technology.

In the reported ultra-low-power applications, body biasing technologies are all tools that have the potential to lower supply voltage and consequently the total energy consumed by the circuit. In this dissertation, the technologies for designing voltage references using MOS body effect are developed to improve the performance of the circuits. Detailed theoretical analysis is presented and measurement results are given to prove the merits of the proposed circuits. The outline of the dissertation is listed as following:

Chapter 1 starts with the introduction of the background, and explains the importance and necessity of the voltage reference for

application in subthreshold LSI. The previous arts are presented and the existing problems in these designs are analyzed in detail. And the objectives in this research are clarified.

Chapter 2 gives an overview of several designs using MOS body effect. For voltage references, the fundamental principles are described in detail, and the classic structures are discussed. Based on the self-biased architecture, an all-MOSFETs structure is proposed to improve the typical architecture. The substrate node of one transistor is connected to its gate node, which constructs a forward-biased connection, while the substrate node of another one has normal connection. Such that the output voltage is the gate-source voltage difference between the two transistors. Then, the temperature compensation can be implemented by choosing an adaptive size ratio of transistors. According to simulations, the typical T.C. is 14.8 ppm/°C. The line sensitivity is approximately 0.0019 %/V. The power dissipation at 1.4 V supply voltage is 1.4 μW. Thanks to the only two current branches in the proposed circuit, the design area is small, approximately 0.014 mm^2.

Chapter 3 concentrates a novel approach for implementing an ultra-low-power voltage reference using the structure of self-cascode MOSFET, operating in the subthreshold region with a self-biased body effect. The difference between the two gate-source voltages in the structure enables the voltage reference circuit to produce a low output voltage below the threshold voltage. The trimming procedures are implemented for this design. The circuit is designed with only MOSFETs and implemented in standard 0.18-μm CMOS technology. Measurements show that the reference voltage is about 107.5 mV, and the temperature coefficient is about 40 ppm/°C, at a range from -20 °C to 80 °C. The voltage line sensitivity is 0.017 %/V. The minimum supply voltage is 0.85 V, and the supply current is approximately 24 nA at 80 °C. The occupied chip area is around 0.028 mm^2.

Chapter 4 presents a nano-power CMOS voltage reference. A combination of switched-capacitor technology and the body effect in

MOSFETs for the implementation of voltage reference is firstly developed, the output voltage is defined as the difference between two gate-source voltages using only a single PMOS transistor operated in the subthreshold region, which has low sensitivity to the temperature and supply voltage. Only two capacitors are required for the operation. The low output, which breaks the threshold restriction, is produced without large capacitive subdivision and scalable by adjusting the ratio of capacitors, such that the chip area is saved. And flexible trimming capability can be achieved with a composite transistor. The chip is implemented in 0.18 μm standard CMOS technology. Measurements show that the output voltage is approximately 123.3 mV, the temperature coefficient is 17.6 ppm/°C, and the line sensitivity is 0.15 %/V. When the supply voltage is 1 V, the supply current is less than 90 nA at room temperature. The area occupation is approximately 0.03 mm^2.

Chapter 5 proposes a novel approach for implementing switched-capacitor voltage reference. With body biasing technology in MOSFET, the operation uses only a single on-chip capacitor and a PMOS transistor to generate a output voltage which has low sensitivity to the temperature. The low output is under the threshold voltage without the use of components dividers, which saves the chip area and avoid the mismatches between capacitors. The design is simulated and measured in 0.18-μm CMOS technology. Measurements show that the output voltage is approximately 121.1 mV. The temperature coefficient after trimming is approximately 35.1 ppm/°C. At room temperature, the line sensitivity is approximately 0.12 %/V, and the supply current is less than 100 nA from 1 V supply. The circuit occupies a 0.013 mm^2 chip area.

Chapter 6 concludes the proposals in this dissertation, and the future works are presented.

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1

Introduction

Voltage reference, as an important analog building block, plays a critical function in determining the performance of integrated circuits. In recent years, the research pays more attention on the design of low-power dissipation. All kinds of subthrehold integrated circuits have be developed. Then, a reference voltage below the threshold voltage as well as nano-power dissipation is required to ensure the operation of these subthreshold integrated circuits. In this chapter, the background of the low-power design has been presented, several typical voltage references have been reviewed, the purpose of this research is confirmed.

1.1 Background

Since the invention of the transistor, continuous technology scaling has led to the integration of growing computational capabilities in an increasingly small volume. The aggressive scaling of CMOS technologies has provided for an exponential growth in the computational power obtainable in a single integrated circuit, which increases more power dissipation. Such that a battery that has more lifetime to ensure the operation in battery-operated systems is required. However, the battery technology has evolved much slower than CMOS technology. To satisfy the growing demand for long-life autonomous portable equipment and high-performance VLSI systems, ultra-low-power operation has become the mainstream technique for LSI design.

The reduction in supply voltage is certainly a very effective lever to reduce power and energy consumption, thereby relaxing the cooling requirements and extending the battery life of portable electronics. Subthreshold circuit became popular for the ultra-low-power design because weak inversion in transistor allows supply voltage reduction as well as the very low bias current [1]. Various subthreshold integrated circuits with a power supply voltage below transistor threshold voltage (V_{th}), such as processor [2, 3, 4], memory [5, 6], ADC [7, 8], and logic circuits [9], are proposed. As a critical building block in these circuits, voltage references are extensively used to generate a DC voltage independent of the process, supply voltage and temperature, which have significant functions in determining the performance of these circuits. Therefore, the designer needs to develop a voltage reference (VR) that produces a low ($< V_{th}$) output voltage and consumes ultra-low power dissipation for subthreshold operation in all subsequent circuits.

1.2 Reported Voltage References

Voltage references (VRs) are widely used in the integrated circuits, which can offer a stable voltage no matter how the temperature and supply voltage changed. The output voltage (V_{ref}) is expressed as a sum of a complementary to absolute temperature (CTAT) term and a proportional to absolute temperature (PTAT)

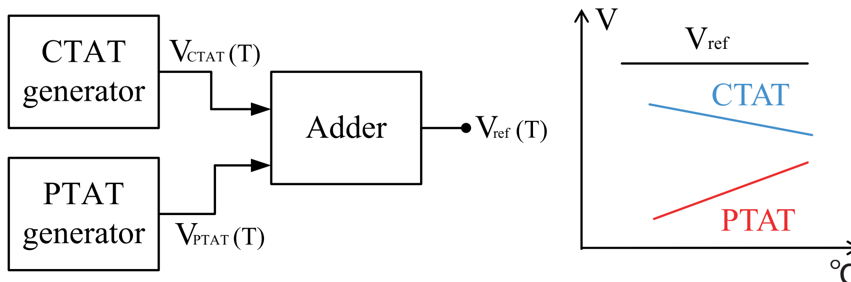


Figure 1.1: Fundamental principle of voltage reference.

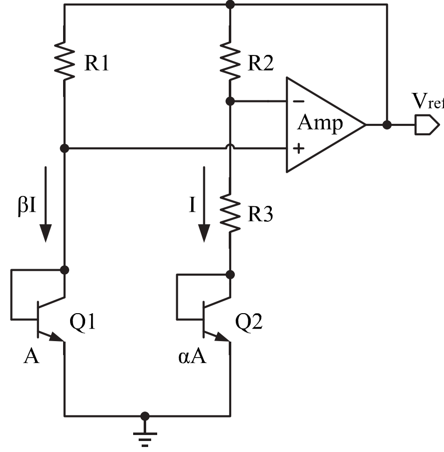


Figure 1.2: Simple structure of bandgap voltage reference.

term [10], as shown in Fig. 1.1. The expression can be given as:

$$V_{ref}(T) = V_{CTAT}(T) + V_{PTAT}(T). \tag{1.1}$$

The CTAT term presents a negative temperature variation, whereas the PTAT term has a positive temperature dependence. Thus, the output can achieve a low sensitivity to the temperature through the compensation between CTAT term and PTAT term, which means V_{ref} has a zero temperature coefficient (T.C.). Such method can be implemented for designing voltage reference circuits in bipolar and CMOS technology.

1.2.1 Bandgap Voltage Reference

A possible implementation in bipolar technology of a VR with approximately linear negative temperature dependence uses the base-emitter voltage (V_{BE}) of a bipolar transistor. Fig. 1.2 shows the simple structure [11], the bipolar transistor is connected as a diode, the output voltage can be expressed as

$$V_{ref} = V_{BE2} + \frac{V_T \ln(\alpha\beta)}{R_3}(R_3 + R_2). \tag{1.2}$$

where V_T is the thermal voltage, α is the size ratio between the two transistors, and β is the current ratio between the two transistors. V_{BE} is used as the CTAT

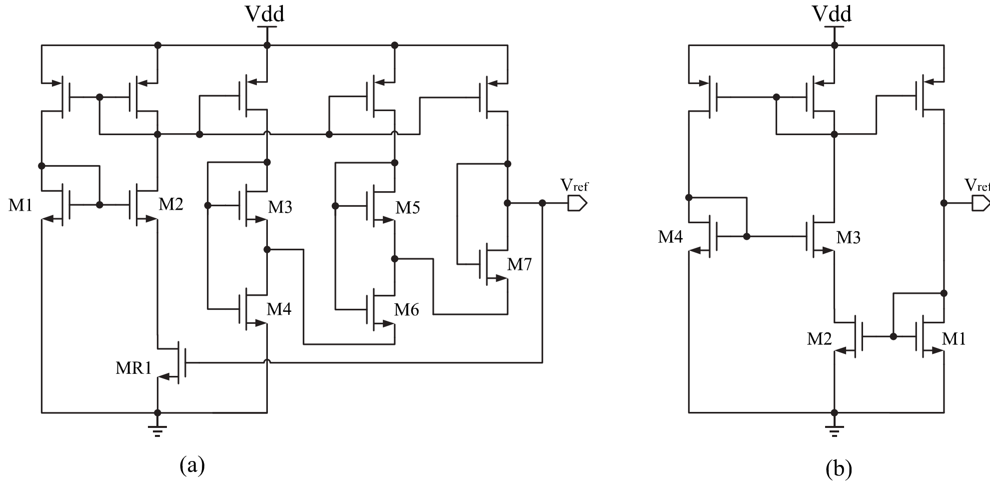


Figure 1.3: Low-power VRs: (a) CTAT term based on V_{gs} of a MOS transistor biased in weak inversion [13]; (b) CTAT term based on V_{th} of a MOS transistor biased in saturation region [16].

term which has a negative T.C., while V_T can supply a positive T.C., such that V_{ref} can achieve a zero T.C. through the temperature compensation.

The most important disadvantage of the voltage reference is that the minimal reference voltage is larger than 1.0 V because of the silicon bandgap energy (about 1.2 V), so the structure is not suitable for the low-voltage applications.

1.2.2 CMOS Voltage Reference

Recently, the design of the low-voltage low power VRs by using MOSFETs is explored. The distinction between CMOS VRs and bandgap VRs depends on the CTAT term. For CMOS VRs, the gate-source voltage (V_{gs}) of a MOS transistor biased in weak inversion or the threshold voltage (V_{th}) is used as the CTAT term because V_{th} has negative T.C. [10]. The reported VRs are given as follows.

Subthreshold MOSFETs used for the design of VR can achieve the CTAT term starting from V_{gs} and the PTAT term exploiting a difference between two gate-source voltages (ΔV_{gs}) in transistors which are biased in the weak inversion. The usual output voltage (V_{ref}) can be given by

$$V_{ref} = V_{gs} + \Delta V_{gs}. \tag{1.3}$$

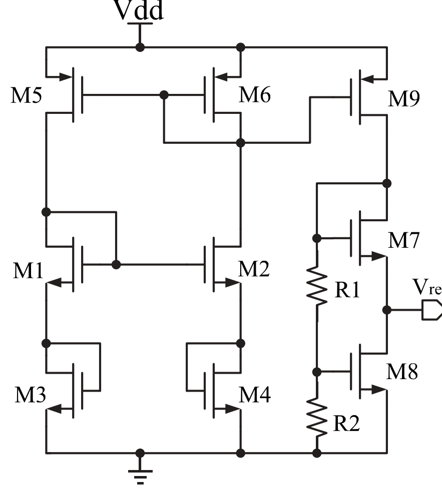


Figure 1.4: CMOS VR using resistor divider [19].

According to the principle, the nano-power CMOS voltage reference circuits are presented in [12, 13]. A characteristic structure is shown in Fig. 1.3(a). Since the CTAT term traditionally depends on V_{th}, Another method for the nano-power dissipation in VRs is using the V_{gs} of a MOS transistor operated in the saturation region as a active load [14, 15, 16], the output voltage can be expressed as

$$V_{ref} = V_{gs}. \tag{1.4}$$

The CTAT term depends on the V_{th}, the typical architecture is presented in Fig. 1.3(b). For both of two methods, the value of output voltage can be less than 1 V. However, the absolute value of V_{th} is used as the basis of the output voltage and is thus a major obstacle for the implementation of the low output voltage under threshold voltage using a standard CMOS process. When the process variations are considered, a low enough T.C. and high accuracy of V_{ref} are not sufficient because the trimming procedures are not implemented for these structures [12, 13, 14, 15, 16]. Hence, high-volume in production lines is unrealistic.

To obtain $V_{ref} < V_{th}$, resistive subdivision has been commonly used in [17, 18, 19, 20], as shown in Fig. 1.4. The output voltage can be given by

$$V_{ref} = \left(1 + \frac{R_1}{R_2}\right) V_{gs8} - V_{gs7}. \tag{1.5}$$

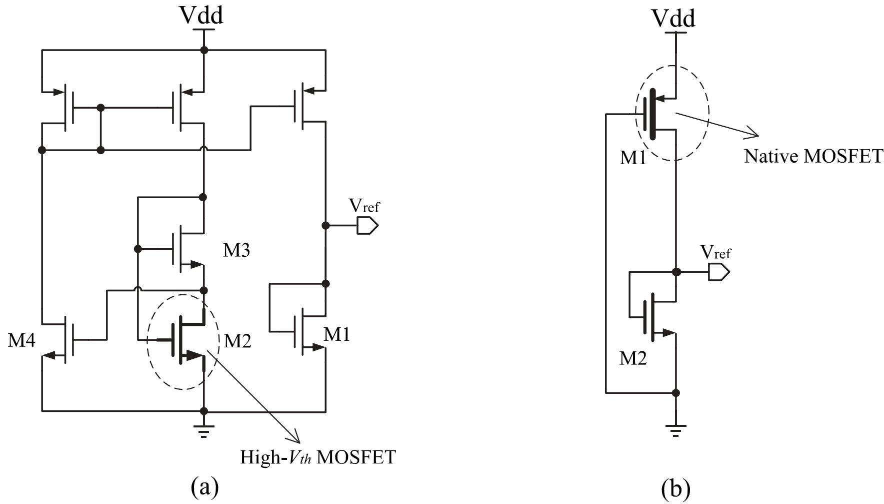


Figure 1.5: CMOS VRs based on the difference of V_{th}: (a)Reported art in [24]. (b)Reported art in [25].

These circuits can generate low output voltage by adjusting the ratio of resistors, and the trimming capacity can be implemented using the resistors network when process variations are considered. However, resistors occupy more chip area, and a trade-off between the design area and power consumption (low current requires large resistor) always exists. Therefore, operation is difficult with nano-power dissipation, and the resistor network required for trimming implementation occupies a large area of the chip.

Utilization of the difference in V_{th} is implemented to achieve the low reference voltage with low-power dissipation [21, 22, 23, 24, 25]. Because the bandgap reference source is used in [21], the output voltage is larger than the threshold voltage, and the power dissipation is still high because resistors are used. In [22], an enhancement transistor and a depletion transistor are used in the typical structure. The low-power reference voltage is lower than threshold voltage by modifying the gate oxide thickness [23], this is complex in standard CMOS process of manufacture. A nano-power CMOS VR without the resistive subdivision is discussed in [24], Fig. 1.5(a) shows the circuit. This method only uses a load transistor operated in the subthreshold region for the VR ($V_{ref} = V_{gs} < V_{th}$), but compensating for the temperature coefficient (T.C.) utilizing only one transistor

operated in the subthreshold region is complex and difficult, and the yield may be low because of the lack of a trimming procedure. An advanced approach is using the native transistor [25], as shown in Fig. 1.5(b). For these VRs that employ two devices with different V_{th} values to achieve a low output, the output voltage depends entirely on the V_{th} difference from two distinct devices. Thus, the value is constrained by the process technology chosen, the impact of process variations also increases. And the implementation of chip fabrication requires multiple-V_{th} technology, which increases the cost of production.

1.3 Research Objectives in this work

In this dissertation, the objective is on the design and development of low-power systems and circuits techniques to implement VRs for application in subthreshold circuits. Body biasing schemes, both in forward body biasing and reverse body biasing directions, are utilized to generate a low reference voltage without threshold restriction in standard CMOS process, and the power dissipation is in the range of nano-level. The output voltage has low sensitivity to the temperature and supply voltage. The trimming process can be easily implemented to ensure a low enough T.C. and accuracy of the output voltage even if the performance of VRs suffers from process variations. Special attention is paid on the combination of switched-capacitor (SC) technology and body-biasing technology for the design of VRs, which demonstrates very good and robust performance in VRs. Theoretical analysis is presented in detail, and the chip implementation is carry out and the measurement results are provided to prove the merits of the proposed VR circuits.

2

Voltage References Utilizing Body Effect in MOSFETs

In this chapter, we will introduce the basic principle of VRs using body effect in MOSFETs in detail, and the previous designs of the voltage references are presented to show the problems in the typical structures. The simple structures are provided to show some improvements.

2.1 Overview of the Design of Integrated Circuit Using MOS Body Effect

Since MOS transistor was invented, body biasing technology has been explored to improve the design of integrated circuits. Body biasing can be used for performance tuning, leakage reduction and chip area saving [26]. The adaptive body-biasing technology is gaining considerable interest for the design of minimum-energy CMOS digital circuits because the value of V_{th} can be reduced through the forward biasing connection in MOSFETs [2, 4, 9]. A low-voltage voltage-controlled oscillator (VCO) is reported in [27]. Bulk-driven technique has been applied in the design of low-voltage amplifier [28]. Few researches have been focus on the design of voltage reference by means of the body-biasing technology. In this work, the detail description about such method is presented, which is a novel design technique for low-power voltage reference.

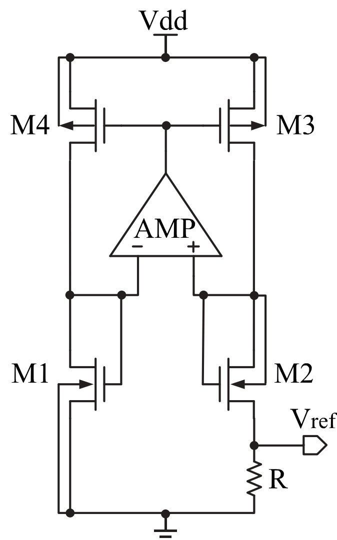


Figure 2.1: Typical structures of voltage reference using forward-biased body effects in MOSFETs [29][30].

2.2 Fundamental of Body-biased Technology for the Design of Voltage References

The methodology on how to compensate for the T.C. of a MOSFET by using body effect in MOSFETs is presented in previous work [29, 30]. Two body biasing effects are investigated, one is the forward-biased connection, anther is the reversed-biased connection. In this section, the typical structures proposed in [29, 30] are presented to explain how to implement VRs by using forward-biased body effect and reversed-biased body effect in MOSFETs, respectively.

2.2.1 VR Using Forward-biased Body Effect

The forward-biased (or self-biased) body effect is applied [29, 30], as shown in Fig. 2.1, which is based on the classic architecture. The circuits consists of transistors M1-M4, a resistor R, and amplifier. Transistors M1 and M2 work in the subthreshold region. The current mirror, composed of M3 and M4, enforces both current branches having a fixed ratio of the current. And the amplifier in closed-loop configuration is connected as a feedback, which enforces the two

inputs having equal voltage. The V_{ref} is resulted from the current flow through R. It is noticed that the substrate node of M2 is connected to its gate node, in which the substrate-source PN junction of M2 is forward-biased (self-biased) by its gate-source voltage. In this structure, two current branches and one resistor are used, the output voltage can be directly derived from the source node of M1 through such back-gate connection.

The drain current I_{dn} flown through n-channel transistor biased in the weak revision is expressed as [13]

$$I_{dn} = I_s\left(\frac{W}{L}\right)\exp\left(\frac{V_{gs}-V_{th}}{nV_T}\right)\times\left[1-\exp\left(-\frac{V_{ds}}{V_T}\right)\right], \tag{2.1}$$

$$I_s = \mu_n(n-1)C_{ox}V_T^2, \tag{2.2}$$

where W/L is the transistor aspect ratio, n is the slope factor, V_T is the thermal voltage, μ_n is the electron mobility, C_{ox} is the oxide capacitance per unit area. According to the circuit shown in Fig. 2.1, the operational principle is illustrated. For Fig. 2.1, the drain currents of M1 and M2 can be given as

$$\begin{aligned} I_{d1} &= I_s\left(\frac{W_1}{L_1}\right)\exp\left(\frac{V_{gs1}-V_{thn1}}{nV_T}\right)\times\left[1-\exp\left(-\frac{V_{gs1}}{V_T}\right)\right] \\ &= I_s\left(\frac{W_1}{L_1}\right)\left[\exp\left(\frac{V_{gs1}-V_{th1}}{nV_T}\right)-\exp\left(-\frac{(n-1)V_{gs1}+V_{th1}}{V_T}\right)\right], \end{aligned} \tag{2.3}$$

$$\begin{aligned} I_{d2} &= I_s\left(\frac{W_2}{L_2}\right)\exp\left(\frac{V_{gs2}-V_{th2}}{nV_T}\right)\times\left[1-\exp\left(-\frac{V_{gs2}}{V_T}\right)\right] \\ &= I_s\left(\frac{W_2}{L_2}\right)\left[\exp\left(\frac{V_{gs2}-V_{th2}}{nV_T}\right)-\exp\left(-\frac{(n-1)V_{gs2}+V_{th2}}{V_T}\right)\right], \end{aligned} \tag{2.4}$$

$$V_{th1} = V_{th0}, \tag{2.5}$$

$$V_{th2} = V_{th0}+\gamma(\sqrt{2\Phi_B-V_{bs2}}-\sqrt{2\Phi_B}), \tag{2.6}$$

where V_{th0} is the threshold voltage with zero biased source-substrate voltage, γ is the substrate back-bias factor, Φ_B is the bulk Fermi potential, and V_{bs2} is the

source-substrate voltage. Due to $n > 1$, $(n-1)V_{gsx}(x=1,2) + V_{thx}(x=1,2) >> V_T$. Thus, Eqs. (3.7) and (3.8) can be approximated as

$$I_{d1} = I_s \left(\frac{W_1}{L_1}\right) \exp\left(\frac{V_{gs1} - V_{th1}}{nV_T}\right), \tag{2.7}$$

$$I_{d2} = I_s \left(\frac{W_2}{L_2}\right) \exp\left(\frac{V_{gs2} - V_{th2}}{nV_T}\right). \tag{2.8}$$

The ratio between I_{d1} and I_{d2} is equal to the size proportion between M3 and M4, then

$$\frac{I_{d1}}{I_{d2}} = \frac{W_4/L_4}{W_3/L_3}. \tag{2.9}$$

With Eqs. (2.5)(2.6)(2.7)(2.8) and (2.9), V_{ref} can be presented by

$$\begin{aligned} V_{ref} &= V_{gs1} - V_{gs2} \\ &= \gamma(\sqrt{2\Phi_B} - \sqrt{2\Phi_B - V_{bs2}}) + nV_T lnK, \end{aligned} \tag{2.10}$$

where

$$K = \frac{\left(\frac{W}{L}\right)_2 \left(\frac{W}{L}\right)_4}{\left(\frac{W}{L}\right)_1 \left(\frac{W}{L}\right)_3}. \tag{2.11}$$

From Fig. 2.1, $V_{bs2} = V_{gs2}$, substitute it into Eq. (2.10). Hence, considering the temperature dependence of V_{gs2}, Φ_B and V_T, differentiating Eq. (2.10) with respect to temperature T gives

$$\begin{aligned} \frac{\partial V_{ref}}{\partial T} = \frac{1}{2}\gamma \Bigg[(2\Phi_B)^{-\frac{1}{2}} \left(2\frac{\partial \Phi_B}{\partial T}\right) - (2\Phi_B - V_{gs2})^{-\frac{1}{2}} \\ \left(2\frac{\partial \Phi_B}{\partial T} - \frac{\partial V_{gs2}}{\partial T}\right)\Bigg] + n\frac{V_T}{T} ln(K). \end{aligned} \tag{2.12}$$

The simple relationship between the surface potential and the gate-source voltage in the subthreshold region is given by [31]

$$V_{gs2} \approx V_{th2} + n(T)[\Phi_S(T) - 2\Phi_B(T)], \tag{2.13}$$

where Φ_S is the surface potential. The temperature model of the threshold voltage can be expressed as [31]

$$V_{th2} = V_{th2}(T_0) + (K_{t1} + K_{t2}V_{bs2})\left(\frac{T}{T_0}\right). \tag{2.14}$$

where $V_{th2}(T_0)$ is the threshold voltage value at T_0 (room temperature), K_{t1} is the T.C. for threshold voltage, and K_{t2} is the body-bias coefficient of the V_{th2} temperature effect. The quantity for $\Phi_S(T) - 2\Phi_B(T)$ as a function of the temperature results

$$\Phi_S(T) - 2\Phi_B(T) = [\Phi_S(T_0) - 2\Phi_B(T_0)]\frac{T}{T_0}, \tag{2.15}$$

assuming that n has little sensitivity to the temperature [18].

Substituting $V_{bs2} = V_{gs2}$, Eqs. (2.14) and (2.15) into Eq. (2.13) and differentiating Eq. (2.13) with respect to temperature and denote that

$$K_{gs2} = \frac{\partial V_{gs2}}{\partial T} \approx \frac{n(T_0)[\Phi_S(T_0) - 2\Phi_B(T_0)] + K_{t1} + K_{t2}V_{gs2}}{T_0[1 - K_{t2}\left(\frac{T}{T_0} - 1\right)]}. \tag{2.16}$$

In the subthreshold region, it is known that $\Phi_B < \Phi_S < 2\Phi_B$, and it is assumed that the typical values of K_{t1} and K_{t2} in [29, 30] are -0.11 and 0.022, respectively. $[1 - K_{t2}(\frac{T}{T_0} - 1)] > 0$ with temperature range. Transistor M2 works in the subthreshold region. In [29, 30], the values of V_{gs2} and $n(T_0)$ are approximately 0.3 V and 2, respectively. Therefore, the V_{gs2} has a negative T.C. ($K_{gs2} < 0$) [29, 30].

The expression of $\Phi_B(T)$ can be given by [18]

$$\Phi_B(T) = \Phi_B(T_0)\frac{T}{T_0} - \frac{3kT}{2q}ln\left(\frac{T}{T_0}\right) + \frac{E_g(T)}{2q} - \frac{E_g(T)}{2q}\frac{T}{T_0}, \tag{2.17}$$

where E_g is the energy gap of the silicon, can be expressed as [18]

$$E_g(T) = 1.16 - \frac{702x10^{-6}}{T + 1108}T^2. \tag{2.18}$$

Differentiating of Eq. (2.20) with respect to temperature T and denoting that

$$\begin{aligned} K_B = \frac{\partial \Phi_B(T)}{\partial T} = \frac{\Phi_B(T_0)}{T_0} - \frac{3k}{2q}ln\left(\frac{T}{T_0}\right) - \frac{3k}{2q} \\ -702x10^{-6}\frac{T^2 + 2216T}{2q(T + 1108)^2} - \frac{E_g(T_0)}{2qT_0}. \end{aligned} \tag{2.19}$$

$\Phi_B(T_0)$ can be calculated by [18]

$$\Phi_B(T_0) = \frac{kT_0}{q}ln\left[\frac{N_{CH}}{n_i(T_0)}\right], \tag{2.20}$$

where N_{CH} is channel doping concentration, and $n_i(T)$ is the intrinsic carrier concentration. With Eqs. (2.19) and (2.20), the value of K_B can be gotten ($\approx$ -0.7 mV/°C [29, 30]). And the T.C. of V_{gs} is negative. Hence, the first term of Eq.(3.14) has a negative T.C..

To get a zero T.C. of V_{ref} at the room temperature T_0, Eq. (3.14) must be satisfied by

$$\frac{\partial V_{ref}}{\partial T} \mid_{T=T_0} = 0. \tag{2.21}$$

Thus, K can be calculated by

$$K = \exp\left\{ \frac{\gamma T}{2nV_T} \left[\frac{2\partial\Phi_B/\partial T - \partial V_{gs1}/\partial T}{\sqrt{2\Phi_B(T_0) - V_{gs1}(T_0)}} - \frac{2\partial\Phi_B/\partial T}{\sqrt{2\Phi_B(T_0)}} \right] \right\}. \tag{2.22}$$

From Eq. (2.34), the size ratio between M1 and M2 and the size ratio between M3 and M4 can be selected to get a zero T.C..

It is noticed that the source-substrate junction of M2 is forward biased. Hence, the threshold of M2 is reduced. Thanks to the subthreshold operation in M2, and turning on the PN junction it is avoided.

2.2.2 VR Using Reversed-biased Body Effect

The revised-biased connection in MOSFETs also can be used to implement the voltage reference circuit, Fig. 2.2 illustrates the typical structure. The circuit is composed of MOSFETs M1-M4, Md1 and Md2 and one resistor R. Transistors M1, M2, Md1 and Md2 are operated in the subthreshold region and have the diode connection. The current mirror composed of M3 and M4 determines the fixed ratio of the current in both current branches. And the amplifier in closed-loop configuration is connected as a feedback to enforce the two inputs having equal voltage. The V_{ref} is resulted from the current flow through R. It is noticed that the substrate nodes of all MOSFETs are connected to their source nodes except M1. The substrate-source PN junction of M1 is reversed-biased by Md1. For the P-channel transistor in the subthreshold region, the drain current I_{dp} is expressed as

$$I_{dp} = I_t \left(\frac{W}{L}\right) \exp\left(\frac{V_{gs} - V_{th}}{nV_T}\right) \times \left[1 - \exp\left(-\frac{V_{ds}}{V_T}\right)\right], \tag{2.23}$$

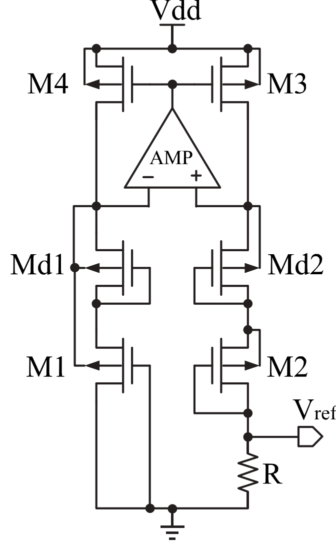


Figure 2.2: Typical structures of voltage reference using reversed-biased body effects in MOSFETs [30].

$$I_t = \mu_p(n-1)C_{ox}V_T^2, \tag{2.24}$$

where μ_p is the hole mobility. Then, the drain currents of M1 and M2 can be given by

$$I_{d1} = I_t\left(\frac{W_1}{L_1}\right)\exp\left(\frac{V_{sg1}-V_{th1}}{nV_T}\right), \tag{2.25}$$

$$I_{d2} = I_t\left(\frac{W_2}{L_2}\right)\exp\left(\frac{V_{sg2}-V_{th2}}{nV_T}\right), \tag{2.26}$$

$$V_{th1} = V_{th0} + \gamma(\sqrt{2\Phi_B + V_{bs1}} - \sqrt{2\Phi_B}), \tag{2.27}$$

$$V_{th2} = V_{th0}. \tag{2.28}$$

The V_{ref} can be provided as

$$\begin{aligned} V_{ref} &= V_{sg1} - V_{sg2} \\ &= \gamma(\sqrt{2\Phi_B + V_{bs1}} - \sqrt{2\Phi_B}) + nV_T lnK, \end{aligned} \tag{2.29}$$

$$K = \frac{\left(\frac{W}{L}\right)_2 \left(\frac{W}{L}\right)_4}{\left(\frac{W}{L}\right)_1 \left(\frac{W}{L}\right)_3}. \tag{2.30}$$

From Fig. 2.2, $V_{bs2} = V_{sgd1}$, V_{sgd1} can be expressed as [18]

$$V_{sgd1} = V_{th}(T_0) + K_{d1}\left(\frac{T}{T_0} - 1\right). \tag{2.31}$$

K_{d1} is the T.C. of V_{sgd1} and has a negative value. Hence, considering the temperature dependence of V_{sgd1}, Φ_B and V_T, differentiating Eq. (2.29) with respect to temperature T gives

$$\frac{\partial V_{ref}}{\partial T} = \frac{1}{2}\gamma\left[(2\Phi_B + V_{sgd1})^{-\frac{1}{2}}\left(2\frac{\partial \Phi_B}{\partial T} + \frac{\partial V_{sgd1}}{\partial T}\right) - (2\Phi_B)^{-\frac{1}{2}}\left(2\frac{\partial \Phi_B}{\partial T}\right)\right] + n\frac{V_T}{T}ln(K). \tag{2.32}$$

According to the analysis in section 2.2.1, the term in the brackets is a negative value. Thus, a zero T.C. can be achieved by selecting an appropriate ratio of M1, M2, M3 and M4.

2.3 Improved Structure of Voltage Reference Using Self-biased MOS Body Effect

According to Eqs. (2.10) and (2.29), the absolute value of V_{ref} is lower than that of V_{th0} because V_{th0} cancel each other. The body effect is utilized to modify the threshold voltage of a MOSFET to get an appropriate quantity of V_{ref}. The T.C. of a MOSFET with body effect can be modified. The biased voltage between source and substrate node is a dynamic voltage varying with temperature. However, the typical structures have the following drawbacks: the low current requires a large resistor, the supply current remains large (1.2 μA in Fig. 2.2); and the output suffers from the offset of the amplifier; the T.C. and the accuracy of V_{ref} are degraded when the value of the resistor varies with the process, the large resistor occupies more chip area; the output voltage and the T.C. are subject to component mismatches and deviations resulting from process variations; the deviations and the mismatches are not well discussed, and the trimming procedures are not considered. Hence, improvements are essential to these designs.

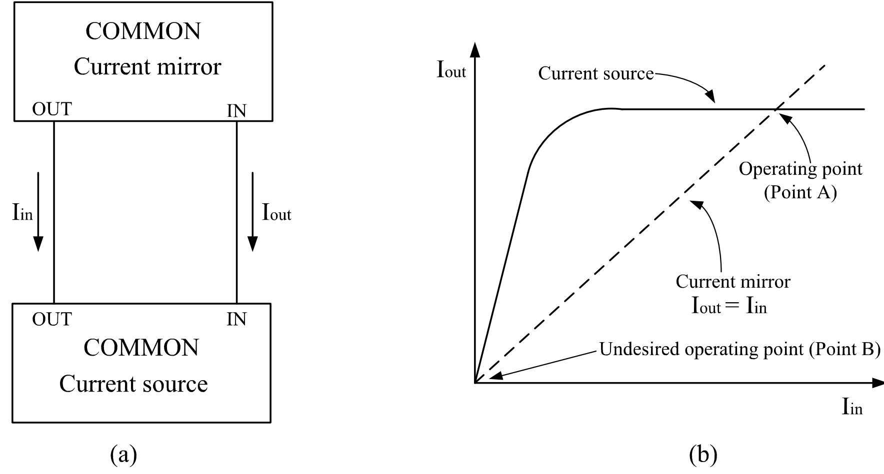


Figure 2.3: (a)Block diagram of a self-biased reference. (b)Determination of operating point.

2.3.1 Introduction of Self-biased Structure

Self-biased structure is a well-known circuit [11], which can make the current have low sensitivity to the supply voltage. A current reference is implemented based on the structure [32] in which the self-biased technique is used. Fig. 2.3(a) shows the concept. Assuming that the feedback loop formed by this connection has a stable operating point, the currents flowing in the circuit are less sensitive to power-supply voltage than in the resistive biased case. The current source and the current mirror define the relationship between the input current I_{in} and the output current I_{out}. From the standpoint of the current source, the output current is almost independent on the input current for a wide range of input current, as shown in Fig. 2.3(b). From the standpoint of the current mirror, I_{in} is set equal to I_{out}, assuming that the gain of the current mirror is unity. The operating point of the circuit must satisfy both constrains and hence is at the intersection of the two characteristics. The desired point (point A) is illustrated in Fig. 2.3(b). Point B is an undesired operating point because $I_{out} = I_{in} = 0$. In essence, I_{in} is "bootstrapped" to I_{out}. Hence, I_{in} and I_{out} have little dependence on power supply.

If the output current in Fig. 2.3(a) increases, the current mirror increases

the input current by the same amount because the gain of the current mirror is assumed to be unity. As a result, the current source increases the output current by an amount that depends on the gain of the current source. Therefore, the loop responds to an initial change in the output current by further changing the output current in a direction that reinforces the initial change. In other words, the connection of a current source and a current mirror as shown in Fig. 2.3(a) forms a positive feedback loop, and the gain around the loop is the gain of the current source. At point A, the gain around the loop is quite small because the output current of the current source is insensitive to changes in the input current around point A. On the other hand, at point B, the gain around the feedback loop is deliberately made greater than unity so that the two characteristics shown in Fig. 2.3(b) intersect at a point away from the origin. As a result, this simplified analysis shows that point B is an unstable operating point in principle, and the circuit would ideally tend to drive itself out of this state.

An important issue in supply-independence biasing is the existence of "degenerate" bias shown in point B in Fig. 2.3(b). Point B is frequently a stable operating point because the currents in the transistors at this point are very small (in the pico-ampere). At such low current levels, leakage currents and other effects reduce the current gain of transistors, usually causing the gain around the loop to be less than unity. As a result, actual circuits of this type are usually unable to drive themselves out of the zero-current state. Thus, unless precautions are taken, the circuit may operate in the zero-current condition. For these reasons, self-biased circuits often have a stable state in which zero current flows in the circuit even when the power-supply voltage is nonzero. To resolve this issue, a mechanism that drives the circuit out of the degenerate bias point when the supply is turn on is added. Thus, a start-up circuit is usually required.

2.3.2 Proposed Voltage Reference Circuits

Combining the supply-independence mechanism and body effect in MOSFETs, a improved scheme by which a VR can be implemented is presented in Fig. 2.4 [33]. The circuit is composed of several MOSFETs and one resistor. All transistors work in the subthreshold region. The output voltage (V_{ref}) is the gate-source

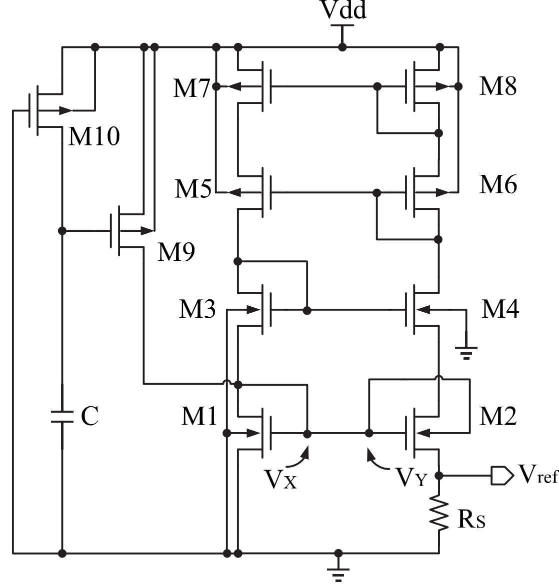


Figure 2.4: Proposed voltage reference.

voltage difference between M1 and M2. It is noticed that the substrate node of M2 is connected to its gate node, which constructs a forward-biased substrate-source PN junction. This circuit has only two current branches and only one resistor, the reference voltage can be directly derived from the source node of M2 with such back-gate connection. Instead of the operational amplifier used in Fig. 2.3, the self-biased structure as the cascode stacks, consists of transistors M3−M8, makes sure that $V_X = V_Y$. And each branch can employ both NMOS and PMOS cascode topology, which can achieve high output impedance and high accuracy of the current ratio between two branches [11]. The V_{ref} has a better power supply rejection ratio to reduce the sensitivity to the supply voltage. Transistors M9, M10 and capacitor C compose the startup circuit to avoid the undesired bias point where all currents are equal to zero. Assuming the ratio between M7 and M8 is the same as that between M5 and M6, M3 and M4, V_{ref} is expressed as

$$\begin{aligned} V_{ref} &= V_{gs1} - V_{gs2} \\ &= \gamma(\sqrt{2\Phi_B} - \sqrt{2\Phi_B - V_{bs2}}) + nV_T lnK, \end{aligned} \tag{2.33}$$

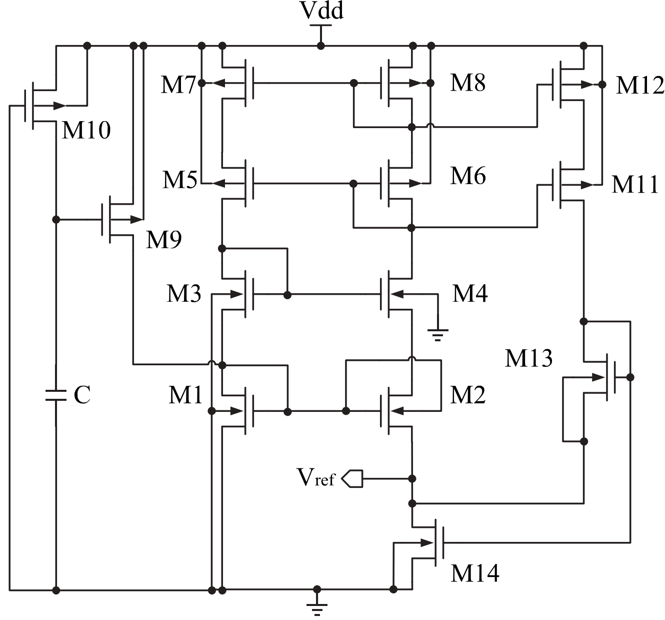


Figure 2.5: Proposed voltage reference without resistor.

where

$$K = \frac{\left(\frac{W}{L}\right)_2 \left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_1 \left(\frac{W}{L}\right)_8}. \tag{2.34}$$

The drawback of such structure is the resistor. If a low current is required, a high value resistance is needed, which takes a large surface area. And the resistivity is not guaranteed by some foundries and can vary with technology. And the T.C. of resistor also suffers from process variations. A solution is the usage of the active load. Self-cascode MOSFET (SCM) structure biased in strong inversion can be used to implement an active load [34, 35]. In our design, the method is used to modify the design of Fig. 2.4 to remove the resistor. Illustrated in Fig. 2.5 [33], all MOSFETs are operated in the subthreshold region except for M14 and M13. M14 works in the deep-triode region as a MOS resistor instead of the ordinary resistor in Fig. 2.4 and M13 is operated in the saturation region, which configures the SCM. The minimum supply voltage is limited in practice by the strong inversion condition of M13 and M14 and can be expressed as

$$V_{dd} \geq V_{ds14} + V_{gs13} + V_{ds11} + V_{ds12}. \tag{2.35}$$

2.3.3 Simulation Results and Comparison

The proposed circuit in Fig. 2.5 is designed in a 0.18-μm CMOS technology. Fig. 2.6 shows simulation results of the output reference voltage as a function of temperature while the supply voltage is 2 V. The average of output voltage V_{ref} is approximately 243 mV. The temperature variation was approximately 0.36 mV in a temperature range from −25°C ∼ 80 °C, the corner analysis results are shown in Table. 2.1 where TT is typical PMOS/typical NMOS, SS is slow PMOS/slow NMOS, FS is fast PMOS/slow NMOS, SF is slow PMOS/fast NMOS, FF is fast PMOS/fast NMOS. The typical T.C. is 14.8 ppm/°C.

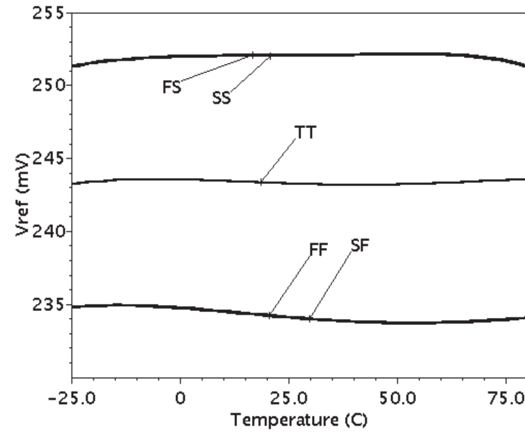


Figure 2.6: Temperature dependence of V_{ref} at different corners.

Table 2.1: Corner analysis results

Type	T.C.	V_{ref}
TT	14.8 ppm/°C	243.24 mV
SS	34.0 ppm/°C	252.03 mV
FS	34.0 ppm/°C	252.03 mV
FF	48.8 ppm/°C	234.10 mV
SF	48.8 ppm/°C	234.10 mV

Fig. 2.7 illustrates the output voltage V_{ref} at room temperature as a function of supply voltage, the voltage sensitivity is low, 0.0019%/V. The circuits operated correctly when supply voltage is higher than 1.4 V. Fig. 2.8 shows the power supply rejection ratio (PSRR) at room temperature. The PSRR at 100Hz is approximately -112 dB. Fig. 2.9 shows the layouts of the proposed design. The layout areas is 0.014 mm^2 (140 μm $\times$100 μm). The output voltage V_{ref} lower than threshold voltage of MOSFETs, the proposed circuits have perfect performance in terms of temperature insensibility and supply insensibility and occupy a minimum chip area. The supply current is about 1 μA at room temperature.

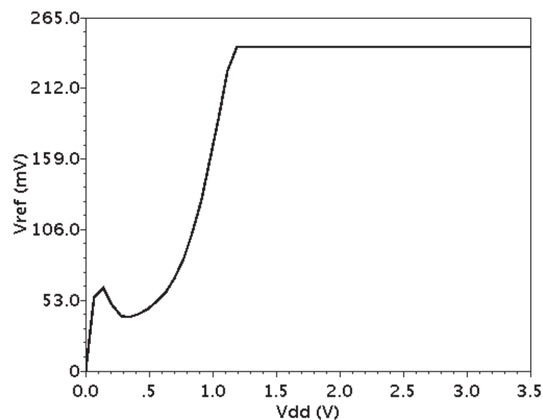


Figure 2.7: V_{ref} as a function of supply voltage.

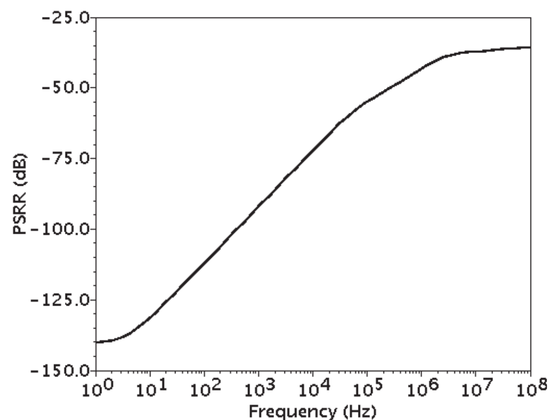


Figure 2.8: The PSRR result in Fig. 2.5.

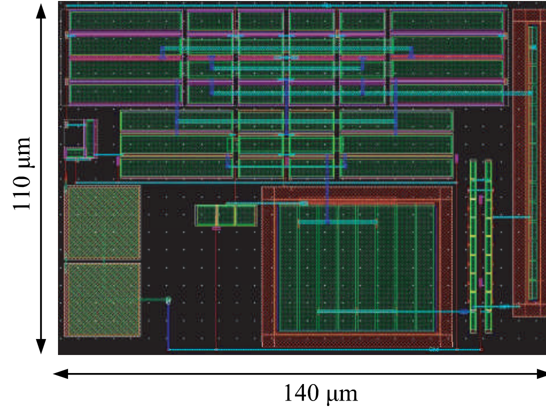


Figure 2.9: Layout of proposed circuit in Fig. 2.5.

Table 2.2 shows characteristics of our proposed devices in comparison with other reported low-power low-voltage reference. It can be noted that the output voltage V_{ref} in the all circuits is lower than threshold voltage of MOSFETs, the proposed circuit has perfect performance in terms of temperature insensibility and supply insensibility, and occupies the smallest of the chip area. Moreover, the circuit can be implemented without the special requirements in process for devices. And the supply current is approximately 1 μA.

2.3.4 Conclusion

Based on the self-biased architecture, low-power low-voltage reference has been proposed by using forward-biased body effect. The simulation result in a standard CMOS 0.18 μm technology illustrates that the variation of the output voltage is small at a temperature range from -25°C $\sim$ 80°C by adjusting the T.C. of a MOSFET with body effect, the typical T.C. is 14.8 ppm/°C. The line sensitivity is approximately 0.0019 %/V. The power dissipation at 1.4 V supply voltage is 1.4 μW. Thanks to the only two current branches in the proposed circuits, the design areas are small, approximately 0.014 mm^2.

Table 2.2: Comparison with other low-voltage low-power voltage reference.

	This work	Ref.[24]	Ref.[23]	Ref.[30]	Ref.[19]	Ref.[20]
Process	0.18 μm	0.18 μm	0.35 μm	0.35 μm	0.35 μm	0.18 μm
V_{th}-NMOS V_{th}-PMOS	0.45 V -0.383 V	0.32 V -0.456 V	0.605 V, 0.658 V 0.812 V	0.5 V -0.65 V	0.9 V -0.9 V	0.77 V -1.05 V
Supply voltage (V)	1.4 to 3.5	0.45 to 2.0	1.1 to 4.0	0.95 to 3.3	1.5 to 4.3	0.85 to 2.5
Supply current (μA) @ room temperature	1 @ 1.4 V	0.007 @ 1 V	0.021 @ 1.1 V vers-1 0.023 @ 1.1 V vers-2	1.2 @ 0.95 V	1.2 @ 1.5 V	3.882 @ 0.85 V
Vref (mV)	243.24	257.5	96.6,vers-1 108.9,vers-2	181	168	221
T.C. (ppm/°C) Temp range (°C)	14.8 (typical) -25 to 80	165 0 to 125	11.4 [-20 80],vers-1 9.2 [-20 80],vers-2	11 (typical) -40 to 100	25 0 to 80	194 -20 to 120
Line sensibility (%/V)	0.0019	0.44	0.09,vers-1 0.17,vers-2	0.199	0.95	0.905
PSRR (dB) @ 100 Hz	-112	-45	<-60,vers-1 <-40,vers-2	-	-65	-
Chip area (mm^2)	0.014	0.043	0.0189,vers-1 0.0193,vers-2	-	0.08	0.0238
Resistive subdivision	No	No	No	No	Yes	Yes
Trimming capacity	-	-	-	-	Resistors	Resistors
Requirements for devices	No	High-V_{th}	Gate-oxide thickness	No	No	No

3

Self-cascode MOSFET with a Self-biased Body Effect for Ultra-low-power Voltage Reference Generator

This chapter proposes a novel approach for implementing an ultra-low-power voltage reference using the structure of self-cascode MOSFET, operating in the subthreshold region with a self-biased body effect [36]. The difference between the two gate-source voltages in the structure enables the voltage reference circuit to produce a low output voltage below the threshold voltage. The circuit is designed with only MOSFETs and fabricated in standard 0.18-μm CMOS technology. Measurements show that the reference voltage is about 107.5 mV, and the temperature coefficient is about 40 ppm/°C, at a range from -20 °C to 80 °C. The voltage line sensitivity is 0.017 %/V. The minimum supply voltage is 0.85 V, and the supply current is approximately 24 nA at 80 °C. The occupied chip area is around 0.028 mm^2.

3.1 Introduction

In the previous chapter, a voltage reference using MOS body effect is implemented based on the schematic of self-biased current mirror. However, the power dissipa-

tion cannot be in the nano-power range, and the output voltage suffers more from the mismatches of transistors. The resistive or active load varying with temperature and process also degrades the performance of voltage reference. According to Fig. 2.6, the trimming work is necessary for the zero T.C. and accuracy of V_{ref}. However, it is difficult for implementing the trimming procedures because the operation of T.C. compensation requires the match of more transistors, and the value of load is not constant.

The cascode structure in current mirror operated in the subthreshold region is widely used in MOS technology, where the effect of channel-length modulation is suppressed and the output impedance is enhanced [11]. In case the same gate bias for both transistors is used, it is called a self-cascode structure. As aforementioned in chapter 2, the structure is also named the self-cascode MOSFET (SCM). Fig. 3.1 shows the configuration. Mb works in the triode region as a resistor whose value is input dependent, while Ma is operated in the saturation region. The voltage between source and drain of Ma is small, and there is no appreciable difference between the V_{gsa} of composite and simple transistors; and the self-

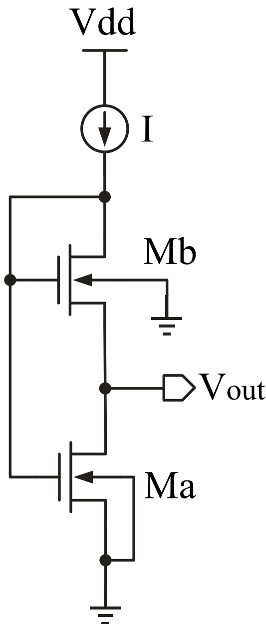


Figure 3.1: Self-cascode structure.

cascode can be used in low voltage operation.

The SCM structure operated in the subthreshold region is used for the PTAT reference [35, 37], which is independent of the current level and process. According to Eq. (2.1), the drain current of Ma is expressed as

$$I_{da} = I_s \left(\frac{W_a}{L_a}\right) \exp\left(\frac{V_{gsa} - V_{tha}}{nV_T}\right) \times \left[1 - \exp\left(-\frac{V_{out}}{V_T}\right)\right]. \quad (3.1)$$

For Mb, from Eqs. (2.7) and (2.8), the drain current of Mb is given by

$$I_{db} = I_s \left(\frac{W_b}{L_b}\right) \exp\left(\frac{V_{gsb} - V_{thb}}{nV_T}\right). \quad (3.2)$$

And $I_{da} = I_{db} = I$, $V_{gsb} = V_{gsa} - V_{out}$. From Eqs. (3.1) and (3.2), neglecting body effect in V_{thb} and solving for V_{out} results in

$$V_{out} \approx nV_T ln\left(\frac{W_b/L_b}{W_a/L_a}\right). \quad (3.3)$$

V_{out} presents a linear temperature dependence due to the logarithmic dependence of V_{out} on the size ration between Ma and Mb, which is useful for realizing PTAT generator.

A novel all-CMOS VR based on the self-cascode MOSFET (SCM) structure with a self-biased body effect is proposed in this chapter. The circuit, operated in the subthreshold region, consumes nano-power dissipation and generates a output voltage with low sensitivity to the temperature and supply voltage. The low reference voltage ($< V_{th}$) and the trimming procedure can be implemented without requiring integrated resistors, thus minimizing the chip occupation. The chapter is organized as follows: Section 3.2 describes and analyzes the operation principle. Section 3.3 presents the proposed VR circuit. Section 3.4 gives the design considerations. Section 3.5 gives the measurement results and compares them. Finally, Section 3.6 is the conclusion.

3.2 Operation Principle of the Proposed VR

The structure using the self-biased body effect can achieve not only the PTAT but also the CTAT for the VR generator. Fig. 3.2 shows the principle of the

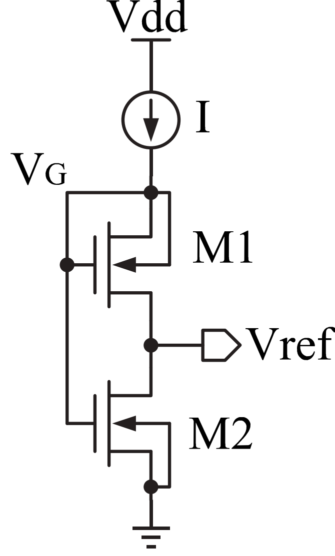


Figure 3.2: Scheme of principle of proposed VR in this study.

proposed circuit. The structure is presented by the current source and the SCM which consists of M1 and M2. Notably, the body of M1 is connected to its gate. With a ultra-low current supply, M1 and M2 are biased in the weak inversion region. According to the subthreshold model illustrated in Eq. (2.1), the drain current I_{d1} of M1 can be expressed as

$$\begin{aligned} I_{d1} = I_s \left(\frac{W_1}{L_1}\right) \exp\left(\frac{V_G - V_{th1} - V_{ref}}{nV_T}\right) \\ \times \left[1 - \exp\left(-\frac{V_G - V_{ref}}{V_T}\right)\right] \\ = I_s \left(\frac{W_1}{L_1}\right) \left\{\exp\left(\frac{V_G - V_{th1} - V_{ref}}{nV_T}\right)\right. \\ \left. - \exp\left[-\frac{(n-1)(V_G - V_{ref}) + V_{th1}}{nV_T}\right]\right\}, \end{aligned} \tag{3.4}$$

$$I_s = \mu_n (n-1) C_{ox} V_T^2, \tag{3.5}$$

$$V_{th1} = V_{th0} + \gamma(\sqrt{2\Phi_B - V_{bs1}} - \sqrt{2\Phi_B}). \tag{3.6}$$

For the second term in the square brackets in Eq. (3.4), $(n-1)(V_G - V_{ref}) + V_{th1} \gg nV_T$ and $1 < n < 2$, so Eq. (3.4) can be given by

$$I_{d1} = I_s \left(\frac{W_1}{L_1}\right) \exp\left(\frac{V_G - V_{th1} - V_{ref}}{nV_T}\right). \tag{3.7}$$

The drain current I_{d2} can be presented as

$$I_{d2} = I_s \left(\frac{W_2}{L_2}\right) \exp\left(\frac{V_G - V_{th2}}{nV_T}\right) \times \left[1 - \exp\left(-\frac{V_{ref}}{V_T}\right)\right]. \tag{3.8}$$

Given that $I_{d1} = I_{d2} = I$, from Eqs. (3.7) and (3.8), V_{ref} can be expressed as

$$V_{ref} = V_T ln\left\{\frac{W_1/L_1}{W_2/L_2} \times \exp\left[\frac{V_{th2} - V_{th1} + (n-1)V_{ref}}{nV_T}\right] + 1\right\}. \tag{3.9}$$

In M1, the body bias is forward ($V_{bs1} > 0$), so $V_{th2} > V_{th1}$ according to Eq. (3.6). If $(W_1/L_1) \gg (W_2/L_2)$, Eq. (3.9) can be approximated as

$$V_{ref} = V_T ln\left\{\frac{W_1/L_1}{W_2/L_2} \times \exp\left[\frac{V_{th2} - V_{th1} + (n-1)V_{ref}}{nV_T}\right]\right\}. \tag{3.10}$$

With $V_{bs1} = V_{gs1}$ and $V_{th2} = V_{th0}$, substituting Eq. (3.6) into Eq. (3.10) yields mathindent=0mm

$$V_{ref} = nV_T ln(K) + \gamma(\sqrt{2\Phi_B} - \sqrt{2\Phi_B - V_{gs1}}), \tag{3.11}$$

$$K = \frac{W_1/L_1}{W_2/L_2}. \tag{3.12}$$

The T.C. of V_{ref} can be given by

$$\frac{\partial V_{ref}}{\partial T} = n\frac{V_T}{T} ln(K) + \frac{1}{2}\gamma \left[(2\Phi_B)^{-\frac{1}{2}} \left(2\frac{\partial \Phi_B}{\partial T}\right)\right. \tag{3.13}$$

$$\left. -(2\Phi_B - V_{gs1})^{-\frac{1}{2}} \left(2\frac{\partial \Phi_B}{\partial T} - \frac{\partial V_{gs1}}{\partial T}\right)\right], \tag{3.14}$$

where the first term can achieve a positive value, whereas the second term in the square brackets has a negative value. Thus, in Eq. (3.11), the first term is the PTAT that has positive T.C., whereas the second term is the CTAT that has negative T.C.. Hence, V_{ref} can achieve the low sensitivity to temperature

by selecting an adaptive size ratio K between M1 and M2. This phenomenon is analyzed in detail in Section 3.

From Eqs. (3.11) and (3.14), V_{ref} can be approximated as the gate-source voltage difference between M1 and M2, the CTAT term is achieved based on two MOSFETs with distinct threshold voltage levels: one without body effect and another with the body effect (V_{gs1} is used as the biased voltage for the body effect in the transistor to change the value of V_{th0}). As a result, V_{th0} values cancel each other, and the absolute value of V_{ref} is lower than that of V_{th0}. And the supply current only requires nano-level amperes.

3.3 Structure of the Proposed VR

Fig. 3.3 shows the proposed VR circuit. The structure consists of the start-up, biased-current and core circuits. Table 3.1 shows the component values.

The start-up circuit comprises transistors M7 to M10 and capacitor C, as shown in Fig. 3.3. As the supply voltage increases, M7 operates as a high-impedance load that is always on, and the capacitor C is charged slowly because of the large value of the capacitor. In the event that the gate of M8 is pulled low, M8 turns off while M9 turns on, the gate of M10 is pulled high, then M10 turns on, the transistor injects currents into the biased-current circuit. Once the voltage in C is sufficient to turn M8 on, the gate of M10 is pulled low and turns off, such that the start-up circuit no longer affects the biased-current circuit.

The biased-current circuit [38] generates the current to be injected in the core circuit, and the cascode current mirror ensures that the generated current is independent of the supply voltage. All MOSFETs are operated in the subthreshold region except M5 and M6. The transistor M5 must work in the deep-triode region as an MOS resistor, and the transistor M6 must be operated in the saturation region to bias M5. Thus the biased current I_P can be presented by [39]

$$I_P = 2\mu_n C_{ox}(nV_T)^2 \frac{(W_5/L_5)^2}{W_6/L_6} \left[ln\left(\frac{W_4/L_4}{W_3/L_3}\right)\right]^2, \tag{3.15}$$

where W_x/L_x (x = 3,4,5,6) is the transistor aspect ratio. The T.C. of I_p can be

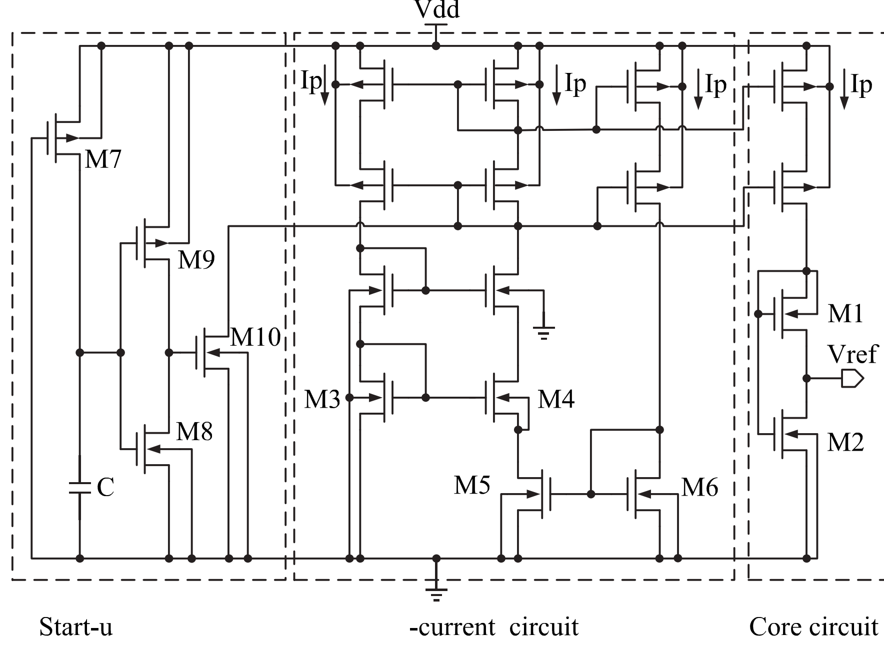


Figure 3.3: Proposed CMOS voltage reference circuit.

Table 3.1: Component values of the proposed VR circuit

Transistor	Value (W/L)
M_1	280 μm / 5 μm = (28 μm / 5 μm) $\times$ 10
M_2	20 μm / 5 μm
M_3	50 μm / 5 μm = (5 μm / 5 μm) $\times$ 10
M_4	220 μm / 5 μm = (5 μm / 5 μm) $\times$ 44
M_5	1.7 μm / 280 μm
M_6	1 μm / 280 μm
M_7	2 μm / 20 μm
M_8	5 μm / 2 μm
M_9	2 μm / 2 μm
M_{10}	4 μm / 2 μm
C	1.2 pF

given by

$$\frac{1}{I_P}\frac{\partial I_P}{\partial T} = \frac{2-m}{T}, \tag{3.16}$$

where m (≈ 1.5) is the mobility temperature exponent. The nano-ampere reference current can be obtained by choosing the sizes of M3 to M6. Therefore, the core circuit driven by the current I_P can work in the subthreshold region. By substituting Eq. (4.8) and Eq. (3.15) into Eq. (3.7), V_{gs1} can be expressed as

$$V_{gs1} = V_G - V_{ref} = V_{th1} + nV_T ln(M), \tag{3.17}$$

$$M = \frac{2n^2(W_5/L_5)^2}{(W_1/L_1)(W_6/L_6)(n-1)}\left[ln\left(\frac{W_4/L_4}{W_3/L_3}\right)\right]^2 \tag{3.18}$$

Eqs. (3.17) and (3.18) show that the T.C. of the biased current I_P in V_{gs1} has been canceled. The temperature modeling of the threshold voltage is then considered as [31]

$$V_{th1}(T) = V_{th1}(T_0) + (K_1 + K_2V_{bs1})\left(\frac{T-T_0}{T_0}\right), \tag{3.19}$$

where $V_{th1}(T_0)$ is the threshold voltage at room temperature ($T_0 = 300$ K), K_1 is the T.C. (-0.23 V in this technology) for the threshold voltage, and K_2 (≈ 0.022) is the body-bias coefficient of the threshold voltage temperature effect. Given that $V_{bs1} = V_{gs1} \approx 0.2$ V in this work, the term K_2V_{bs} can be neglected. By differentiating V_{gs1} with respect to the temperature and assuming n has small variations with temperature, Eq. (3.17) can be given by

$$K_G = \frac{\partial V_{gs1}}{\partial T} = \frac{\partial V_{th1}}{\partial T} + n\frac{V_T}{T}ln(M), \tag{3.20}$$

K_G is the T.C. of V_{gs1}. We assume that the value of n is approximately 1.2, and the T.C. of V_T is about 0.087 mV/°C [11]. Thus, by calculating Eq. (3.20) with Eq. (3.19) and the sizes in Table 3.1, K_G is about -1.3 mV/°C.

The T.C. of Φ_B is about -0.7 mV/°C in this process, so the second term in the square bracket in Eq. (3.14) has a negative T.C.. To have a zero T.C. output voltage, the following condition must be satisfied:

$$\frac{\partial V_{ref}}{\partial T}\mid_{T=T_0} = 0. \tag{3.21}$$

From Eqs. (3.12)and (3.14), the size ratio K between M1 and M2 can be chosen to obtain a zero T.C. output voltage, and K can be calculated as

$$K = \exp\left\{\frac{\gamma T}{2nV_T}\left[\frac{2\partial\Phi_B/\partial T - \partial V_{gs1}/\partial T}{\sqrt{2\Phi_B(T_0) - V_{gs1}(T_0)}} - \frac{2\partial\Phi_B/\partial T}{\sqrt{2\Phi_B(T_0)}}\right]\right\}. \tag{3.22}$$

3.4 Design Considerations and Simulations

3.4.1 Process Variations

According to Eqs. (3.10) and (3.11), the output voltage (V_{ref}) in this paper is the difference between two gate-source voltages, which requires the threshold voltages (V_{th0}) in M1 and M2 to be identical. In other words, the threshold voltages between the two transistors must match very well. However, the process variations, including within-die (WID) variations and die-to-die (D2D) variations [13, 24, 40], result in the mismatch of threshold voltage. WID accounts for variations that originate between different devices and interconnects that reside within the same chip. WID influences the relative accuracy of transistor parameters. D2D accounts for variations that originate between different chips in the same wafer or different wafers. D2D influences the absolute accuracy of transistor parameters.

In Fig. 3.1, according to Eq. (3.11), the relative variations (WID) in V_{th0}, γ, and W_x/L_x (x = 1,2) are used in the matching description mainly because the mismatch of these parameters is fatal to the T.C. and accuracy of V_{ref}. Eq. (3.11) can be calculated as

$$V_{ref} = \sigma V_{th0} + nV_T ln(K + \sigma K) + (\sigma\gamma + \gamma)(\sqrt{2\Phi_B} - \sqrt{2\Phi_B - V_{gs1}}), \tag{3.23}$$

where σV_{th0}, $\sigma\gamma$, and σK are the mismatch of threshold voltage, coefficient of body bias effect, and size ratio between M1 and M2, respectively. The relative variations can be decided by [40] $\sigma(P) = A_p/\sqrt{WL}$, where A_P is the area proportionality constant related to the process, and P represents the parameters V_{th0}, γ, and K. To reduce these variations, transistors M1 and M2 must have the same channel length and large sizes. Meanwhile, the careful layout technique can be used [41].

For the absolute variations (D2D), the influence of the threshold voltage variation (ΔV_{th0}) is dominant in V_{gs1} with respect to Eqs. (3.6) and (3.17). In this work, ΔV_{th0} is about ± 50 mV according to simulation results, which is the worst case. The variation depends on the process and cannot be decreased in this design. By contrast, the T.C. of V_{th0} is insensitive to the process variation [13, 24], so the T.C. of V_{ref} suffers less from the variation in the T.C. of V_{th0}. However, ΔV_{th0} results in the variation in V_{gs1} with respect to Eqs. (3.6) and (3.17). Thus, the accuracy of V_{ref} and its T.C. suffer from ΔV_{th0} according to Eqs. (3.11) and (3.14), and T.C. is more significantly impacted by the variation. In particular, ΔV_{th0} results in the variation in the T.C. of the CTAT term. To compensate for the T.C. variation of the CTAT term, the T.C. of the PTAT term should be adjusted, which suggests that the size ratio K in Eq. (3.14) can be adjusted. Such adjustment can be performed using the composite transistor [42] for digital trimming, as shown in Fig. 3.4. NMOS transistors used as the switches (S1 to S6) are implemented in our experiment. By using six digital control bits, the different aspect ratios of M1 can be generated for the trimming procedure after chip fabrication.

To determine the influence resulting from ΔV_{th0} on the accuracy and the T.C. of V_{ref}, the simulated results for the corner analysis with typical code of "111000" (S1 to S6: 111000, where "1" means the switch turns on, whereas "0" means the switch turns off) are shown by the solid lines in Fig. 3.5, where SS is slow-slow, TT is typical-typical, and FF is fast-fast for PMOS and NMOS, respectively. From Eq. (3.22), a zero T.C. has been achieved for TT by choosing an adaptive size ratio K, which indicates that the absolute value of positive T.C. is equal to that of negative T.C. according to Eq. (3.14). For SS, $V_{th0}(S) > V_{th0}(T)$, which indicates that $V_{gs}(S) > V_{gs}(T)$, such that the absolute value of negative T.C. is decreased according to the term in the square brackets of Eq. (3.14). The condition suggests that the absolute value of positive T.C. is larger than that of the negative T.C.. Thus, the output voltage presents a positive temperature variation. Likewise, for FF, $V_{th0}(F) < V_{th0}(T)$, such that absolute value of negative T.C. is increased, the absolute value of positive T.C. is smaller than that of negative T.C., such that the output voltage exhibits negative temperature dependence.

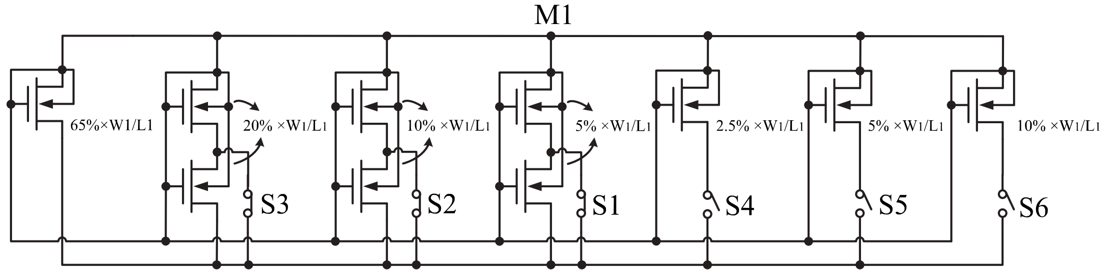


Figure 3.4: Implementation of trimming network for M1.

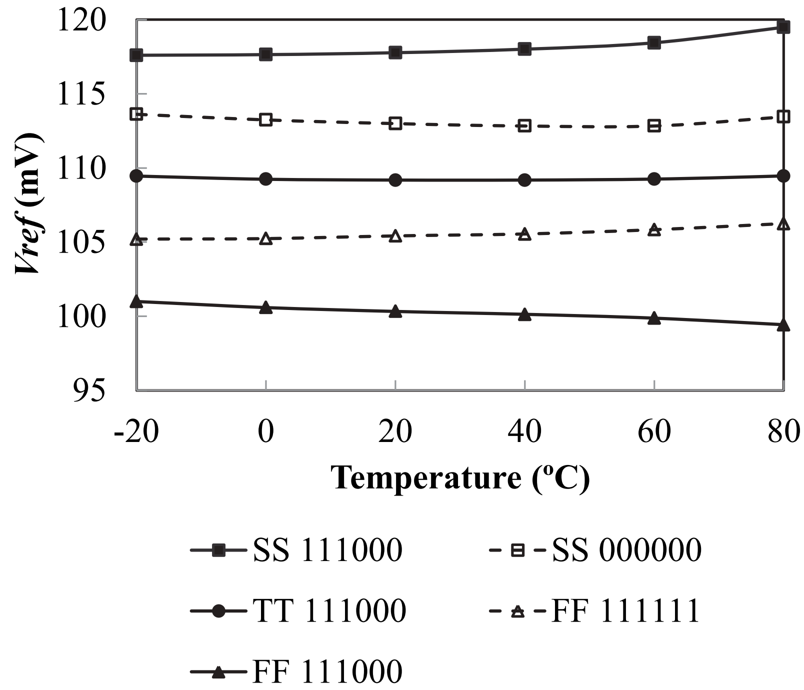


Figure 3.5: Simulated temperature characteristics of V_{ref} for corner analysis with different digital codes for trimming.

Based on the simulation results shown by the solid lines in Fig. 3.5, the resolution and range for trim illustrated in Fig. 3.4 are determined because the SS and FF styles are the worst cases. The simulation results for evaluating the trimming performance in different code conditions are shown by the dashed lines in Fig. 3.5. For SS, to compensate for the T.C. variation shown by the solid line in Fig. 3.5, the proportion of the positive T.C. in Eq. (3.14) should be reduced, which indicates that the aspect ratio of M1 should be decreased, and zero T.C. can be achieved at SS style with the lowest code of “000000.” For FF, the proportion of the positive T.C. in Eq. (3.14) should be raised to compensate for the T.C. variation illustrated by the solid line in Fig. 3.5, which indicates that the aspect ratio of M1 should be increased, and the reference voltage at FF style with the highest code of “111111” presents positive temperature dependence. Hence, the resolution of 2.5% is sufficient to improve the temperature performance within the variation range. And the trimming procedure also minimizes the output spread.

3.4.2 Minimum Current Consumption and Minimum Supply Voltage

According to the configuration of the proposed circuit in Fig. 3.3, the supply current drawn from the power supply (neglecting the current flowing in the start-up circuit) can be expressed as the sum of the currents flown into the biased-current and the core circuits ($I_{dd} = 4I_P$). The power dissipation can be reduced by setting the nano-ampere current in each branch.

As shown in Fig. 3.3, the current mirrors in the cascode structure improve the line sensitivity and power supply rejection ratio (PSRR), but this structure increases the minimum supply voltage. The transistor M6 works in the saturation region, and the supply voltage can be redistributed as a sum of two drain-source voltages V_{ds} and a gate-source voltage V_{gs} in the branches of both biased-current and core circuits. Considering the ultra-low biased current I_P (only several nano-ampere) and subthreshold operation, the minimum supply voltage must ensure $V_{ds} > 4V_T$ and $V_{gs6} > V_{th6}$. Thus, the minimum Vdd can be given by $V_{dd} \geq 8V_T + V_{th6}$.

Fig. 3.6 shows the simulated supply voltage sensitivity. The minimum operational supply voltage can be less than 1 V. The biased current I_P is also too minimal to turn on the forward-biased PN junction (substrate-source connection).

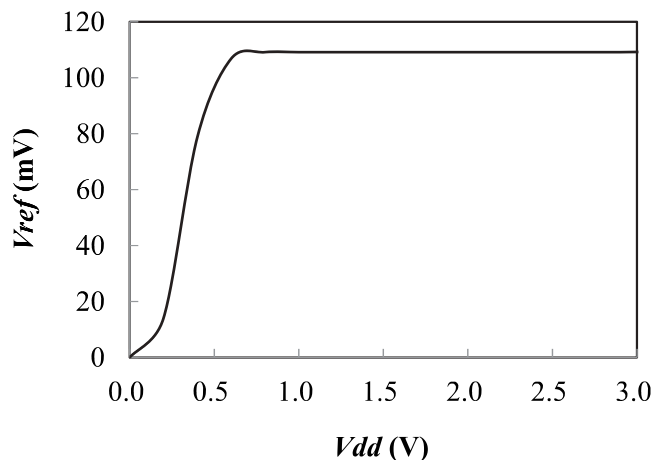


Figure 3.6: Simulated V_{ref} versus Vdd.

3.5 Measurement Results

The proposed VR was implemented in double-poly five-metal 0.18 μm CMOS technology. The chip micrograph is shown in Fig. 3.7, and the active silicon area is about 0.028 mm^2.

Fig. 3.8 illustrates the simulated and test results with and without trimming at Vdd = 1 V. The experimental output voltage after trimming is about 107.5 mV, the voltage variation is 0.43 mV when the temperature varies from -20 °C to 80 °C, and the T.C. is about 40 ppm /°C. Fig. 3.9 shows a plot of the measured output voltage V_{ref} versus temperature from -20 °C to 80 °C; the supply voltage is varied from 0.85 V to 3 V.

Fig. 3.10 shows the experimental values of the total current flowing in the proposed VR circuit (including start-up, biased-current and core circuits), which are drawn from different supply voltages over the temperature range -20 °C to 80

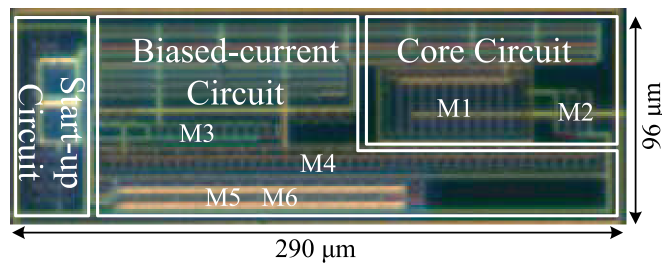


Figure 3.7: Chip micrograph of the proposed circuit.

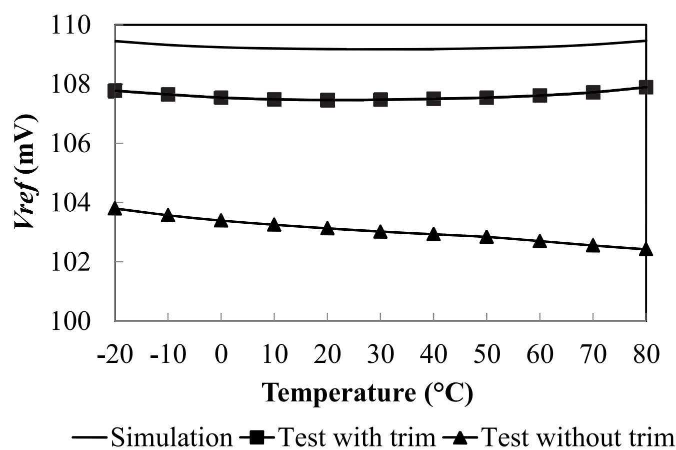


Figure 3.8: Measurement results versus temperature.

°C. The value is about 24 nA at 80 °C, and the power dissipation with a 0.85 V power supply is about 20 nW at 80 °C.

The supply voltage dependence of the proposed VR is shown in Fig. 3.11. The voltage variation is about 0.04 mV when the supply voltage changes from 0.85 V to 3 V, the line sensitivity is 0.017 %/V. The measured PSRR is shown in Fig. 3.12. The value is about -72 dB at 100 Hz, and V_{ref} has low sensitivity to the variation in the supply voltage.

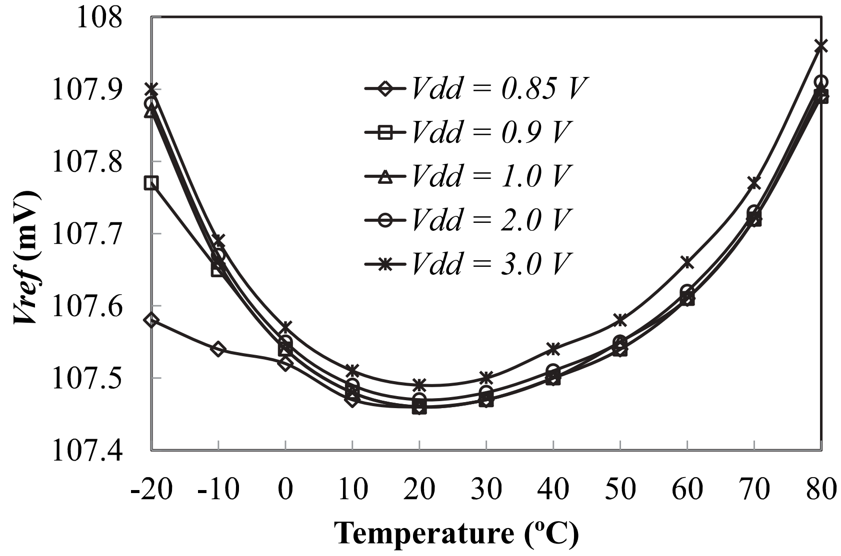


Figure 3.9: V_{ref} versus temperature at different supply voltages.

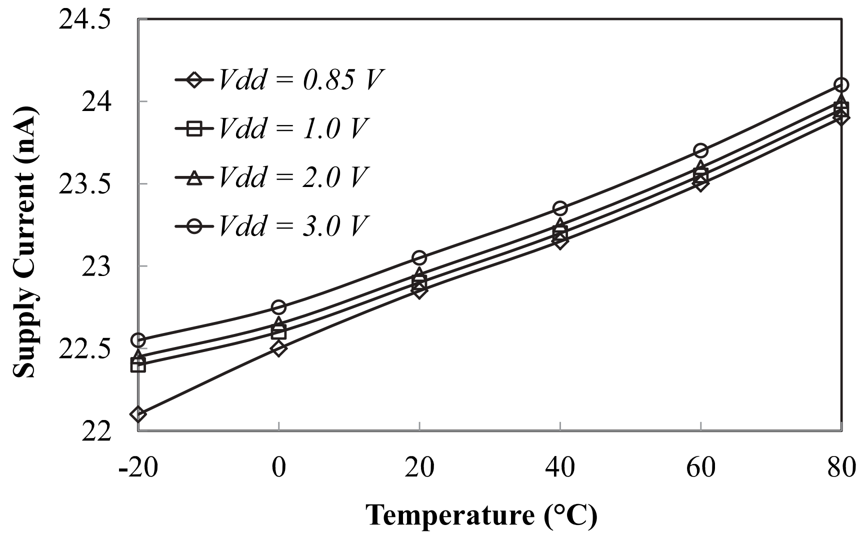


Figure 3.10: Supply current versus temperature at different supply voltages.

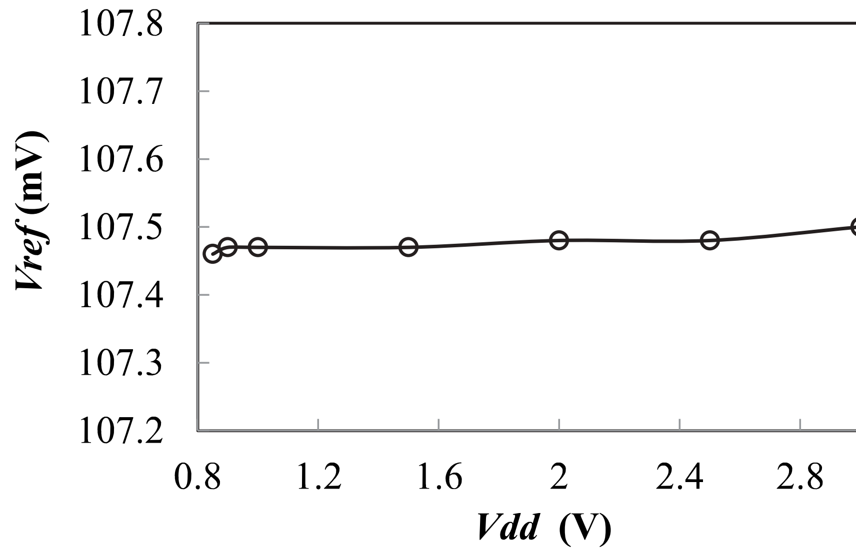


Figure 3.11: V_{ref} versus supply voltage.

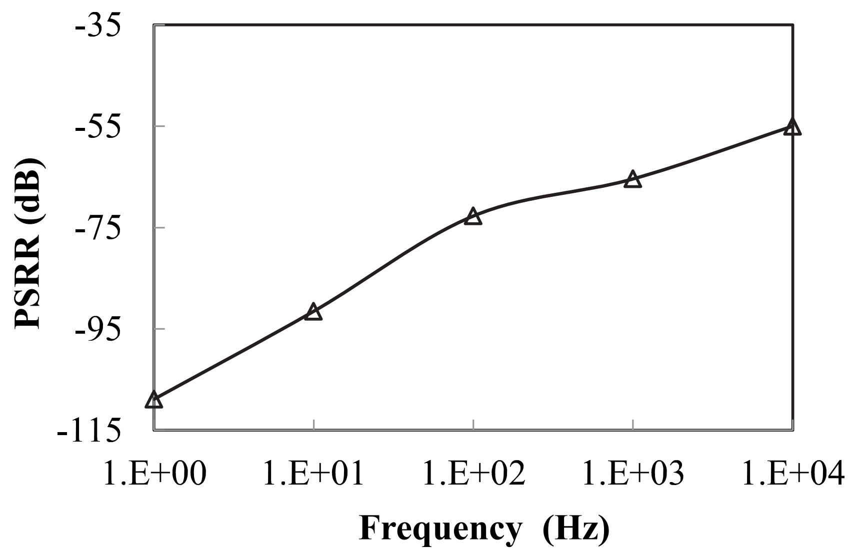


Figure 3.12: Experimental PSRR result.

To evaluate the process dependence, five samples from the same wafer are tested at 1 V supply voltage after trimming. Fig. 3.13 shows the results. The T.C. ranges from 40 ppm/°C to 72 ppm/°C, and the value changes with different dies because the deviation in the threshold voltage results from D2D variations. The average T.C. is approximately 52.8 ppm/°C, and the average reference voltage is about 107.3 mV.

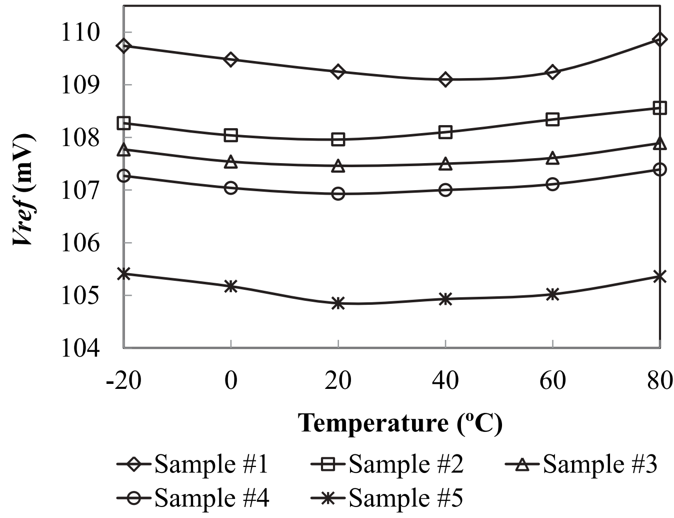


Figure 3.13: V_{ref} versus temperature for five samples at $Vdd = 1$ V.

Table 3.2 summarizes characteristics of our proposed circuit compared with other published low-voltage low-power voltage references in CMOS process. Standard CMOS VRs producing the conventional voltage ($V_{ref} > V_{th}$) are not taken into account. The comparison reveals that the proposed configuration achieves the low output voltage without using the resistive subdivision and consumes nano-power dissipation. The trimming capacity ensures the circuit have an appropriate T.C., and the circuit has satisfactory performance in terms of sensitivity to supply voltage. The chip has a small area occupation.

Table 3.2: Comparison with other low-voltage low-power voltage reference.

	This work	Ref.[24]	Ref.[19]	Ref.[20]	Ref.[17]	Ref.[18]
Process	0.18 μm	0.18 μm	0.35 μm	0.18 μm	0.6 μm	1.2 μm
V_{th}-NMOS V_{th}-PMOS	0.45 V -0.383 V	0.32 V -0.456 V	0.45 V	0.461 V -0.439 V	0.9 V -0.9 V	0.77 V -1.05 V
Supply voltage (V)	0.85 to 3.0	0.45 to 2.0	1.5 to 4.3	0.85 to 2.5	1.4 to 3.0	1.2
Supply current (nA) @ room temperature	23 @ 3 V	7 @ 1 V	1200 @ 1.5 V	3882 @ 0.85 V	< 9700	3600 @ 1.2 V
Vref (mV)	107.3	257.5	168	221	309.3	295
T.C. (ppm/°C) Temp range (°C)	52.8 -20 to 80	165 0 to 125	25 0 to 80	194 -20 to 120	36.9 0 to 100	119 -25 to 125
Line sensibility (%/V)	0.017	0.44	0.95	0.905	0.083	-
PSRR (dB) @ 100 Hz	-72	-45	-65	-	-47	-40
Chip area (mm^2)	0.028	0.043	0.08	0.0238	0.055	0.23
Use of resistive subdivision	No	No	Yes	Yes	Yes	Yes
Implementation of trimming capacity	Transistors	-	Resistors	Resistors	Resistors	Resistors

3.6 Conclusion

An all-MOSFETs VR is proposed in this chapter. Based on the difference between two gate-source voltages in the SCM structure operated in the subthreshold region with a self-biased body effect, this circuit can produce a low output voltage without threshold restriction in standard CMOS technology, the value is about 107.5 mV. The T.C. is about 40 ppm/°C after trimming, and the line sensitivity is 0.017 %/V. The ultra-low power dissipation and compact area occupation are also among the advantages of the proposed VR for application in low-voltage low-power subthreshold LSI.

4

Switched-capacitor Voltage Reference Using Reverse-biased Body Effect in MOSFETs

A nano-power CMOS voltage reference is proposed in this chapter [43]. Through a combination of switched-capacitor technology with the body effect in MOSFETs, the output voltage is defined as the difference between two gate-source voltages using only a single PMOS transistor operated in the subthreshold region, which has low sensitivity to the temperature and supply voltage. A low output, which breaks the threshold restriction, is produced without any subdivision of the components, and flexible trimming capability can be achieved with a composite transistor, such that the chip area is saved. The chip is implemented in 0.18 μm standard CMOS technology. Measurements show that the output voltage is approximately 123.3 mV, the temperature coefficient is 17.6 ppm/°C, and the line sensitivity is 0.15 %/V. When the supply voltage is 1 V, the supply current is less than 90 nA at room temperature. The area occupation is approximately 0.03 mm^2.

4.1 Introduction

In Chapter 2 and Chapter 3, the self-biased technology in MOS transistor can be used for voltage reference generator. And the implementation requires at least

two transistors. Such that the match between the two transistors is critical to the performance of VR. From Eqs. (3.11) (3.14) and (3.23), the mismatch of V_{th0} degrades the accuracy and the T.C. of the reference voltage. Through the trimming procedures in Chapter 3 can minimize the T.C. and the output spread, the spread of the output voltage can not be further reduced. Moreover, the value of the output voltage is not scalable, which limits the application in circuits.

Generally, the switched-capacitor (SC) technique is popular for the design of bandgap VRs [44, 45, 46] because of the following advantages [47]: the offset of the amplifier can be canceled; instead of two transistors, only one transistor is used to generate the output voltage, thereby reducing the chip area and avoiding mismatch between transistors; the capacitors match better and occupy less area; and the low current does not require large resistors. One typical structure [44, 46] is shown in Fig. 4.1, the output voltage V_{ref} can be expressed as

$$V_{ref} = \frac{C_2}{C_3}\left[V_{be} + \frac{C_1}{C_2}V_T ln\left(\frac{I_1}{I_2}\right)\right]. \tag{4.1}$$

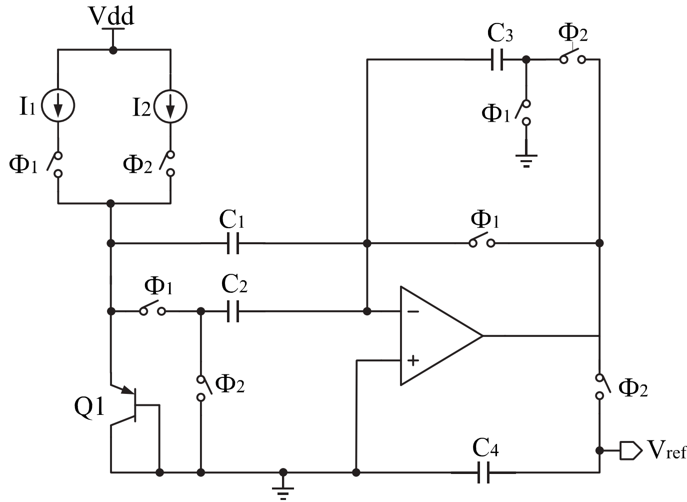


Figure 4.1: Switched-capacitor bandgap voltage reference [44].

A CMOS-based switched-capacitor voltage reference (SCVR) [48] is proposed to improve the design in [15]. Fig. 4.2 shows the structure, the output voltage is given by

$$V_{ref} = \frac{C_1}{C_3}\left[\left(1 + \frac{C_2}{C_1}\right)V'_{gs1} - V''_{gs2}\right]. \tag{4.2}$$

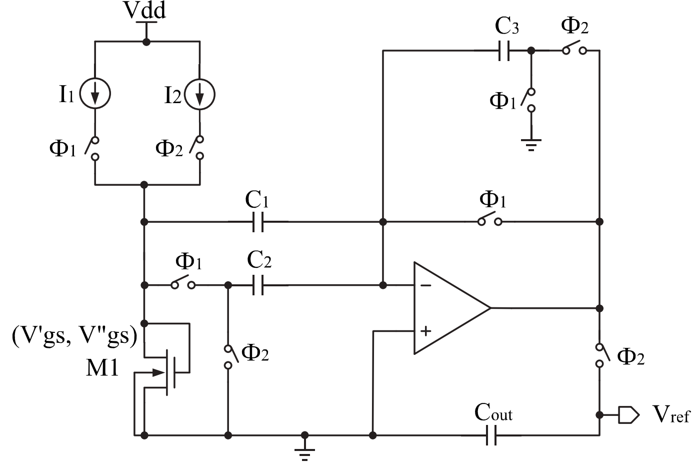


Figure 4.2: Switched-capacitor CMOS voltage reference [48].

Low output is produced through capacitive subdivision instead of the resistive subdivision used in [19], and nano-power dissipation can be achieved. The trimming capacitors can be adjusted for process variations to obtain a low T.C.. However, this operation conventionally requires three capacitors, and the capacitive subdivision requires a large value. Thus, this operation occupies more chip area. Therefore, a method that combines the SC-based technology with the body-biasing technology in MOSFETs is explored in this paper to solve the aforementioned problems, which also improves the design shown in Fig .2.2. Low output ($< V_{th}$) is produced and can be scalable with standard CMOS technology, and the method achieves power and area savings. The remainder of this chapter is organized as follows: Section 4.2 describes the operating principle of the proposed SCVR. In Section 4.3, implementation of the circuit is presented. Considerations for this design and simulations are discussed in Section 4.4, and measurement results are demonstrated in Section 4.5. Finally, Section 4.6 provides the conclusions.

4.2 Operating Principles of Proposed SCVR

The proposed SCVR circuit shown in Fig. 4.3 is based on a sample and hold structure [47]. The circuit is composed of a bias current circuit, a core circuit, switched

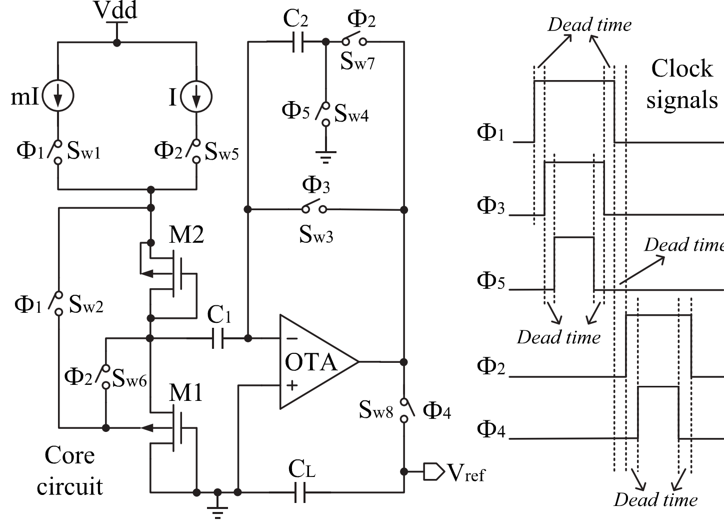
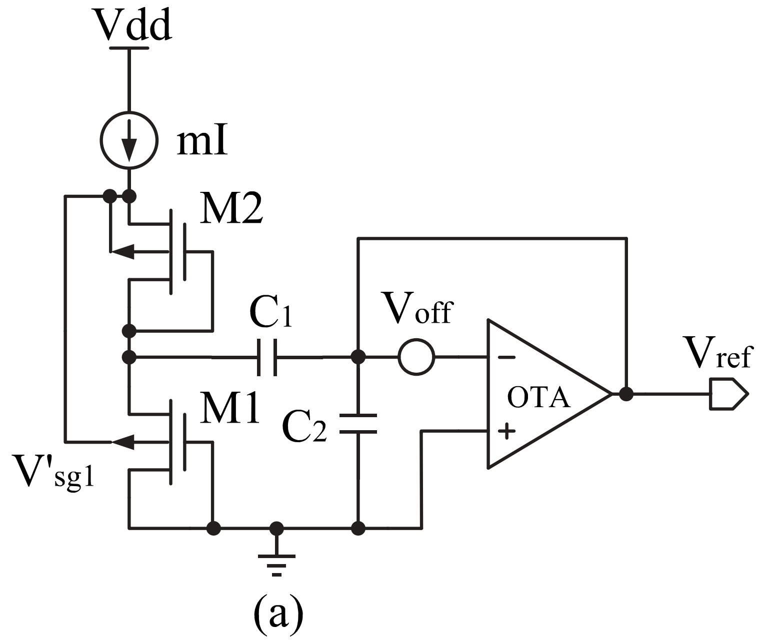


Figure 4.3: Proposed SCVR using MOS body effect.

capacitors, and an operational trans-conductance amplifier (OTA). The switches $S_{W1} - S_{W8}$ are controlled by non-overlapping clock signals ($\Phi_1, \Phi_2, \Phi_3, \Phi_4, \Phi_5$). The core circuit inputs two different gate-source voltages (V'_{sg1} and V''_{sg1}) in M1 to the OTA during $\Phi_1 = 1$ and $\Phi_2 = 1$, respectively. If the clock signals Φ_1 and Φ_2 overlap, M1 will be biased at a state where the body of M1 is connected to its source and to the source of M2 during the overlap. As a result, an invalid gate-source voltage of M1 will be stored in C_1 and the invalid voltage will degrade the accuracy of the reference voltage because the reference voltage appears during $\Phi_2 = 1$. Meanwhile, more power will be dissipated during the overlap. Hence, the dead time between Φ_1 and Φ_2 is necessary to ensure accurate output and to preserve power dissipation. Φ_3 is designed to turn off the switch before Φ_1 so that the stored voltage in capacitor C_1 will be immune to the input-dependence charge injection from the switch; In addition, Φ_5 should be turned off before Φ_3 to avoid charge injection and storage on capacitors C_1 and C_2. The dead-time region between Φ_2 and Φ_4 prevents the accuracy of V_{ref} from being impacted by the charge injection effect.

The equivalent structure of the proposed SCVR circuit is presented in Figs. 4.4(a) and (b). During the sampling state ($\Phi_1 = 1$ and $\Phi_2 = 0$), the PMOS transistor M1 is biased at mI (m is the ratio between the two different currents),



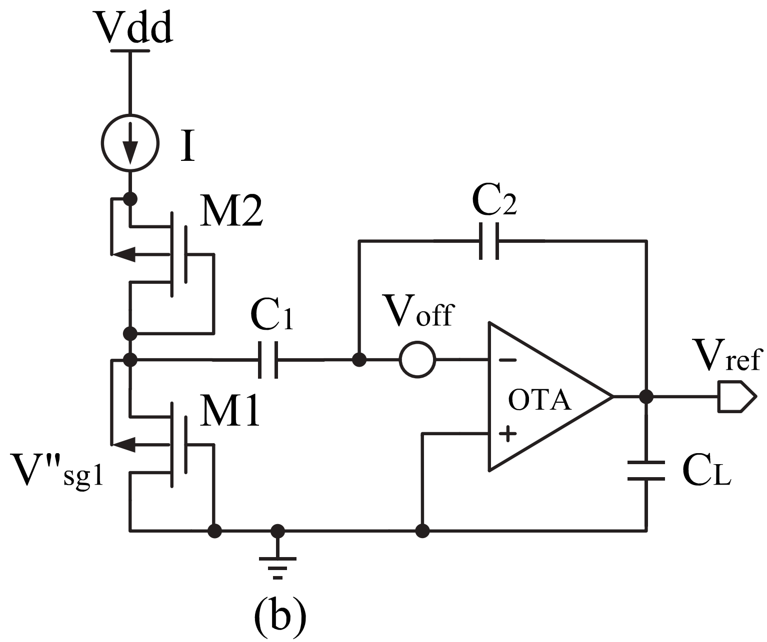


Figure 4.4: Equivalent schematic of the proposed SCVR circuit (a) when $\Phi_1 = 1$ and $\Phi_2 = 0$, (b) when $\Phi_1 = 0$ and $\Phi_2 = 1$.

and a gate-source voltage is stored in capacitor C_1. Capacitor C_2 is connected to the ground. During the hold state ($\Phi_1 = 0$ and $\Phi_2 = 1$), M1 is biased at I and another gate-source voltage is provided as input to C_1, while C_2 is connected to the output to form a negative feedback loop. The charges (ΔQ_1 and ΔQ_2) on each capacitor in terms of the offset voltage V_{off} of the OTA are given by Eqs. (4.3) and (4.4)

$$\begin{aligned}\Delta Q_1 &= C_1(V'_{sg1} - V_{off}) - C_1(V''_{sg1} - V_{off}) \\ &= C_1(V'_{sg1} - V''_{sg1}) \end{aligned} \tag{4.3}$$

$$\Delta Q_2 = C_2(-V_{off}) - C_2(V_{ref} - V_{off}) = -C_2V_{ref} \tag{4.4}$$

From the equations, V_{off} can be eliminated by storing the capacitors, which is auto-zeroing technology. According to the law of conservation of charge, the charges must equal to each other

$$\Delta Q_1 + \Delta Q_2 = 0. \tag{4.5}$$

From Eqs. (4.3) and (4.4), the output voltage can be expressed as

$$V_{ref} = \frac{C_1}{C_2}(V'_{sg1} - V''_{sg1}). \tag{4.6}$$

The load capacitor C_L, which is usually off-chip [44, 45, 46, 48], ensures that the output is valid during the sampling period. The control circuit of the switches for the non-overlapping clock signals is presented in Figs. 4.5(a) and (b). The operation is shown in Fig. 4.6. The result is the difference between the two gate-source voltages (ΔV_{sg}) of M1 during the two phases.

According to Eq. (2.23), the gate-source voltage V_{sg} of the PMOS transistor in the subthreshold region can be expressed as ($V_{sd} > 4V_T$)

$$V_{sg} = V_{th} + nV_T ln\left(\frac{I_D}{KI_t}\right), \tag{4.7}$$

$$I_t = \mu_p(n-1)C_{ox}V_T^2. \tag{4.8}$$

where I_D is the drain current, K (= W/L) is the aspect ratio of the transistor. $V_T = kT/q$, where k is Boltzmann's constant.

As shown in Figs. 4.4 and 4.6, the body of M1 is connected to the source of M2 during the sampling state ($\Phi_1 = 1$) to form a reverse-bias connection; thus, V'_{sg1} is defined as

$$V'_{sg1} = V'_{th1} + nV_T ln\left(\frac{mI}{K_1 I_t}\right), \tag{4.9}$$

$$V'_{th1} = V_{th0} + \gamma\left(\sqrt{2\Phi_B + V_{bs1}} - \sqrt{2\Phi_B}\right). \tag{4.10}$$

During the hold state ($\Phi_2 = 1$), V''_{sg1} can be given by

$$V''_{sg1} = V''_{th1} + nV_T ln\left(\frac{I}{K_1 I_t}\right), \tag{4.11}$$

$$V''_{th1} = V_{th0}. \tag{4.12}$$

With Eqs. (4.9) to (4.12) and $V_{bs1} = V_{sg2}$, Eq. (4.6) can be presented as

$$V_{ref} = \frac{C_1}{C_2}\left[\gamma\left(\sqrt{2\Phi_B + V_{sg2}} - \sqrt{2\Phi_B}\right) + nV_T ln(m)\right] \tag{4.13}$$

$$V_{sg2} = V_{th2} + nV_T ln\left(\frac{mI}{K_2 I_t}\right) \tag{4.14}$$

In Eq. (4.13), the first term inside the square brackets is CTAT and achieves a negative T.C.. The second term is proportional to the PTAT and implements a positive T.C.. Because of the body-biasing effect from the bias voltage V_{sg2}, the CTAT term is achieved with two distinct threshold voltage levels (V'_{th1} and V''_{th1}). Therefore, the absolute value of V_{th0} in V_{ref} is canceled. Under the assumption that $C_1 = C_2$, a low output voltage ($V_{ref} < V_{th0}$) is obtained.

The proposed SCVR has advantages as follows: The operation only requires two capacitors (C_1 and C_2), whereas other SCVRs require more [46, 48]. Based on Eqs. (4.6) and (4.13), the low output does not require capacitive subdivision; furthermore, the ratio C_1/C_2 can be used to determine the scale of the output. The reference voltage is implemented with only one transistor (M1) in the standard process, such that the component matching errors are decreased, and the chip area is saved. The input offset of the amplifier can be canceled. The bias currents only require nano-ampere levels because M1 and M2 work in the subthreshold region, and the current ratio m can be selected to obtain a zero T.C., as demonstrated in the next section.

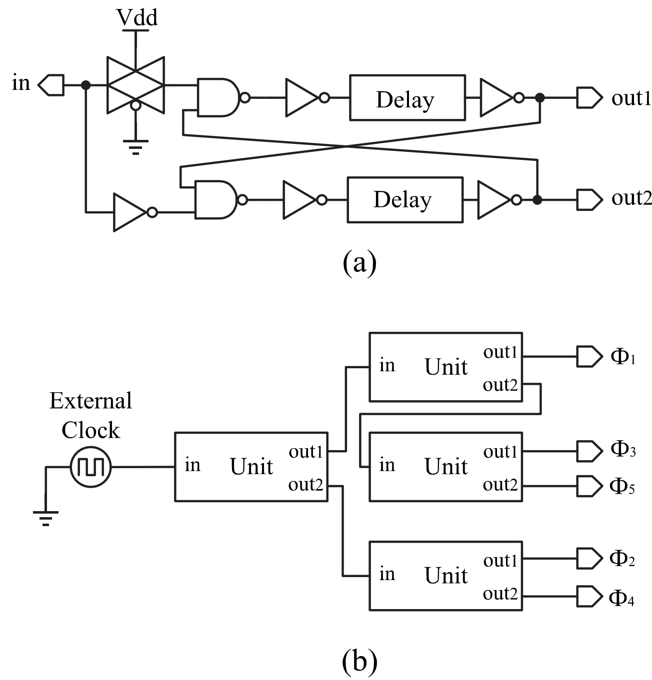


Figure 4.5: Control circuit for switches. (a) The non-overlapping clock unit. (b) The whole circuit for the clock signals.

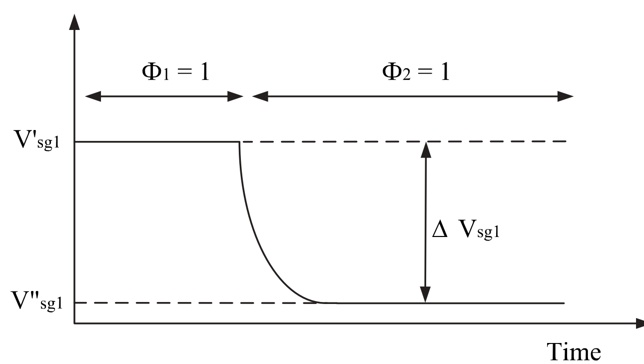


Figure 4.6: Gate-source voltage of M1 during the two phases.

4.3 Implementation of Proposed SCVR Circuit

Fig. 4.7 shows the proposed SCVR circuit composed of the start-up circuit, the bias current circuit, the core circuit, and the OTA.

4.3.1 Nano-ampere Bias Current Circuit

The cascode current-bias circuit [38] can generate a nano-level current that is insensitive to technology, temperature, and supply voltage; thus, low-power dissipation can be ensured. Transistors M5 and M6 operate in the subthreshold region, whereas M7 and M8 work in the linear region and the saturation region, respectively. Current mirrors in the cascode structure improve line sensitivity; however, the structure increases the minimum supply voltage. For the subthreshold operation in current mirrors and the saturation operation in M8, the minimum supply voltage must ensure $V_{sd} > 4V_T$ and $V_{gs8} > V_{th8}$. Thus, the minimum supply voltage can be redistributed as the sum of two drain-source voltages V_{ds} and a gate-source voltage V_{gs8} in the branches of the circuit ($V_{dd} > V_{th8} + 8V_T$).

4.3.2 Control of T.C.

The core circuit consists of transistors M1 and M2, switches, and capacitors. The zero T.C. is satisfied by

$$\frac{\partial V_{ref}}{\partial T} \mid_{T=T_0} = 0, \tag{4.15}$$

where T_0 is room temperature. Thus, the temperature dependence of the SCVR can be obtained by differentiating Eq. (4.13) with respect to temperature and can be given by

$$\begin{aligned} \frac{C_1}{C_2} \left\{ \frac{1}{2}\gamma \left[(2\Phi_B(T_0) + V_{sg2}(T_0))^{-\frac{1}{2}} \left(2\frac{\partial \Phi_B}{\partial T} + \frac{\partial V_{sg2}}{\partial T} \right) \right. \right. \\ \left. \left. -(2\Phi_B(T_0))^{-\frac{1}{2}} \left(2\frac{\partial \Phi_B}{\partial T} \right) \right] + n\frac{V_T}{T} ln(m) \right\} = 0 \end{aligned} \tag{4.16}$$

In this work, the T.C. of Φ_B is approximately -0.7 mV/°C, the T.C. of V_{sg2} is approximately -1.25 mV/°C, Φ_B is approximately 0.35 V, γ is approximately 0.5 $\sqrt{V}$, n is approximately 1.2, and V_{sg2} is approximately 0.31 V. For Eq. (4.16),

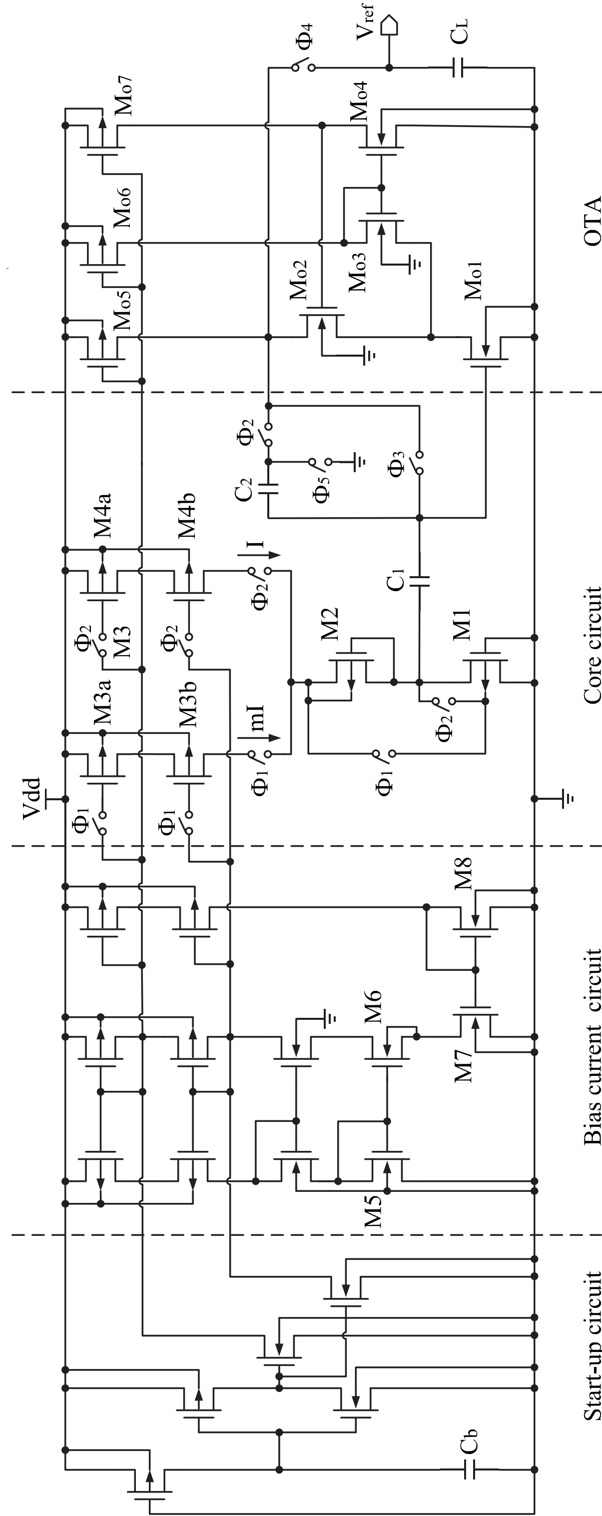


Figure 4.7: Proposed switched-capacitor voltage reference circuit.

the first term in the brace has a negative T.C., whereas the thermal voltage V_T has a positive T.C. (0.087 mV/°C) [11] in the second term. Hence, a zero T.C. can be achieved by choosing an adaptive biased-current ratio m that is the size ratio between M3a (M3b) and M4a (M4b). With the value of the parameters in Eq. (4.16), the value of m can be calculated from

$$\begin{aligned} m &= \exp\left\{\frac{\gamma T}{2nV_T}\left[(2\Phi_B(T_0)^{-\frac{1}{2}}\left(2\frac{\partial\Phi_B}{\partial T}\right)\right.\right. \\ &\left.\left. -(2\Phi_B(T_0)+V_{sg2}(T_0))^{-\frac{1}{2}}\left(2\frac{\partial\Phi_B}{\partial T}+\frac{\partial V_{sg2}}{\partial T}\right)\right]\right\} \end{aligned} \tag{4.17}$$

4.3.3 OTA circuit

The OTA [49] consists of the transistors $M_{o1} - M_{o7}$. The input offset resulting from asymmetries and process variations is canceled by the use of the switched-capacitor network. The transistors M_{o1} and M_{o2} form the cascode amplifier, and M_{o3} and M_{o4} constitute the feedback loop to increase the output impendence and boost the gain of the OTA, thereby enhancing the precision and speed of the switched-capacitor amplifier. The OTA can be operated with a nano-current supply. From simulations, the gain of the OTA is approximately 70 dB when $Vdd = 1$ V at room temperature.

4.4 Design Considerations and Simulations

4.4.1 Charge Injection Effects and Clock Feed-through

The switched-capacitor circuit suffers from charge-injection errors and clock feed-through, which influences the precision. The priori method is the transmission gate at the switch [11]. The charge injection and clock feed-through effects can be effectively eliminated with the complementary structure because the opposite charge packets (holes and electrons) injected from the PMOS and NMOS cancel each other, and the on-resistance in the switch can be reduced to achieve high-speed operation.

4.4.2 Operational Clock Frequency

For SC circuits, the output is not valid in one phase because of the discrete-time nature of these circuits; the solution is to use an output filter capacitor. However, a droop of the output voltage across the load capacitor is caused by leakage current that mainly consists of the switch leakage current and bias current of amplifier. Thus, a ripple always exists at the output. The value of the ripple (V_{ripple}) is expressed by [50]

$$V_{ripple} = \frac{I_{leak}}{C_L f_{clk}}, \tag{4.18}$$

where I_{leak} is the leakage current that flows in or out of the hold capacitor when the sampled and hold amplifier is in hold mode, and f_{clk} is the clock frequency. There is a trade-off between the clock frequency and power consumption; the lower the frequency, the less the power dissipated. However, lower frequency can result in larger voltage ripples and can degrade the accuracy of the output voltage according to Eq. (4.18). Hence, the operational frequency must not be too small. With our design used in ADC [7], the output voltage is not allowed to droop by more than 1/2 LSB. With a large leakage current at 80 °C, the transient analysis is simulated to evaluate the performance, as shown in Fig. 4.8. The ripple is approximately 0.5 mV with a 100 pF output capacitor when the clock frequency is 1 kHz.

4.4.3 Process Variations and Trimming

Process variations are generally distinguished between within-die (WID) variations and die-to-die (D2D) variations [39]. WID variations (e.g., σV_{th}, $\sigma W/L$) cause mismatch between transistors of the same chip and influence the relative accuracy of the transistor parameters, whereas D2D variations (e.g., ΔV_{th}, $\Delta W/L$) influence the absolute accuracy of the transistor parameters. For the core circuit in this study, the influence of WID variation (σV_{th}) decreases because only one transistor is used for the voltage reference generator. The zero T.C. is primarily determined by the size ratio between M3a (M3b) and M4a (M4b); thus, the mismatch of W/L ($\sigma W/L$) between transistors results from WID variations. This

effect can be effectively reduced because of the careful layout techniques and large sizes of transistors.

However, D2D variations cannot be avoided. The influence of ΔV_{th} is dominant because V_{th} is poorly controlled in a manufacturing environment. As shown in Eq. (4.14), V_{sg} suffers from ΔV_{th} because of process variations. Thus, according to Eqs. (4.13) and (4.16), the process variations result in spreads in the output voltage and in the T.C.. In particular, the T.C. is more significantly impacted. To investigate the impact, Fig. 4.9 shows the simulated results for the T.C. when $Vdd = 1.5$ V and $C_1 = C_2 = 600$ fF. Because $V_{th}(S) > V_{th}(T) > V_{th}(F)$, $V_{sg2}(S) > V_{sg2}(T) > V_{sg2}(F)$ at room temperature T_0 for M2. Thus, from Eqs. (4.16) and (4.17), if the adaptive size ratio m between M3a (M3b) and M4a (M4b) is set to achieve a zero T.C. for TT, then the absolute value of the negative T.C. is equal to that of the positive T.C.. For SS, V_{sg2}(S) causes a decrease in the value of the negative T.C. in accordance with Eq. (4.16), such that the absolute value of the negative T.C. is smaller than that of the positive T.C., and the output voltage shows a positive temperature variation. Conversely, V_{sg2}(F) leads to an increase in the value of the negative T.C., such that the absolute value of the negative T.C. is larger than that of the positive T.C. for FF, and the output voltage exhibits a negative temperature dependence. Therefore, current trimming (changing the T.C. of the PTAT term) is used to correct the slope (compensate for the T.C. variation in the CTAT term); thus, the size ratio m should be adjustable after chip fabrication. One solution is the use of a composite transistor [42], Fig. 4.10(a) presents the trimming network. The trim range and the resolution are determined from the simulations shown in Fig. 4.9. The aspect ratios of M3a and M3b can be changed by digital logic control to adjust the T.C., as shown in Fig. 4.11. The solid lines show the temperature characteristics for the typical code of "111000" (S1 to S6: 111000, where "1" indicates that the switch turns on, whereas "0" means the switch turns off). The trimming performance is shown by the dashed lines in Fig. 4.11. For SS, the temperature characteristics have a negative variation with the lowest code of "000000," and the temperature characteristics for FF have a positive variation with the highest code of "111111." Hence, the resolution of 2% is enough for adjustment to obtain a zero T.C. within the range of variation because SS and FF are the worst cases in this process, and

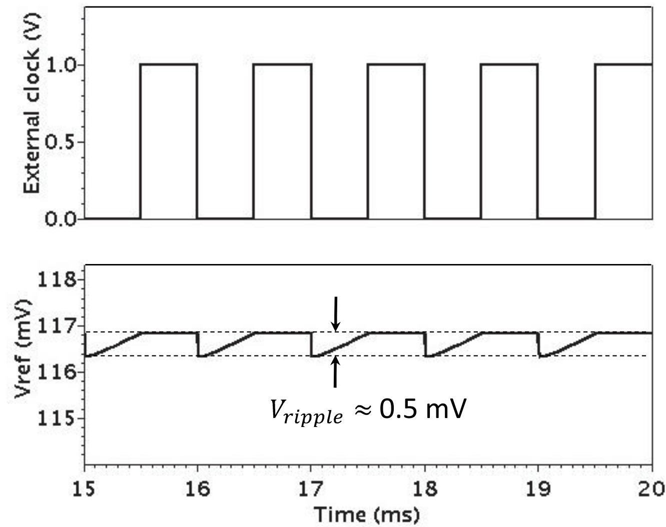


Figure 4.8: Simulated output waveforms when C_L is 100 pF at 80 °C.

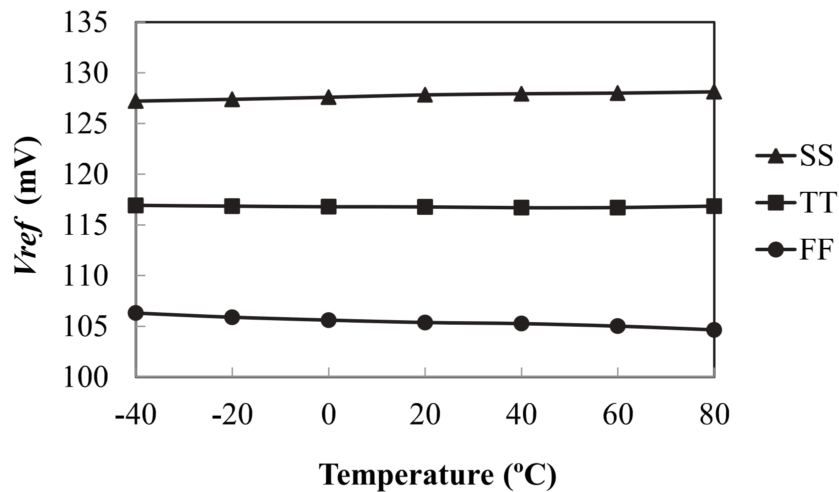


Figure 4.9: Simulated V_{ref} as a function of temperature at different corners. TT: typical PMOS/typical NMOS; SS:slow PMOS/slow NMOS; FF: fast PMOS/fast NMOS.

Table 4.1: Programmable outputs by six bits digital code S_a to S_f.

S_a	S_b	S_c	S_d	S_e	S_f	V_{ref} (mV)
0	0	0	1	1	1	99.8
0	0	1	1	1	1	102.2
0	1	0	1	1	1	104.5
0	1	1	1	1	1	106.8
1	0	0	1	1	1	109.1
1	0	1	1	1	1	111.5
1	1	0	1	1	1	113.8
1	1	1	1	1	1	116.1
1	1	1	1	1	0	118.5
1	1	1	1	0	1	120.9
1	1	1	1	0	0	123.5
1	1	1	0	1	1	126.2
1	1	1	0	1	0	129.0
1	1	1	0	0	1	131.9
1	1	1	0	0	0	135.0

the spread of V_{ref} is also minimized. The adjustable range of m has little impact on the power dissipation and the signal-to-noise ratio because the bias circuit generates a bias current of several nano-amperes.

Based on Eq. (4.16), the programmable outputs can be implemented by adjusting the ratio between C_1 and C_2; the method can also effectively reduce the output voltage spread. Fig. 4.10(b) shows such an adjustment with 2% resolution. Six digital control bits are used to satisfy the requirement of increasing or decreasing the output value. Table 4.1 shows the simulated programmable outputs for TT at room temperature, the value is scalable from 99.8 mV to 135.0 mV by changing the ratio between C_1 and C_2.

In our work, the purpose of the trimming process is to obtain the zero T.C. as well as the minimum output spread. The detailed trimming procedures are as follows. First, the circuit is fabricated with the typical trimming code for the

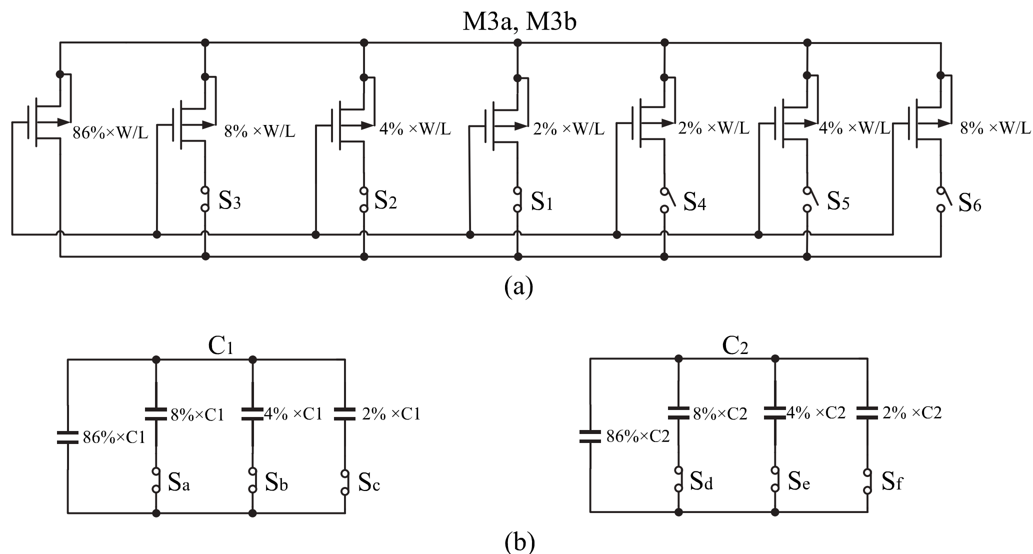


Figure 4.10: (a) Composite structure in M3a and M3b for trimming; (b) implementation of scalable output for C_1 and C_2.

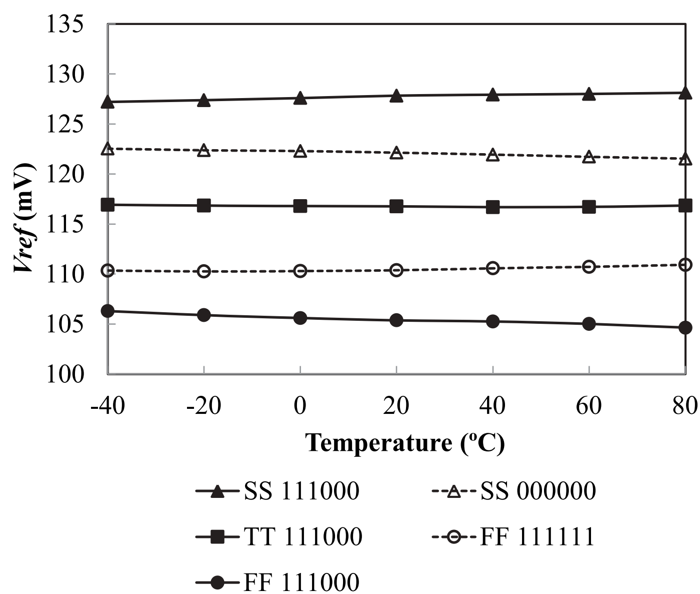


Figure 4.11: Simulated corner analysis under different code conditions.

initial state; then, the voltage reference is measured from -40 °C to 80 °C in 20 °C intervals. With these collected data, the T.C. is obtained. If the T.C. is not equal to zero because of process variations; then, the T.C. curve has a slope S_p. From Eq. (4.16), the slope S_p can be defined as

$$S_p = \frac{C_1}{C_2}\left[N + n\frac{V_T}{T}ln(m)\right], \tag{4.19}$$

where

$$N = \frac{1}{2}\gamma\left[(2\Phi_B(T_0) + V_{sg2}(T_0))^{-\frac{1}{2}}\left(2\frac{\partial\Phi_B}{\partial T} + \frac{\partial V_{sg2}}{\partial T}\right) - (2\Phi_B(T_0))^{-\frac{1}{2}}\left(2\frac{\partial\Phi_B}{\partial T}\right)\right].$$

To obtain the zero T.C., m should be adjusted to compensate for the slope; then, Eq. (4.19) is expressed by

$$\frac{C_1}{C_2}\left[N + n\frac{V_T}{T}ln(m+\Delta m)\right] = 0, \tag{4.20}$$

where Δm is the required range for trimming. The n and T.C. of V_T are assumed to have minimal sensitivity to the process variation, and capacitors are assumed to match very well. With Eqs. (4.19) and (4.20), the required trimming code can be calculated by

$$\frac{\Delta m}{m} = \exp\left(-\frac{C_2 S_p q}{C_1 n k}\right) - 1, \tag{4.21}$$

After obtaining the zero T.C., the output voltage spread can be reduced by changing the ratio between C1 and C2.

NMOS transistors are used as switches (S_1 to S_6, S_a to S_f). In production lines, one-time-programmable (OTP) memories such as fuses can be used to control the switches with minimal power consumption [51].

4.4.4 Effects from Noise

The noise performance should be considered in the SCVR circuit. The most critical noise sources are the non-zero resistance switches, the active transistors inside the OTA, and the noise induced by the clocks. The high-frequency noise is folded back into the signal's baseband in sampled data networks clocked at the same frequency as f_{clk} because of fold effects in sampled noise [52].

For OTA, thermal noise can be reduced by designing a large trans-conductance $g_{m(o1)}$ in M_{o1} and a small trans-conductance $g_{m(o5)}$ in M_{o5} because the noise is proportional to $g_{m(o5)}/g_{m(o1)}$ [11]. The use of transistors with large widths and lengths can decrease flicker noise.

For the switches S_{W1}-S_{W8} shown in Fig. 4.3, the noise analysis is as follows. During the sampling mode ($\Phi_1 = 1$), the switches S_{W1}, S_{W2}, S_{W3} and S_{W4} turn on; thus, the contributor of the noise is the on-resistors of the switches S_{W1}, S_{W2}, S_{W3} and S_{W4}. Then, the total input-referred noise variance V_{ni}^2 is sampled by the capacitors C_1 and C_2, which can be expressed by [11]

$$V_{ni}^2 = \frac{kT}{C_1} + \frac{kT}{C_2}. \tag{4.22}$$

With the closed-loop gain in OTA ($A_{cl} = -C_1/C_2$), during hold mode ($\Phi_2 = 1$), the total output noise variance contributed by the switches S_{W1}, S_{W2}, S_{W3} and S_{W4} is given by

$$V_{no1}^2 = \frac{kT}{C_1} \cdot A_{cl}^2 + \frac{kT}{C_2}. \tag{4.23}$$

During the hold mode ($\Phi_2 = 1$), the switches S_{W5}, S_{W6}, S_{W7} and S_{W8} turn on; thus, the noise is from the on-resistors R_5, R_6, R_7 and R_8 of the switches S_{W5}, S_{W6}, S_{W7} and S_{W8}, respectively. Fig. 4.12 illustrates the equivalent small signal model for noise analysis. C_{in} is the input parasitic capacitance, G_m is the trans-conductance of OTA, Rout is the output resistance, and V_{n5}, V_{n6}, V_{n7} and V_{n8} are the noise sources that model thermal noise of R_5, R_6, R_7 and R_8, respectively.

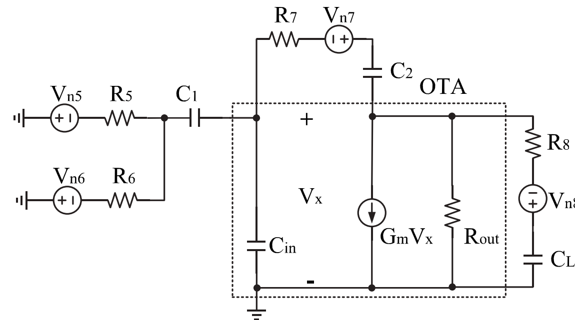


Figure 4.12: Equivalent small signal model for noise analysis due to the switches S_{W5}-S_{W8}.

The output noise variation due to R_8 is kT/C_L; then, the total output noise variance contributed by the switches S_{W5}, S_{W6}, S_{W7} and S_{W8} can be calculated by [53]

$$V_{no2}^2 = \left(\frac{kTRC_2^2}{C_1} + kTR_7\right) B_W + kT\left[\frac{C_2C_m}{C_L(C_LC_n + C_2C_m)}\right] + \frac{kT}{C_L}, \tag{4.24}$$

where $B_W = G_mC_2/(C_LC_n+C_2C_m)$, with $C_m = C_1+C_{in}$ and $C_n = C_2+C_1+C_{in}$, is the bandwidth of the circuit in Fig. 4.12 with $R_{out} >> (C_m + C_2)/C_2G_m$, and $R = R_5R_6/(R_5 + R_6)$. All on-resistors of switches are assumed to have the same value. From Eqs. (4.23) and (4.24), with the folding effects, the total noise variance from the switches $S_{W1} - S_{W8}$ can be expressed by [54]

$$V_{ntot}^2 = (V_{no1}^2 + V_{no2}^2)\left(1 + \frac{2f_{on}}{f_{clk}}\right), \tag{4.25}$$

where f_{on} is the cutoff frequency of the switched-capacitor amplifier.

4.5 Measurement Results

The proposed SCVR circuit is fabricated in the CMOS 0.18 μm process. For this circuit, capacitors C_1 and C_2 are approximately 600 fF, Fig. 4.13 shows the chip micrograph, and the chip area is approximately 0.03 mm^2. The clock frequency is 1 kHz, and the off-chip capacitor C_L used for the output filter capacitor is 100 pF. The measured output waveforms are shown in Fig. 4.14.

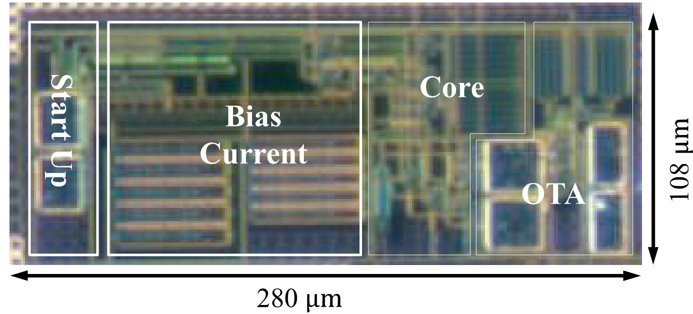


Figure 4.13: Chip micrograph of the proposed SCVR.

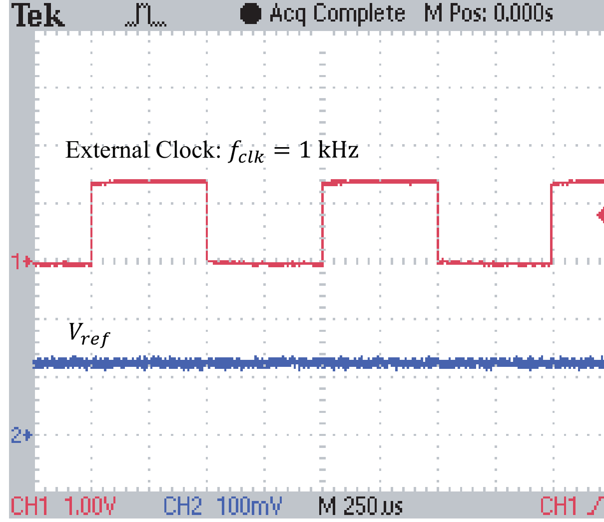


Figure 4.14: Measured output waveforms of the proposed SCVR.

Fig. 4.15 shows the plot of the output voltage as a function of temperature (-40 °C to 80 °C) with the simulated and test results, the measured T.C. after trimming is approximately 17.6 ppm/°C at $Vdd = 1.5$ V, and the output voltage is approximately 123.3 mV. Additionally, the temperature characteristics of V_{ref} when the supply voltage ranges from 1 V to 3 V, are presented in Fig. 4.16. Based on the measurements at -40 °C, proper operation is obtained for $Vdd \geq 1$ V. The measurement line sensitivity is approximately 0.15 %/V when Vdd varies from 1 V to 3 V at room temperature. Fig. 4.17 shows a plot of the supply current as a function of temperature at different supply voltages, the supply current is approximately 90 nA at room temperature when Vdd is 3 V, and the operating currents of the biased circuit, the core circuit, and the OTA are approximately 15 nA, 30 nA, and 45 nA, respectively.

The measured results of the SCVR for the three trimmed samples are shown in Fig. 4.18. The average voltage variation is approximately 1 mV, and the T.C. from the three samples are 19.5 ppm/°C, 17.6 ppm/°C, and 15.6 ppm/°C, respectively.

The output noise spectrum is measured with a 100 pF output capacitor at room temperature, as shown in Fig. 4.19. The peak value is approximately 367 $\mu V/\sqrt{Hz}$ at 1 kHz.

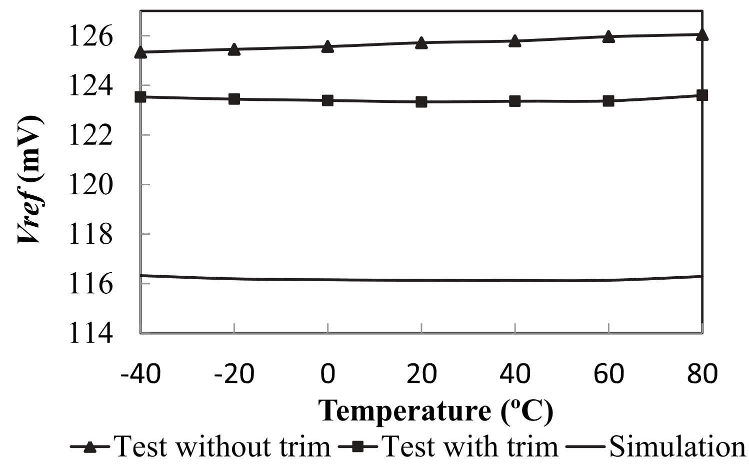


Figure 4.15: Measured and simulated temperature dependence at Vdd = 1.5 V.

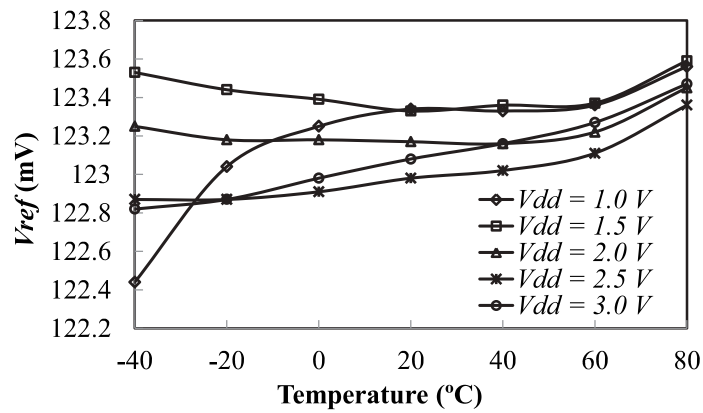


Figure 4.16: V_{ref} as a function of temperature for different supply voltages.

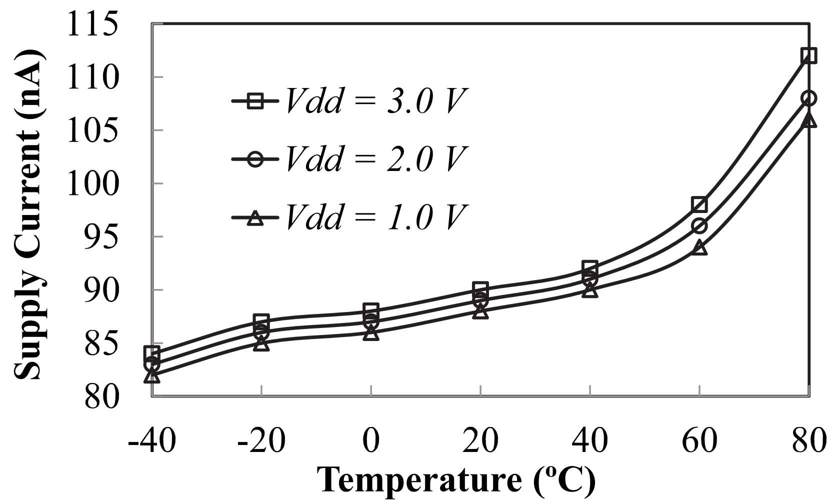


Figure 4.17: Supply current as a function of temperature for different supply voltages.

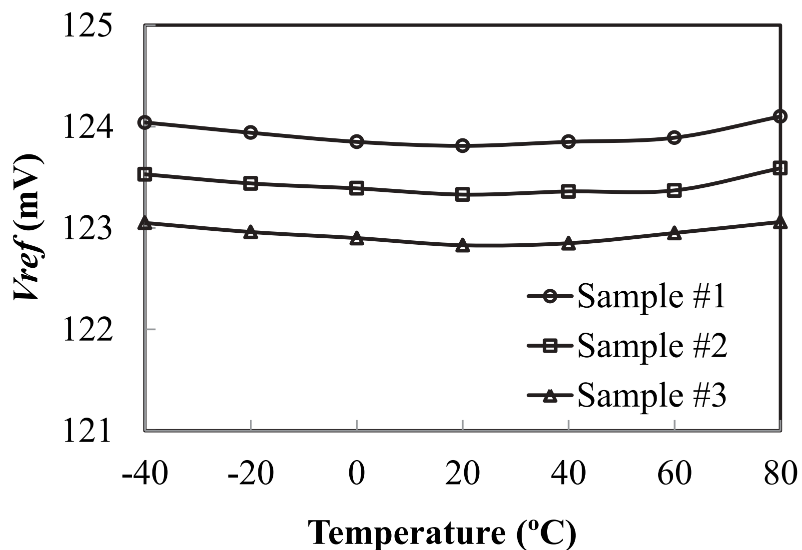


Figure 4.18: Measured V_{ref} versus temperature for three samples with $Vdd =$ 1.5 V.

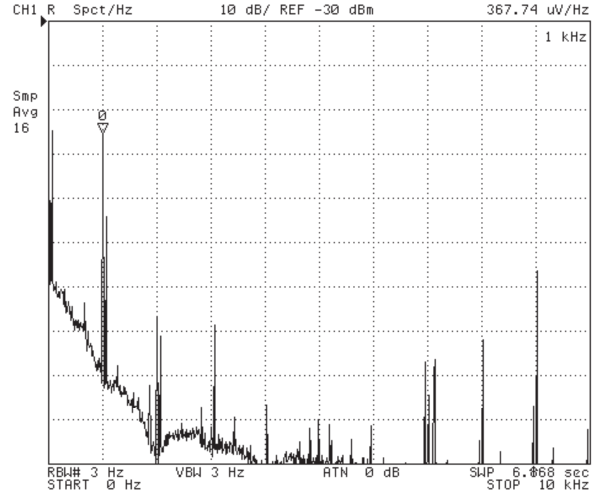


Figure 4.19: Measured output noise spectrum for the proposed SCVR.

Table 4.2 compares the proposed SCVR with other reported low-power CMOS VRs with low output ($< V_{th}$). The results show that the SCVR circuit can be implemented in standard CMOS technology and that, low output, under threshold voltage, is achieved without using any component subdivision, and is scalable.

The output voltage has satisfactory sensitivity to the temperature and supply voltage. The circuit also has advantages in nano-level power dissipation and compact silicon occupation.

Table 4.2: Comparison with other low-voltage low-power voltage reference.

	This work	Ref.[48]	Ref.[19]	Ref.[24]	Ref.[25]
Process	0.18-μm	0.35-μm	0.35 μm	0.18 μm	0.13 μm
V_{th}-NMOS V_{th}-PMOS	0.45 V -0.383 V	0.55 V -0.7 V	0.45 V	0.32 V -0.456 V	N/A
Supply voltage (V)	1.0 to 3.0	1.0 to 4.0	1.5 to 4.3	0.45 to 1.8	0.5 to 3.0
Supply current @ room temperature	$<$ 90 nA @ 1 V	250 nA @ 1 V	1200 nA @ 1.5 V	7 nA @ 0.45 V	59 pA @ 0.5 V
Vref (mV)	123.3	190.1	168	257.5	176.1
T.C. (ppm/°C) Temp range (°C)	17.6 -40 to 80	16.9 -40 to 80	25 0 to 80	165 0 to 125	5.3-47.4 -20 to 80
Line sensibility (%/V)	0.15	0.76	0.95	0.44	0.036
Chip area (mm^2)	0.03	0.049	0.08	0.043	0.0093
Component subdivision	-	Capacitors	Resistors	-	-
Trimming components	Transistors	Capacitors	Resistors	-	Transistors
Output type	Scalable	Scalable	Scalable	Constrained	Constrained
Device type	Standard	Standard	Standard	High-V_{th}	Native

4.6 Conclusion

A CMOS switched-capacitor voltage reference with body biasing technology at subthreshold operation is proposed in this paper. The low output voltage, which is below the threshold voltage, can be achieved with standard technology and without using any component subdivision. In addition, the value can be made scalable. The T.C. is 17.6 ppm/°C, the line sensitivity is approximately 0.15 %/V, and the circuit consumes power at the nano-level and occupies a small area. The influences resulting from process variations can be effectively suppressed, and the proposed trimming procedure with a composite transistor improves the T.C.. when the circuit suffers from D2D variations. The design can ensure a precise voltage reference for applications in subthreshold integrated circuits.

5

A Single-capacitor Switched CMOS Voltage Reference Using MOS Body Effect

In this chapter, we propose a novel methodology for the implementation of a switched-capacitor voltage reference. By means of the MOS body effect, the switched operation uses a single capacitor and a PMOS transistor to generate a reference voltage that has low sensitivity to temperature. The low output under the threshold voltage is achieved without the use of components dividers, which conserves the chip area. The circuit is implemented in 0.18-μm CMOS technology. Measurements show that the output voltage is approximately 121.1 mV. The temperature coefficient is approximately 35.1 ppm/°C. At room temperature, the line sensitivity is approximately 0.12 %/V, and the supply current is less than 100 nA from 1 V supply. The circuit occupies a 0.013 mm^2 chip area.

5.1 Introduction

From the reported works [44, 45, 46, 48], the implementation of SCVR circuits is based on the switched-capacitor amplifier, the structures of the switched-amplifier have two types [11]: unity-gain sampler and noninverting amplifier. The SCVR structures described in Chapter 4 mainly depend on the noninverting amplifier, as shown in Figs. 4.1, 4.2 and 4.3.

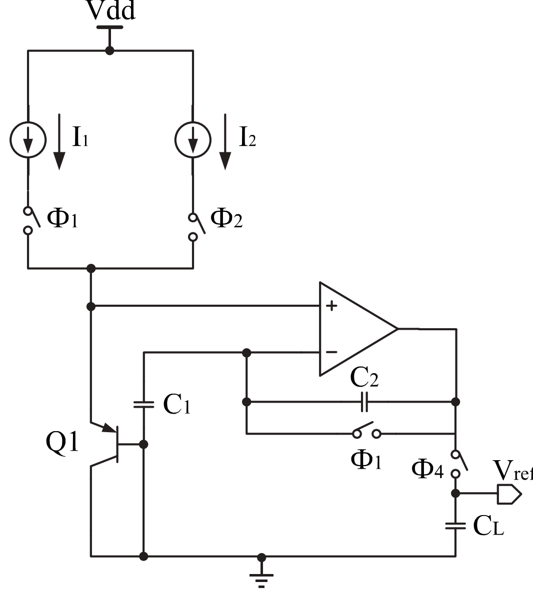


Figure 5.1: Switched-capacitor bandgap voltage reference [45].

The SCVR based on the unity-gain sampler is initially reported in [45], Fig. 5.1 shows the structure. The output voltage V_{ref} is expressed as

$$V_{ref} = V_{be} + \frac{C_1}{C_2} V_T ln\left(\frac{I_1}{I_2}\right). \tag{5.1}$$

In this structure, a bipolar transistor and two capacitors are used. The value of the output is above 1.0 V because the silicon bandgap energy is used as the reference source. And the offset of amplifier cannot be eliminated because the auto-zeroing technology is not implemented.

A sample-based reverse bandgap reference is reported in [55], the principle is briefly illustrated in Fig. 5.2, which is also based on the unit-gain sampler. The reference voltage can be given by

$$V_{ref} = \frac{C_1}{C_1 + C_2} V_{be} + V_T ln\left(\frac{I_2}{I_1}\right). \tag{5.2}$$

The low output can be achieved by using the capacitive divider, and the implementation of auto-zeroing technology cancel the offset of amplifier. However, the operations need three capacitors, such that the match between capacitors is critical to the accuracy of V_{ref} and its T.C. and the more chip area is occupied.

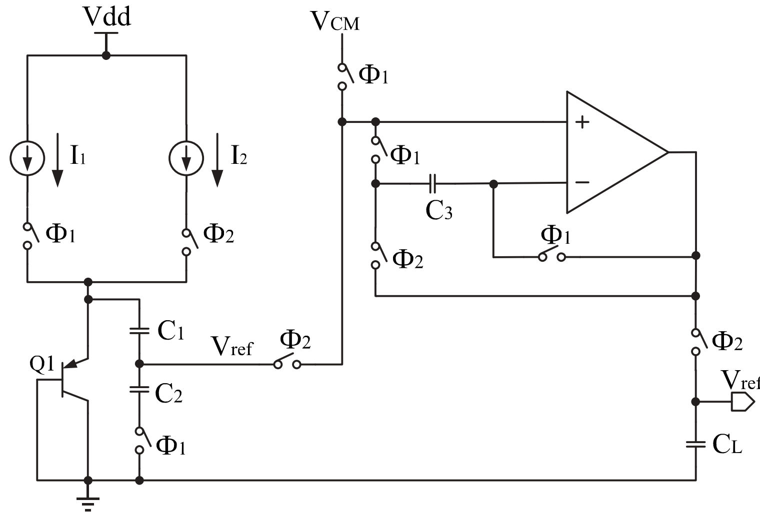


Figure 5.2: Sampled reverse bandgap principle [55].

The SCVR can be designed without the use of the amplifier [56]. The design requires two transistors, such that the mismatch degrades the performance of the voltage reference. And the operation requires more capacitors, such that the performance of V_{ref} suffers more from mismatch between capacitors, and the low output requires the large capacitive subdivision which occupies more chip area.

In Chapter 4, an ultra-low-power switched-capacitor voltage using body effect in MOSFETs is originally proposed, in which the structure is based on the noninverting amplifier. In this chapter, the methodology combining the switched-capacitor technology with body effect is used for the design of voltage reference again. Only one capacitor is required for the SCVR operation, such that the mismatch between capacitors is avoid and the chip area is saved. In section 5.2, operating principles of proposed circuit are presented. Implementation of the proposed SCVR is given in section 5.3. Considerations is discussed in section 5.4. In section 5.5, the simulation results are demonstrated. Finally, the conclusion is given in section 5.6.

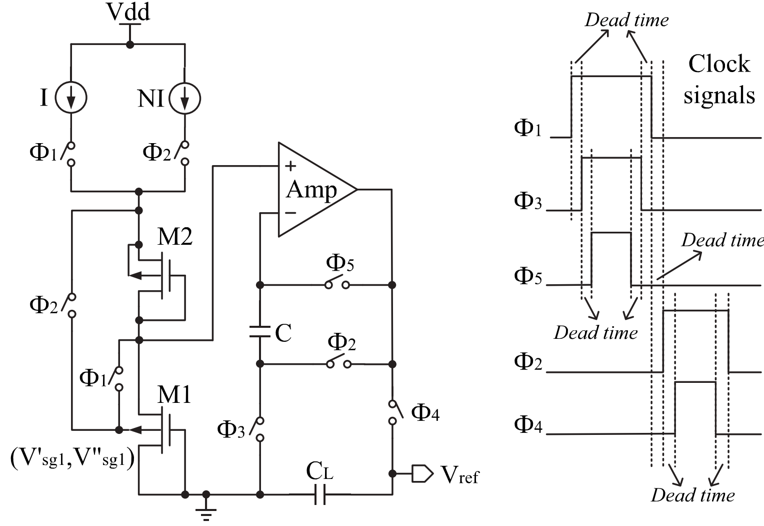


Figure 5.3: Proposed CMOS SCVR circuit using body biasing technology.

5.2 Operating Principles of Proposed Circuit

Fig. 5.3 shows the proposed SCVR circuit whose operation is based on the unit-gain sampler. The circuit is composed of a bias current circuit, a core circuit, a switched capacitor, and an operational amplifier. The switches are controlled by non-overlapping clock signals ($\Phi_1, \Phi_2, \Phi_3, \Phi_4, \Phi_5$). The core circuit inputs two different gate-source voltages (V'_{sg1} and V''_{sg1}) in M1 to the OTA during $\Phi_1 = 1$ and $\Phi_2 = 1$, respectively. As described in Chapter 4, the dead time between Φ_1 and Φ_2 ensures accurate output and to preserve power dissipation. Φ_3 is designed to turn off the switch before Φ_1 so that the stored voltage in capacitor C will be immune to the input-dependence charge injection from the switch; In addition, Φ_5 should be turned off before Φ_3 to avoid charge injection and storage on capacitor C. The dead-time region between Φ_2 and Φ_4 prevents the accuracy of V_{ref} from being impacted by the charge injection effect.

The equivalent structure of the proposed SCVR circuit is presented in Figs. 5.4(a) and (b). During the sampling state ($\Phi_1 = 1$ and $\Phi_2 = 0$), the PMOS transistor M1 is biased at a current of I and the body of M1 is connected to its source, a gate-source voltage V'_{sg1} corresponding to the current is produced, C is connected between the inverting input of the amplifier and the ground, the

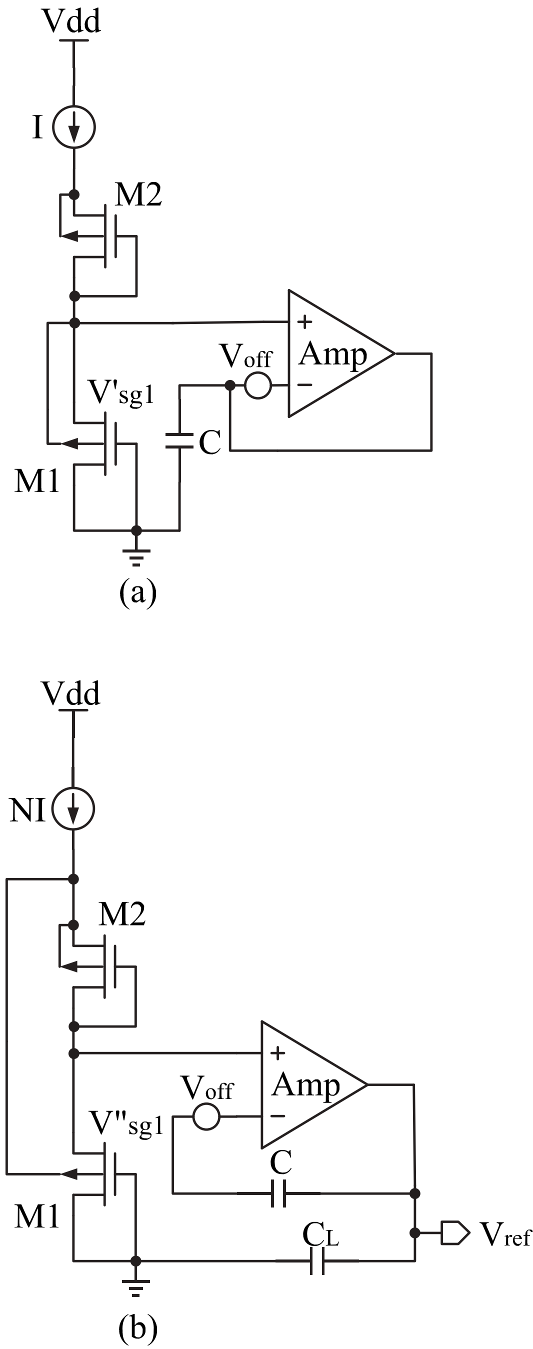


Figure 5.4: Equivalent schematic of the proposed SCVR circuit (a) when $\Phi_1 = 1$ and $\Phi_2 = 0$, (b) when $\Phi_1 = 0$ and $\Phi_2 = 1$.

output of the amplifier is directly connected to its inverting input, and the V'_{sg1} is stored on capacitor C. Next, during the hold state ($\Phi_1 = 0$ and $\Phi_2 = 1$), M1 is biased at another current of NI (N is the ratio between the two different currents) and another gate-source voltage V''_{sg1} is generated, and C is connected between the amplifier inverting input and its output, which forms a negative feedback loop. The charge (ΔQ_C) on capacitor C in terms of the offset voltage V_{off} of the amplifier is given by

$$\Delta Q_C = Q'_C - Q''_C = (V'_{sg1} - V_{off})C - (V''_{sg1} - V_{off} - V_{ref})C. \tag{5.3}$$

Using the conservation of charge principle, the transfer of the charges must be satisfied by

$$\Delta Q_C = 0. \tag{5.4}$$

With Eq.(5.3), the output reference voltage V_{ref} can be shown by the following equation:

$$V_{ref} = V''_{sg1} - V'_{sg1}. \tag{5.5}$$

From the equation, the amplifier can be auto-zeroed. Hence, the input offset is eliminated. The load capacitor C_L is off-chip to guarantee the output is valid during the sampling period. The control circuit of the switches for the non-overlapping clock signals is presented in Figs. 4.5(a) and (b). The operation is shown in Fig. 5.5. The V_{ref} is the difference between the two gate-source voltages (ΔV_{sg}) of M1 during the two phases.

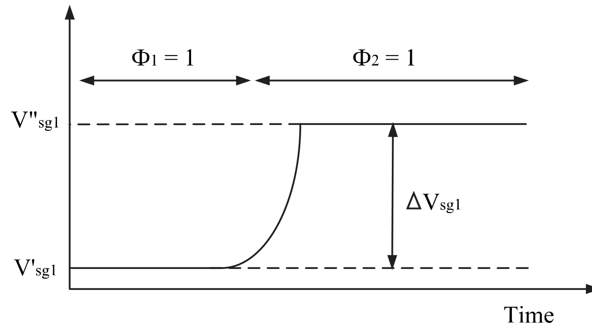


Figure 5.5: Gate-source voltage of M1 during the two phases.

As shown in Figs. 5.4 and 5.5, and transistor M1 is biased at the weak inversion during the two phases, during the sampling state ($\Phi_1 = 1$), with Eq. (2.23), V'_{sg1} is defined as

$$V'_{sg1} = V'_{th1} + nV_T ln\left(\frac{I}{K_1 I_t}\right), \tag{5.6}$$

$$V'_{th1} = V_{th0}. \tag{5.7}$$

the body of M1 is connected to the source of M2 during the hold state ($\Phi_2 = 1$) to form a reverse-bias connection; thus, V''_{sg1} is defined as

$$V''_{sg1} = V''_{th1} + nV_T ln\left(\frac{NI}{K_1 I_t}\right), \tag{5.8}$$

$$V''_{th1} = V_{th0} + \gamma\left(\sqrt{2\Phi_B + V_{bs1}} - \sqrt{2\Phi_B}\right). \tag{5.9}$$

With Eqs. (5.6) to (5.9) and $V_{bs1} = V_{sg2}$, Eq. (5.5) can be given by

$$V_{ref} = \gamma\left(\sqrt{2\Phi_B + V_{sg2}} - \sqrt{2\Phi_B}\right) + nV_T ln(N), \tag{5.10}$$

$$V_{sg2} = V_{th2} + nV_T ln\left(\frac{NI}{K_2 I_t}\right). \tag{5.11}$$

According to the analysis in Chapter 2, the first term inside the square brackets of Eq. (5.10) is CTAT and achieves a negative T.C.. The second term is proportional to the PTAT and implements a positive T.C.. And the output voltage is under the threshold voltage because the absolute value of V_{th0} in V_{ref} is canceled.

The proposed SCVR has the following advantages: The sampling-and-hold operation is implemented with only a single capacitor C and the low output does not require capacitive subdivision, whereas other SCVRs [44, 45, 46, 48, 55] depend on SC network for division and the matching of integrated capacitors to generate stable output voltages across temperature, which increases chip area in scaled processes. Moreover, the reference voltage is implemented with only one transistor (M1) in the standard process, such that the component matching errors are largely decreased, and the chip area can be saved. The auto-zeroing technique can be implemented with only one capacitor in this design, whereas others requires more [48, 55]. With the same structure of unit-gain sampler, the

input-offset amplifier can be eliminated through our operation while the offset is existing in [46]. The bias currents only require nano-ampere levels because M1 and M2 work in the subthreshold region, and the current ratio N can be selected to obtain a zero T.C..

5.3 Implementation of Proposed Circuit

As shown in Fig. 5.3, the SCVR circuit is composed of the bias current circuit, the core circuit, and the operational amplifier.

The bias current circuit [38] is shown in Fig. 5.6. All transistors work in the subthreshold region except M5 and M6, M5 is biased in the linear region and M6 is biased in the saturation region. And transistors M3-M4 determinate the value of the bias current, which can be expressed by Eq. (3.15). Cascode current mirrors in the stacked structure improve line sensitivity, but a trade-off between line regulation and low-voltage operation being necessary in this case. For the subthreshold operation in current mirrors and the saturation operation in M8, the minimum supply voltage must ensure $V_{sd} > 4V_T$ and $V_{gs6} > V_{th6}$. Thus, the minimum supply voltage can be redistributed as the sum of two drain-source voltages V_{ds} and a gate-source voltage V_{gs6} in the branches of the circuit ($V_{dd} > V_{th6} + 8V_T$).

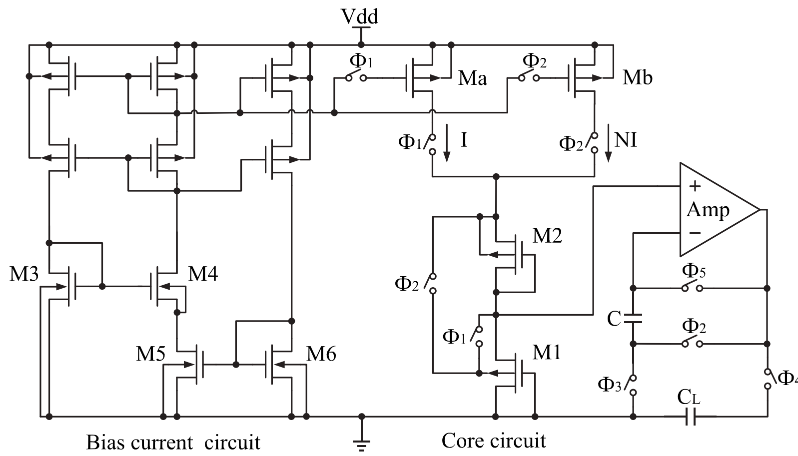


Figure 5.6: Proposed switched-capacitor voltage reference circuit.

From Fig. 5.3, the core circuit is composed of transistors M1 and M2, capacitor C and switches. The zero T.C. can be obtain from Eq. (4.15). Thus, by differentiating Eq. (5.10) with respect to temperature, the temperature dependence of the SCVR can be given by

$$\frac{1}{2}\gamma\left[(2\Phi_B(T_0)+V_{sg2}(T_0))^{-\frac{1}{2}}\left(2\frac{\partial\Phi_B}{\partial T}+\frac{\partial V_{sg2}}{\partial T}\right)\right.$$
$$\left.-(2\Phi_B(T_0))^{-\frac{1}{2}}\left(2\frac{\partial\Phi_B}{\partial T}\right)\right]+n\frac{V_T}{T}ln(N)\Bigg\}=0 \tag{5.12}$$

As described in Chapter 2, the first term in the brace has a negative T.C., whereas the thermal voltage V_T has a positive T.C. in the second term. Hence, a zero T.C. can be achieved by choosing an adaptive biased-current ratio N which can be calculated from

$$N = \exp\left\{\frac{\gamma T}{2nV_T}\left[2\Phi_B(T_0)^{-\frac{1}{2}}\left(2\frac{\partial\Phi_B}{\partial T}\right)\right.\right.$$
$$\left.\left.-(2\Phi_B(T_0)+V_{sg2}(T_0))^{-\frac{1}{2}}\left(2\frac{\partial\Phi_B}{\partial T}+\frac{\partial V_{sg2}}{\partial T}\right)\right]\right\} \tag{5.13}$$

Fig. 5.7 shows the schematic of the amplifier, transistors $M_{o3} - M_{06}$ consist the fold-cascode structure to obtain a high voltage gain, thereby enhancing the

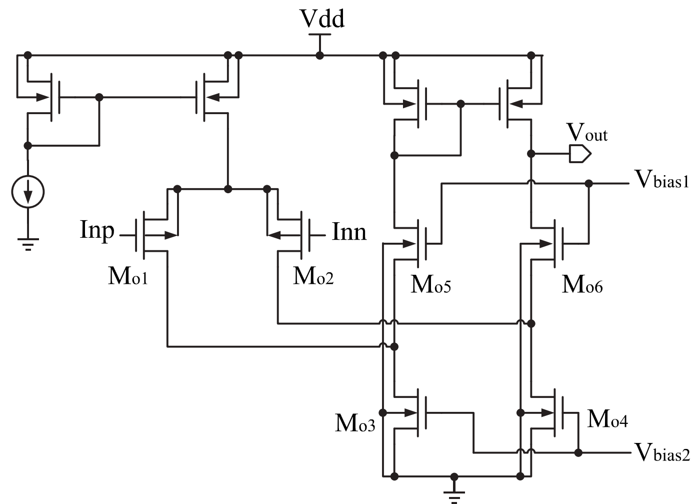


Figure 5.7: Operational amplifier.

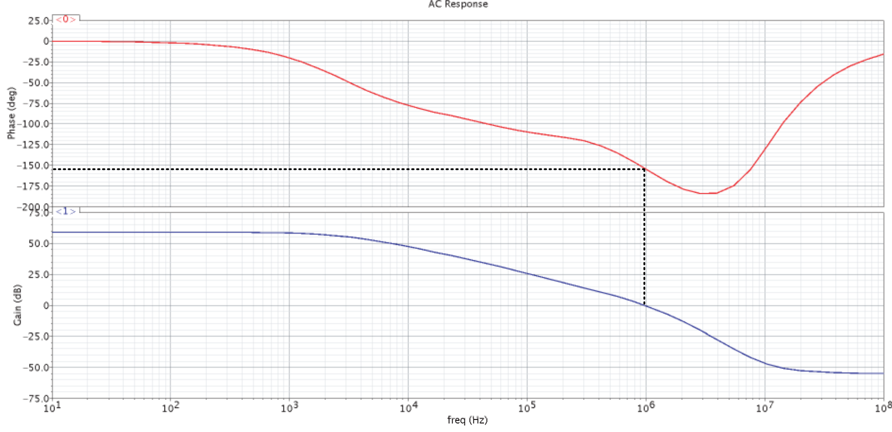


Figure 5.8: Simulated gain and phase response.

precision and speed of the switched-capacitor amplifier. The OTA can be operated with a nano-current supply. The simulated frequency response is shown in Fig. 5.8, the gain of amplifier is approximately 58 dB when V_{dd} is 1 V.

5.4 Design Considerations

The main consider in our design is the process variations, as discussed in section 4.4 in Chapter 4. For the core circuit in this study, the influence of WID variation (σV_{th}) decreases because only one transistor is used for the voltage reference generator. And the mismatch of capacitors is avoid because only one capacitor is used. However, according to Eq. (5.10), D2D variations cannot be avoided. The influence of ΔV_{th} is dominant because V_{th} is sensitive to process variations, which leads to spreads in the output voltage and in the T.C. according to Eqs. (5.10) and (5.12).

Therefore, current trimming must be implemented to correct the temperature slope (compensate for the T.C. variation), which means the size ratio N should be adjustable after chip fabrication. Composite transistor [42] is an effective method to implement the trimming work, Fig. 5.9 shows the operation, the resolution is 2%. The aspect ratios of Mb can be changed by digital logic control to adjust the T.C.. In this design, the scalable output cannot be implemented because only

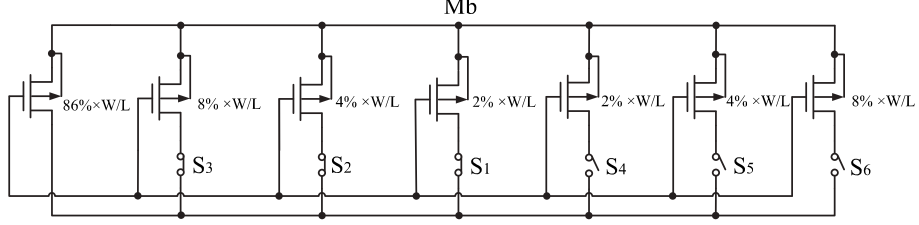


Figure 5.9: Composite structure of Mb for trimming T.C..

one capacitor is used. Comparing with the proposed design shown in Fig. 4.3 in Chapter 4, the spread of V_{ref} cannot be further reduced when the zero T.C. is obtained by the trimming implementation.

NMOS transistors are used as switches (S_1 to S_6). In production lines, one-time-programmable (OTP) memories such as fuses can be used to control the switches with minimal power consumption [51]. The required trimming code can be calculated as following procedures. First, as depicted in Section 4.4.3 in Chapter 4, the slope S_u can be defined as

$$S_u = P + n\frac{V_T}{T}ln(N), \tag{5.14}$$

where

$$P = \frac{1}{2}\gamma\left[(2\Phi_B(T_0) + V_{sg2}(T_0))^{-\frac{1}{2}}\left(2\frac{\partial\Phi_B}{\partial T} + \frac{\partial V_{sg2}}{\partial T}\right) - (2\Phi_B(T_0))^{-\frac{1}{2}}\left(2\frac{\partial\Phi_B}{\partial T}\right)\right].$$

To obtain the zero T.C., N should be adjusted to compensate for the slope; then, Eq. (5.14) is expressed by

$$P + n\frac{V_T}{T}ln(N + \Delta N) = 0, \tag{5.15}$$

where ΔN is the required range for trimming, and the n and T.C. of V_T are assumed to have minimal sensitivity to the process variation. With Eqs. (5.14) and (5.15), the required trimming code can be calculated by

$$\frac{\Delta N}{N} = \exp\left(-\frac{S_u q}{nk}\right) - 1. \tag{5.16}$$

5.5 Simulations and Measurements

The proposed SCVR circuit is implemented in the standard CMOS 0.18 μm technology. Because only a single capacitor is required for the operation, the accuracy of capacitor is not necessary. Hence, the MOS transistor as a capacitor [11] can be used to save the chip area. The clock frequency is 1 kHz, and the off-chip capacitor C_L used for the output filter capacitor is 100 pF. Fig. 5.10 shows the simulated transient responses, the ripple, which is caused by the leakage current (as analyzed in Section 4.4.3 in Chapter 4), is approximately 0.16 mV.

Fig. 5.11 presents the simulated temperature dependence at different corners. The solid lines illustrate the temperature performance when the process variations are considered, the variation ΔV_{th} leads to the no-zero T.C. if a zero T.C. is achieved at TT style, the reason is given in Section 4.4.4 in Chapter 4. The dash lines evaluates the trimming capacity by using the composite transistor. The positive T.C. in SS style can be changed to a negative one with the lowest code, and the negative T.C. can be altered to a positive one at the highest code. Hence, the resolution and range is enough to compensate for the T.C. within the variation range, and the spread of output also can be minimized by this trimming implementation.

Fig. 5.12 shows the chip die of the proposed SCVR circuit, the chip area is approximately 0.013 mm^2. Fig. 5.13 presents the temperature characteristics of the output voltage at 1 V to 2.5 V supply voltage. At Vdd =1.0 V, the output voltage is approximately 121.1 mV at room temperature, and the T.C. after trimming is approximately 35.1 ppm/°C. The measurement line sensitivity is approximately 0.12 %/V at room temperature. The measured results of the switched CMOS VR for five samples after trimming are shown in Fig. 5.14, the T.C. ranges from 34 ppm/°C to 38.9 ppm/°C.

Table 5.1 compares the proposed SCVR with other reported low-power VRs with low output ($< V_{th}$) implemented in standard CMOS technology. The comparing results show that the proposed SCVR circuit can generate a low output under the threshold voltage without any component subdivision. The output voltage has competitive T.C. and line sensitivity, and the power dissipation and chip area occupation are also comparable to the other VRs.

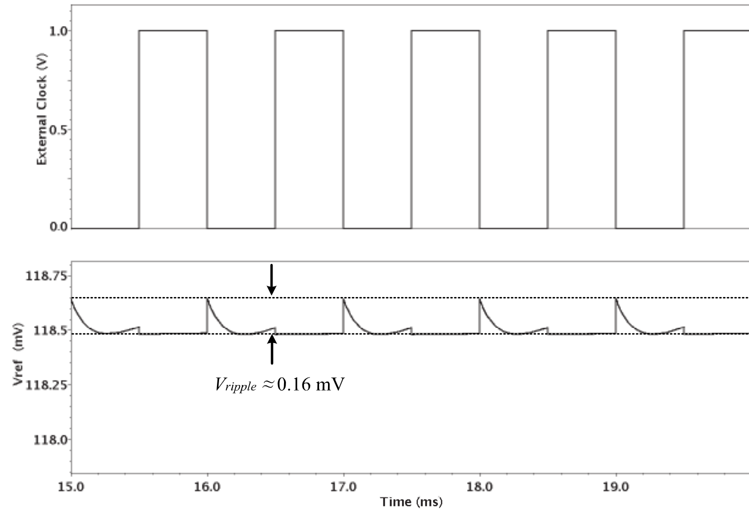


Figure 5.10: Simulated output waveforms when C_L is 100 pF at 80 °C.

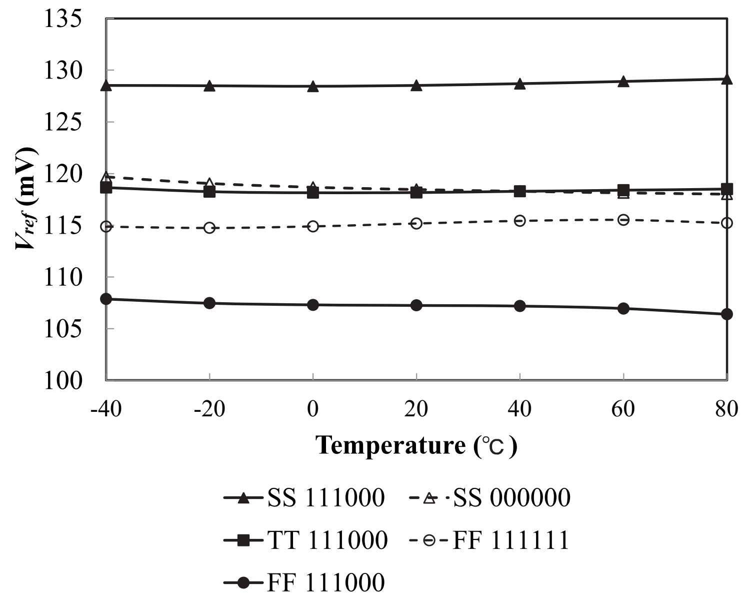


Figure 5.11: Simulated V_{ref} as a function of temperature at different corners at Vdd = 1.0 V. TT: typical PMOS/typical NMOS; SS:slow PMOS/slow NMOS; FF: fast PMOS/fast NMOS.

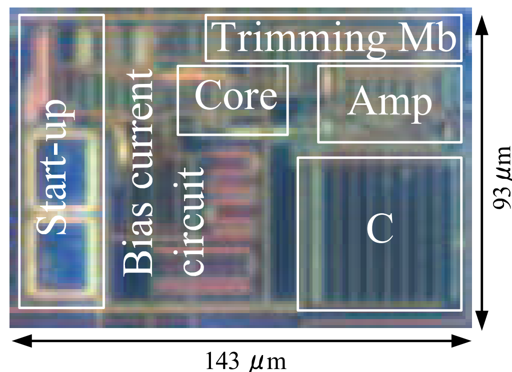


Figure 5.12: Chip die of the proposed SCVR.

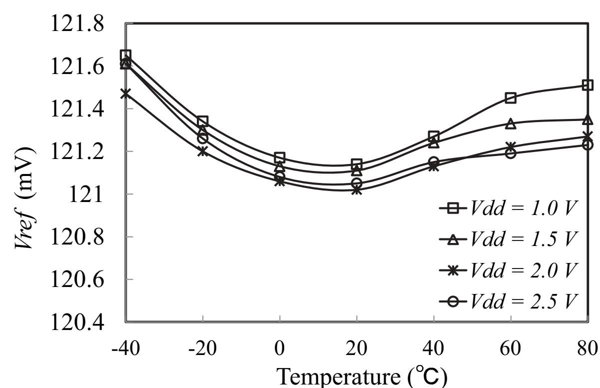


Figure 5.13: V_{ref} as a function of temperature at different supply voltages.

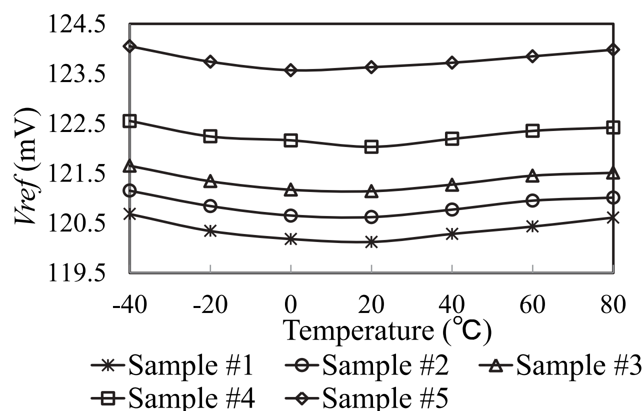


Figure 5.14: Measured V_{ref} versus temperature for five samples at Vdd = 1.0 V.

Table 5.1: Comparison with other low-voltage low-power voltage reference.

	This work	Ref.[48]	Ref.[19]	Ref.[55]	Ref.[56]
Process	0.18-μm	0.35-μm	0.35 μm	0.13 μm	0.065 μm
V_{th}-NMOS V_{th}-PMOS	0.45 V -0.383 V	0.55 V -0.7 V	0.45 V	0.3 V -0.4 V	N/A
Supply voltage (V)	1.0 to 2.5	1.0 to 4.0	1.5 to 4.3	0.75 to 1.6	0.75
Supply current @ room temperature	104 nA @ 1 V	250 nA @ 1 V	1200 nA @ 1.5 V	227 nA @ 0.75 V	138 nA @ 0.75 V
Vref (mV)	121.1	190.1	168	256	423
T.C. (ppm/°C) Temp range (°C)	35.1 -40 to 80	16.9 -40 to 80	25 0 to 80	40 -40 to 85	160 -35 to 80
Line sensibility (%/V)	0.12	0.76	0.95	0.005	N/A
Chip area (mm^2)	0.013	0.049	0.08	0.07	0.0055
Component subdivision	No	Capacitors	Resistors	Capacitors	Capacitors
Trimming components	Transistors	Capacitors	Resistors	Transistors	Transistors
Reference type	MOS	MOS	MOS	Diode	Diode

5.6 Conclusion

The growing interest in subthreshold LSI has generated a demand for low reference voltage below the threshold voltage and power dissipation in nano-level range in VR circuits, a novel CMOS voltage reference is introduced in this chapter. Combining the switched-capacitor technology with the body-biasing technique in MOSFET, the circuit is implemented in standard CMOS technology. Comparing to prior SCVR designs, the operation in proposed circuit requires only one capacitor and one transistor, thereby further suppressing the influence resulting from process variations and saving the chip occupation. The T.C. is approximately 35.1 ppm/°C, and the line sensitivity is about 0.12 %/V. The supply current is dozens of nano amperes. And the trimming procedure with a composite transistor can ensure the zero T.C. even if the circuit suffers from process variations. This work illustrates a novel approach that enable the SCVR design with low output voltage and ultra-low-power dissipation.

6

Conclusions and future works

Body-biasing effect is effective and popular for the implementation of the ultra-low-voltage ultra-low-power integrated circuit in CMOS technology. In this dissertation, the method is originally explored for the design of voltage references for application in subthreshold LSI. The body biasing scheme in MOS transistor has two types: forward body bias and reverse body bias. These two directions are used for the implementation of the voltage references.

Detail analysis of the principle for compensating T.C. by using both forward body bias and reverse body bias in MOSFETs is presented. An improved design based on the self-biased architecture can remove the amplifier and resistor in traditional structure, thereby saving the power dissipation and area occupation.

Based on the difference between two gate-source voltages in the self-cascode MOSFET structure operated in the subthreshold region with a self-biased (forward-biased) body effect, an all-MOSFETs VR is proposed. This circuit can produce a low output voltage without threshold restriction in standard CMOS technology. The influence results from process variations is considered, and the trimming procedures are implemented. The circuit is designed with only MOSFETs and fabricated in standard 0.18-μm CMOS technology, the measurement results show that the value of the reference voltage is under the threshold voltage. The zero T.C. can be achieved after trimming, and the circuit has the perfect line sensitivity. The ultra-low power dissipation and compact area occupation are also among the advantages of the proposed VR for application in low-voltage low-power subthreshold LSI.

For the VR using the reverse body effect, the promising solution is the usage of switched-capacitor technology. A combination of body-biasing technique and switched-capacitor technique for the implementation of ultra-low-power VR is first developed in this dissertation.

A novel CMOS SCVR with body biasing technology at subthreshold region is proposed, the operation is based on the structure of the noninverting amplifier. The low output voltage, which is below the threshold voltage, can be achieved with standard technology and without using any component subdivision. In addition, the value can be made scalable by choosing the different capacitive ratio. The trimming procedure is implemented, and the method to determine the required trimming code is also presented. The noise analysis in the SCVR circuit is discussed in detail. The chip is implemented in 0.18 μm standard CMOS technology. Measurement results show that the proposed circuit has satisfied T.C. and line sensitivity, and the circuit consumes power at the nano-level range and occupies a small area. The influences resulting from process variations can be effectively suppressed, and the proposed trimming procedure with a composite transistor improves the T.C. when the circuit suffers from D2D variations. The design can ensure a precise voltage reference for applications in subthreshold integrated circuits.

Based on the unity-gain sampler, a novel structure of SCVR circuit is implemented by combining the switched-capacitor technology with the body-biasing technique in MOSFET in standard CMOS process. Comparing to prior SCVR designs, the operation in proposed circuit requires only one capacitor and one transistor, thereby further suppressing the influence resulting from process variations and saving the chip occupation. According to the measurement results, the low T.C. can be achieved, and the circuit also has the competitive line sensitivity. The supply current needs dozens of nano amperes. And the trimming procedure with a composite transistor can ensure the zero T.C. even if the circuit suffers from process variations. This work illustrates a novel approach that enable the SCVR design with low output voltage as well as ultra-low-power dissipation.

Together, the developed design technologies for the implementation of the ultra-low-power voltage references in this dissertation make it advantageous for application in subthreshold designs.

The supply voltage should be further reduced in future work, the minimum supply voltage of these designs in this dissertation is mainly limited by the biased-current circuit. The reason is the use of transistor operated in saturation region, the minimum supply voltage must be larger than threshold voltage at low temperature where the threshold voltage increases. Hence, the saturated device in the biased-current circuit is removed or replaced, the voltage reference circuit can be operated at lower supply voltage. And it is better that the operation can be implemented in standard CMOS technology. According to Figs. 3.10 and 4.17, supply current should be reduced at high temperature because the leakage current increases when the temperature raises, especially in other CMOS technology, e.g., 65 nm, 28nm. For these processes, with small threshold voltage, the minimum supply voltage can be obtained. However, the increasing leakage current, especially at high temperature, should be considered. Finally, some circuits, such as LDO, DC-DC converters, can be considered with embedded voltage references proposed in this dissertation.

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