Waseda University Doctoral Dissertation

Study on High Efficiency CMOS Rectifiers for Energy Harvesting and Wireless Power Transfer Systems

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The field of vibration energy harvesting and wireless power transfer technologies are growing rapidly in recent years, which are largely stimulated by the advances of different researches, such as piezoelectronic vibration harvester and biomedical implant devices. They play a more and more important role in renewable resources and sensor systems. Among the components constituting the two systems, rectifier as the interface circuit is a critical part and it is quite significant to promote their performances.

Rectifier in vibration energy harvesting system is utilized to change the AC power generated by piezoelectronic generator to DC one. Commonly, the typical working frequency of the generator is from mHz to kHz. Conventional rectifiers consisting of diode-connected transistors in CMOS integrated circuits are not suitable for this application considering the big forward voltage drop and poor efficiency. The output voltage amplitude of different micro harvesting generators may vary and output voltage and power are usually low. Therefore, both low power, low voltage and wide input voltage amplitude range are needed for the rectifier in vibration energy harvesting system. By using the bulk-driven comparator technique, a paper published in TCAS2011 reduced the minimum operation voltage to 0.5 V. Another research in NOLTA2012 further improved the minimum input voltage to as small as 0.3 V with similar concept. Both researches filled the rectifiers gap in the field of low voltage energy harvesting system. However, the drawbacks of the bulk-driven techniques are also obvious. Body diode is easily to be turned on when reverse voltage is larger than 0.7 V. This phenomenon decides that the maximum operation voltage of the rectifiers proposed in the above two papers are smaller than 1 V. Besides the energy harvesting, rectifier for wireless power transfer is also a key research in the power transfer system, especially for the biomedical implant devices. In this case, the rectifier integrated in the receiver rectifies the signals and powers the implant device. The distance between two coils and the relative position of coils center influence the transfer efficiency. Far distance and the position mismatch result in small received voltage amplitude. Thus, minimum operation voltage of the rectifier should be as low as enough to avoid the influence caused by poor coupling.

On the other hand, higher performance of the rectifier means higher total efficiency. Rectifier consisting of active diode for wireless power transfer was first proposed in ISCAS2005 to replace the conventional diode-connected MOS rectifiers. Comparator is used to control a switch, which works as an ideal diode without voltage drop. These active rectifiers are much frequency dependent. High frequency will result in reverse current if the control circuit cannot response quickly, which reducing the conversion efficiency. A 100 kHz, 1.2 V rectifier with reverse current consideration was first proposed in JSSC2009. Considering the influence of poor coil coupling, the operation voltage is not small enough. In the case of higher frequency of 13.56 MHz, both passive and active rectifiers can be used. In the design of passive rectifiers, threshold voltage cancellation technology is commonly used (TBCAS2012). However, the utilization of capacitors increases chip area and all these circuits are investigated for low input signal applications, where current direction is not controlled. Though the active rectifier proposed in TCAS2012 can control the current direction, the time delay of the comparator with a common gate structure results in the reverse current and poor power efficiency. Basing on the above considerations and drawbacks of previous researches, three novel rectifier circuits that focus on different issues have been proposed in this dissertation, respectively.

The dissertation is organized with five chapters as follows.

In Chapter 1, the application background and different topologies of previous researches are briefly introduced. Then the motivations and objective of this dissertation are presented based on the drawbacks of previous designs. The last section of this chapter is the organization of this dissertation.

In Chapter 2, a low voltage CMOS active rectifier is proposed. This structure is designed for transcutaneous power transmission in low power battery-less devices such as biomedical implants. By using a simple comparator-controlled switch that needs a small supply voltage, the lowest input voltage amplitude can be reduced to 0.7 V with a standard CMOS 0.18 μm process, which is much smaller than 1.2 V in previous researches. Comparing with traditional diode bridge structure, the proposed rectifier uses only one comparator and a negative voltage converter. This proposed design dramatically

reduces the power loss. In combination with current offset bias circuit, the reverse current of the rectifier under different input amplitudes is minimized. The proposed circuit is measured with an input source frequency from 100 kHz to 1.5MHz and a load of 500 Ω. The measurement results show that the proposed rectifier can achieve a maximum peak voltage conversion efficiency of more than 88% and a power efficiency of approximately 86.5%. The performances are improved comparing with the measured voltage conversion efficiency of 86% and simulated power efficiency of 87% in the paper of JSSC2009.

In Chapter 3, a wide input amplitude range and highly efficient CMOS rectifier for low power energy harvesting system is proposed. The working frequency is from 10 Hz to 1 kHz. Comparing with previous design with bulk-driven comparator, the proposed rectifier utilizes full bridge structure and source-driven comparator is used in the novel active diode. Body diode is always reversely biased even the input voltage is higher than 1 V, which makes the rectifier work at a wide range of input voltage amplitudes of 0.45 V up to 1.8 V under a standard 0.18 μm CMOS process. The comparator that consists of common-gate stage and control stage is biased to weak inversion region to control the switch of the active diode. This technology reduces the minimum operation voltage to as low as 0.45 V. The proposed rectifier can achieve a peak voltage conversion efficiency of over 96% and a power efficiency over 90% with a load value of 50 kΩ. Simulated power consumption of the rectifier is 264.35 nW with a 500 mV input, which is about 30% smaller than the best recently published results (TCAS2011). The power transistors used in the rectifier are only 1/3 of the previous design. Smaller transistors result in better efficiency and help to save the chip area.

In Chapter 4, a 1 V, high efficiency comparator-based CMOS rectifier for wireless power transfer in biomedical applications is presented. A novel active diode controlled by a cross-coupled comparator is designed to overcome the common-mode voltage limit of traditional structure and improve the conversion efficiency. Reverse current is also reduced by utilizing a switch off response compensation technique considering the charge delay caused by large gate-capacitor of the switch transistors and high frequency. The switch off response compensation technique can not only reduce the reverse current but also maximize

the conduction time of the active diode by using a SR latch circuit. The proposed rectifier is verified using a standard 0.18 μm CMOS process with an input source frequency of 13.56 MHz. Results show that the rectifier can achieve a maximum voltage conversion efficiency of 92% and power efficiency about 86% with a load value of 500 Ω. Simulated power consumption of the rectifier is only 0.259 mW with a 1 V peak input voltage. Though the minimum operation voltage in previous paper can be as low as 0.8 V by using Vth cancellation technology, the voltage efficiency is only 37.5% even with a light load of 2 kΩ.

In Chapter 5, the conclusions of this dissertation are given.

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Chapter 1

Introduction

1.1 Background

1.1.1 Rectifier devices and circuits

A rectifier is an electrical and electronic device, which is widely utilized in different applications. The function of a rectifier is to convert AC (alternating current) source to DC (direct current) ones, which is known as rectification. The first generation of rectifier is made of vacuum tube diode and copper oxide metal. The two technologies were widely used before the development of semiconductor industry. With the development of semiconductor technology, the rectifier consisting of vacuum tube diode gradually fade out the market. The traditional rectifiers can only be found in some vacuum tube audio equipment. Instead, the semiconductor diode, such as p-n junction diode and schottky diode became popular in the power rectification applications of both low current and high current fields. With the development of integrated CMOS technology, the diode connected MOS transistors are widely used in integrated circuits in place of the discrete diode components.

Rectifiers can be divided into multi phase rectifier and single phase rectifier. Three phase (multi phase) rectifier circuits are very important for industrial application and high voltage DC energy transmission. However, most rectifiers for domestic equipment are

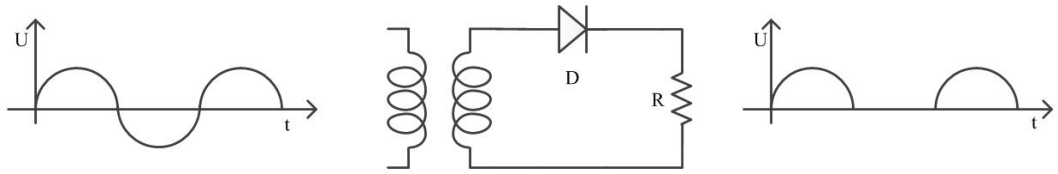


Figure 1.1: Half wave rectifier [1].

single phase, especially for low power, low voltage integrated circuits. Considering our research topics, we only focus on the single phase rectifier in this dissertation.

Single phase rectifiers can be divided into two types: half wave rectifier and full wave rectifier. For the half wave rectifier, the function of rectification is only available in the positive half cycle or negative half cycle, and the other cycle is blocked, which is shown in Fig. 1.1. These drawbacks decide that the average output voltage is not high, because half cycle of the input source is wasted and only one half is used to charge the output capacitor. Half wave rectification requires a single diode in a single phase supply. The output voltage ripple of the half wave rectifier is larger than the full wave rectifier. Thus, there should be much more filtering techniques used in the output terminal to overcome the AC frequency harmonics.

A full wave rectifier converts the whole cycle of the input AC source to DC by using two conductive branches. Each branch rectifies one half of the whole cycle, but only one constant terminal is charged as its output. The function is shown in Fig. 2.2. The output voltage is much higher than the half wave type, because both the negative and positive waveforms are passed to the output and converted to direct current. That's why the full wave rectifier structure is widely used in CMOS integrated circuits design.

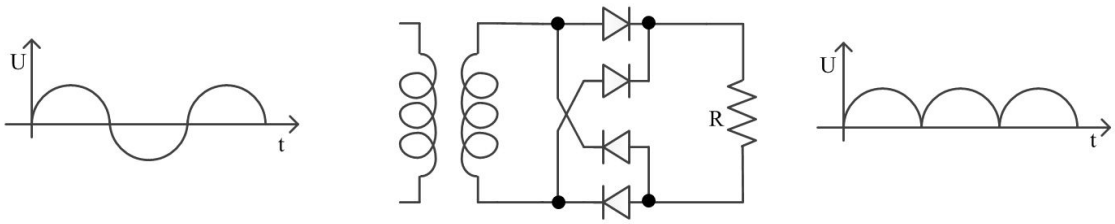


Figure 1.2: Full wave rectifier [1].

1.1.2 Rectifier applications

The field of energy harvesting and wireless power transfer are two hot topics recently, which are stimulated by the advances of different researches [2], [3], [4], [5], [6], [7], [8]. In both applications, rectifiers play a very important role in the interface circuit to convert the AC sources to DC sources and power the load system. The performance and efficiency of the rectifier influence the system a lot.

Energy harvesting technology is the process by which energy is derived from external sources, such as solar power, thermal energy, wind energy, salinity gradients and kinetic energy. The power is captured and stored for small and wireless autonomous devices, like those used in wearable electronics and wireless sensor networks. Comparing with conventional battery power systems, energy harvesting device has a long lifetime and is widely used in the system which is difficult to access to. Besides the battery, the input fuel (oil, coal, etc) wasted by the large size generator is also un-ignored. Comparing with these limited sources, the energy source harvested from environment is free and ambient. For instance, the solar energy is ambient and can be harvested by the solar panel every day and vibration energy exists from operating engines and moving devices. Among different types of energy harvesting technologies [9], [10], [11], vibration energy harvesting technology attracts a great of interests by its widely applications. Vibration energy harvesting is well suited for technical environment, such as engines and railroad bridges. Commonly, vibration energy harvesters convert mechanical vibrational energy into alternating electrical energy, thus rectifier is needed to change the AC source to DC one, which can be used

to drive a multitude of load systems or recharge a battery. Moreover, the output voltage amplitude of different micro harvesting generators may vary and output power is usually low, therefore both efficiency and wide input amplitude range are needed for the rectifier design. Thus, the rectifier plays a very important role in the vibration energy harvesting circuit interface.

Wireless energy transmission or wireless power transfer technology is to transfer the power from a supply source to the consuming devices. The power is commonly transferred through coupling coils without using solid wire or conductor [12], [13]. There are a number of technologies for wireless power transfer. Most of them are using time varying electromagnetic field as the transmission mediums [13], [14], [15]. The development of wireless power transmission does a great help to the devices which are inconvenient to be powered by interconnecting wires, especially for the application of biomedical implant devices and monitoring devices in some severe environment.

Wireless power can be transferred and power one or more devices. Power source is commonly connected to the transmitter device. Coil in the transmitter transmits the power through the electromagnetic field across some intervening space to the coil in the receiver [15]. The transfer voltages or currents are alternating sources, which cannot directly power the load circuit.

Commonly, there are two types of wireless power techniques [16]: radiative and non radiative. The radiative technique is also called far field technique or power beaming. Because the power is transferred through electromagnetic radiation like laser beam or microwave. The big merit of radiative technique is the longer transfer distances. However the energy should be aimed in the receiver. Wireless powered drone aircraft and solar power satellite are well known as the applications for radiative types. However, an unsolved issue for the radiative type still limits its application. For the longer transfer distance people and other living things exposure themselves to the potentially injurious electromagnetic field, which is a big risk to them. The other type of non radiative or near field techniques is commonly utilized in the power transmission for short distance. The energy is transferred by using inductive coupling coils or capacitive coupling electrodes through magnetic field

or electric field [17]. The applications of near field type are widely found in daily life, such as wireless charged cars, wireless toothbrush charger and RFID tag. This technique can be also utilized for implantable medical devices like implanted hearing-aid, heart pacemakers and blood flow monitor. Recently, most of researches focus on the wireless charge for these hand-held computing devices and implantable devices without tethered to the wall plug.

Among different applications of wireless power transfer technology, the development of implantable biomedical devices is enabled by the advances in the field of neural recording [18], cochlear implants [19], and blood flow sensing. Wireless power supply for implantable biomedical devices are very important, considering the critical issue of the consistent power supply, where stable and long life time power are two important factors. Conventional power method of using a battery should be avoided due to the short life time, periodical replacement and large size, which is bad to human being's healthy. By using the power transfer technology, sustained power can be supplied to the implant devices. However power received by the receiver is commonly alternation source, rectifier is needed to convert the AC source to DC source. Rectified DC power is then supplied to the load circuit and charges the battery. Thus, the performance of the rectifier is very important in the whole system design due to several reasons:

1. Voltage efficiency: The rectifier converts the AC voltage supplied by the receiver to DC voltage and powers the load circuit. The voltage efficiency of the rectifier decides the output voltage. Higher efficiency means larger output voltage;

2. Minimum operation voltage: The rectifier used in the application must be self-biased. The voltage received from the receiver is not only the rectified signal. The peak amplitude of the input source also influences the output voltage. As introduced in the above, inductive coupling between coils or capacitive coupling are the two main technologies for the near field applications. The distance between the two coils and the relative position of coil center influence the transfer efficiency. Farer distance of two coils and the position mismatch of the coil's center result in small transfer voltage, which means the voltage amplitude received by the receiver will be

influenced a lot. Thus, a low voltage rectifier can cover the influence caused by the capacitive coupling or inductive coupling coils mismatch;

3. Power efficiency: Wireless power transmission system consists of power amplifier, inductive coil, rectifier and regulator. It is important to mention that the efficiency of the rectifier is usually the bottleneck. Higher power efficiency means higher total efficiency;

4. Working frequency: As introduced above, there are two categories of the wireless power techniques, near-field and radiative. The working frequency chosen for the system is also very important. The working frequency should not be too low considering of the coil's size in the receiver if it is utilized in the biomedical implant devices. However, it should also not be too high for avoiding the potential hazards to human safety.

Based on the above considerations, rectifier plays a very important role in the application of energy harvesting system and wireless power transfer system. The performance of the rectifier decides the efficiency of the system.

1.1.3 Topologies of previous researches

The history of rectifier goes back to 1928. A device of electrolytic rectifier was patented by G. W. Carpenter in 1928 [20]. But it would be only suited to the use of low voltage applications, because the breakdown voltage of these rectifiers are very low and the electric shock is easy to happen, which is a big risk. With the development of semiconductor technology, discrete component was induced. Rectifiers achieved by diodes and capacitors were widely used. The half-wave rectifier consists of a single diode and very simple. The full wave rectifier composed of diode bridge makes full use of the input source, because both the negative and positive period pass to the load. Thus, the output ripple is much smaller than the half wave rectifier. The diode structure rectifier is always used in high supply voltage field. However, it is seldom used in low voltage systems because

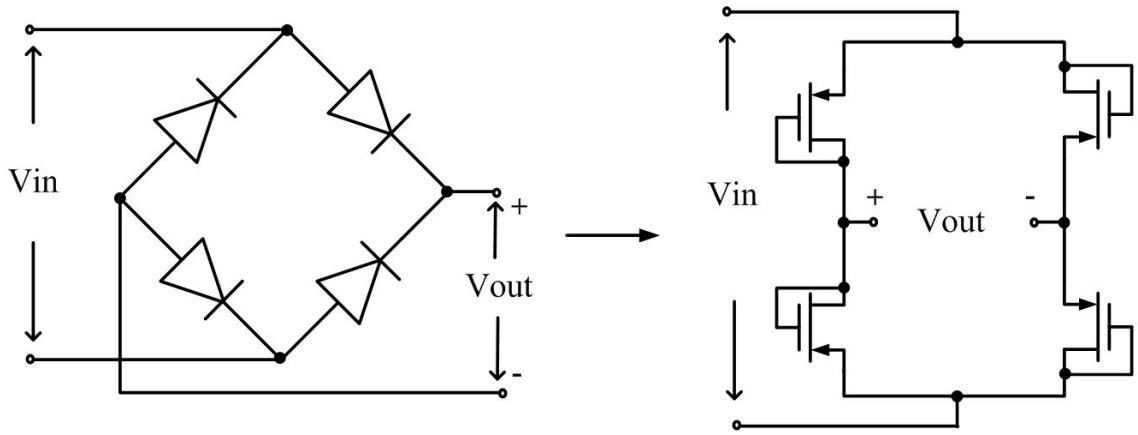


Figure 1.3: CMOS rectifier with diode configuration.

of the large forward voltage loss (typically 0.7 V-1 V), which cannot be accepted in low voltage integrated systems. Though schottky diode with a low forward voltage drop can replace the common diode to improve the voltage conversion efficiency, the high production cost and high reverse leakage current block its uses. Since integrated circuit is developing day by day, circuit designers try to implement different kinds of discrete components in the integrated circuits. In CMOS implementation circuits, discrete diode can be replaced by CMOS transistors in diode-connected configuration, which is given in Fig. 1.3. However, the voltage conversion and power efficiency are not sufficient because of the two diode forward voltage drops still exist. The voltage drop on each diode-connected MOS transistors is one V_{GS} and the minimum V_{GS} can be reduced to one V_{th} (the threshold voltage). Low threshold voltage transistor can be utilized to further reduce the operation voltage. However the additional masks and fabrication steps increase the process cost.

In [21], the author used a cross coupled structure to replace two semiconductor diodes of the diode-bridge structure, which is shown in Fig. 1.4. Input AC source is directly connected to the gate terminals to drive the NMOS transistors. When the input voltage amplitude is larger than V_{th}, one of the two NMOS transistors will be turned on depending on the input source phase. Two diode-connected transistors work as switches. They turn off to block the reverse current when input source amplitude is smaller than the output voltage

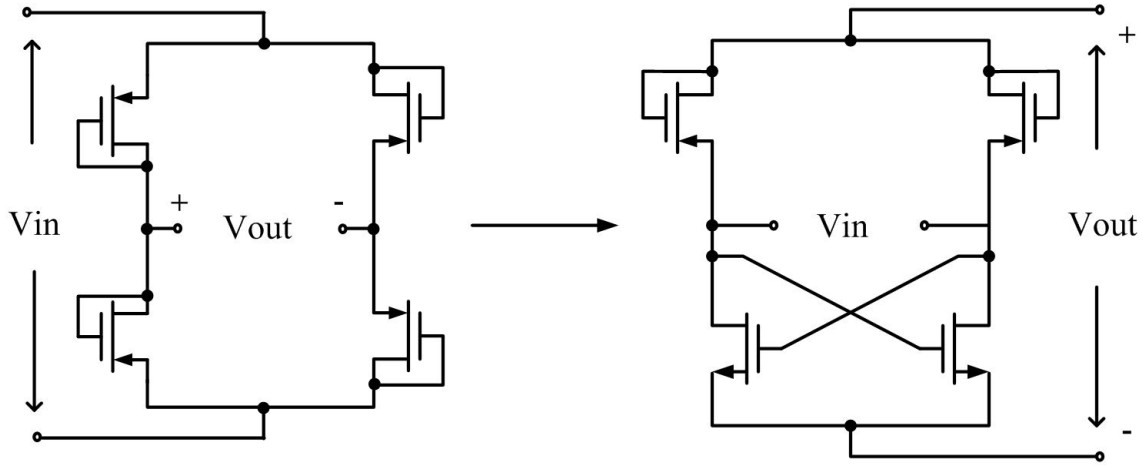


Figure 1.4: CMOS rectifier with cross-couple configuration.

and turn on when the input voltage amplitude is larger than the output voltage. By using the cross-couple structure, voltage drop is reduced because the voltage drop on each cross-coupled transistor is only one V_{dsn}. However, the two switches are still in diode structure connection and voltage loss still exists on each switch, thus the efficiency is not optimized for the voltage drop on the switch diode.

We call all the above rectifiers integrated passive rectifiers. The merit of these passive rectifiers is frequency independent, because the structure is simple and no other circuits are included. However, the voltage and power efficiency are commonly not sufficient because of the voltage drop on diode-connected MOS transistors. Though the cross-couple structure can reduce the voltage drop to only one V_{th} and low threshold voltage technology can be utilized to further reduce it,the passive rectifiers are still not suited for some low voltage applications. Sometimes, passive rectifiers are even the bottleneck of the whole system.

In order to overcome the drawbacks of above passive rectifiers and to further improve the voltage conversion efficiency and power efficiency. A concept of active diode was first proposed in [22] instead of the diode connected transistors in the conventional passive rectifiers. The active diode works as an ideal diode without voltage drop and reverse current. Figure 1.5 shows the conceptual schematic of the active diode [22]. It is composed

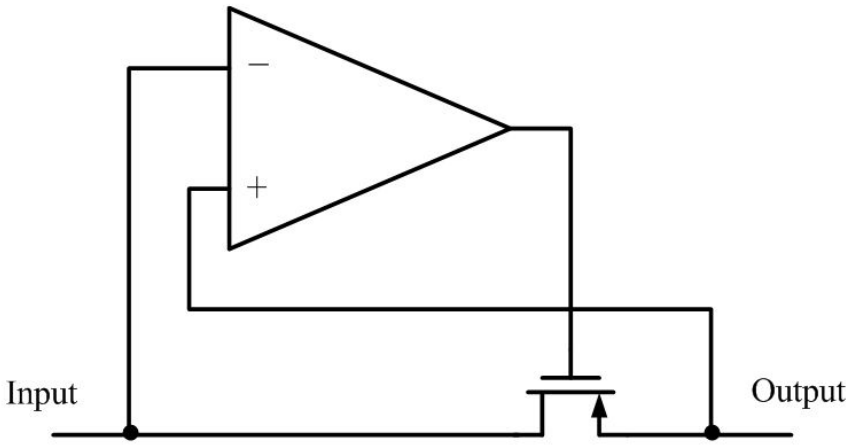


Figure 1.5: Conceptual schematic of active diode [22].

of a comparator and a transistor switch. It should be mentioned that the comparator should be powered by the output signal. When the input source amplitude is larger than the amplitude of output voltage, the comparator will turn on the switch and current flows from input source to the output terminal and charges the load. When voltage amplitude of the output is larger than input source, the comparator should turn off the switch immediately, otherwise reverse current will flow from output terminal to input terminal. The reverse current will decrease the power efficiency and increase the output voltage ripple. Thus, the design of active diode is very important.

After the proposing of active diode, the research of rectifier using active diode is promoted in many applications. Vibration energy harvesting is one of the applications. Rectifier for vibration energy harvesting system was first proposed in [23]. As the output voltage amplitude and output power of vibration generator vary case by case. Commonly, the voltage amplitude is very small. Thus, the rectifier in [24] was designed that it can work even the input source amplitude is 0.5 V. The proposed rectifier is composed of two stages: the negative voltage convertor and the active diode. The bulk-input comparator idea was used in the active diode design. Figure 1.6 shows part of the bulk-input comparator. Commonly, gate-input comparator has usually at least three stacked transistors. This

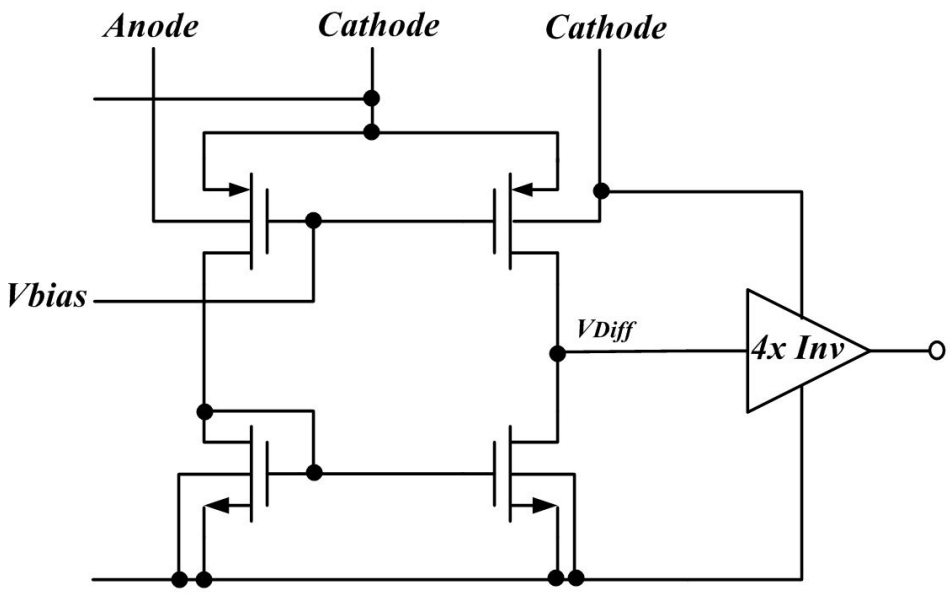


Figure 1.6: Schematic of bulk-input comparator [24].

decides that the rectifier is difficult to work with only 0.5 V input voltage. Therefore, the bulk-input comparator idea was utilized and designed with only two stacked transistors and no tail current source is used in the circuit [24]. By using this idea, the minimum operation voltage of the rectifier is only 500 mV. In order to further reduce the operation voltage, a body bias block was added to bias the PMOS transistor in the negative voltage converter [25]. The concept is shown in Fig. 1.7.

As the input voltage amplitude is equal to $|V_{GS}|$ of the transistors in the negative voltage convertor, the switch transistor can be only turned on if input source amplitude is larger than V_{th}. By adding the body bias block, V_{th} of PMOS transistors is reduced. The minimum operation voltage of the rectifier is only 0.3 V. However, the drawbacks of the two rectifiers are also obvious. It can be concluded by two points:

1. Body reverse current: In the previous published two papers [24], [25], the maximum operation voltage of the rectifier is only 1 V. In [24], the value is as small as 0.7 V. The reason can be found in Fig. 1.6. The comparator uses bodies as the anode and cathode terminals. The input signal is treated as anode. The output voltage is treated not only the cathode but also the supply voltage of the comparator. If the voltage

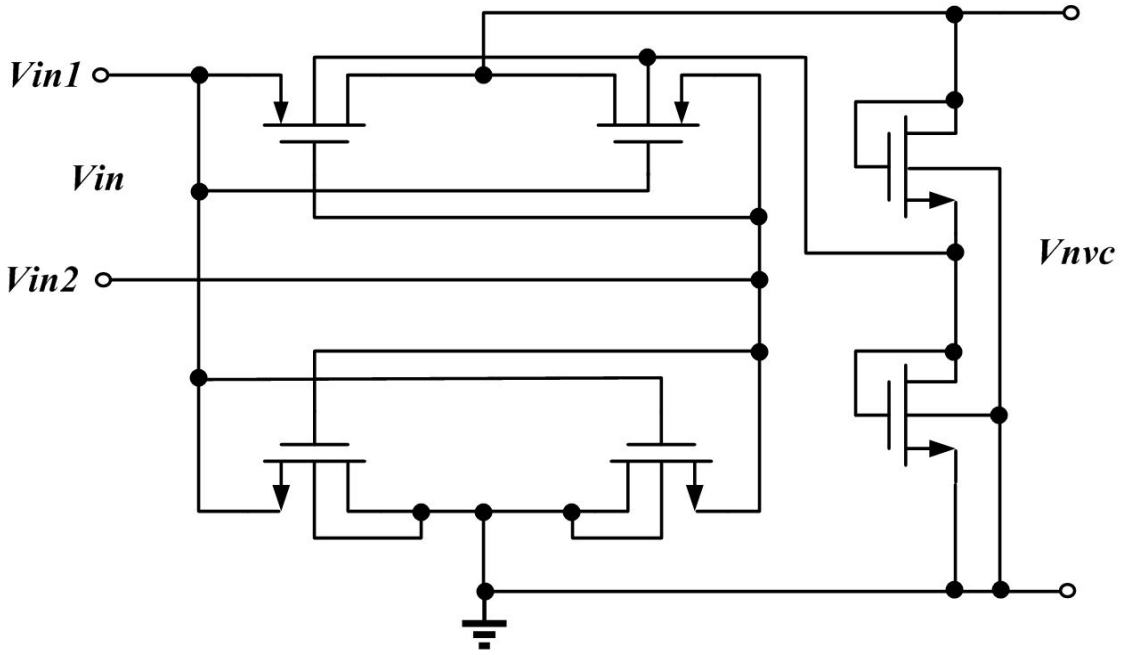


Figure 1.7: Schematic of negative voltage converter with body bias block [25].

conversion efficiency is high enough, the voltage amplitude of cathode terminal is close to the peak voltage of input source. As the input voltage amplitude connected to anode terminal varies from 0 V to peak voltage, the absolutely value of $|V_{bs}|$ will be larger than 0.7 V sometimes if the input voltage peak amplitude is larger than 0.7 V. Thus, the pn junction will be turned on and the reverse current will flow from cathode terminal to anode terminal through the body pn junction. This large reverse current will increase along with the input peak voltage amplitude. Reverse current results in not only the poor power efficiency but also the large output voltage ripple. That is the reason why the maximum operation voltage of the two papers is only 1 V, which is much smaller than the breakdown voltage of 1.8 V if using the standard 0.18 μm CMOS process.

2. Drivability and chip area: Both papers use bulk input comparator to realize the active diode. However, the transconductance g_{mb} of the bulk input comparator is much smaller than the transconductance g_m of gate input transistors. Thus, more buffer

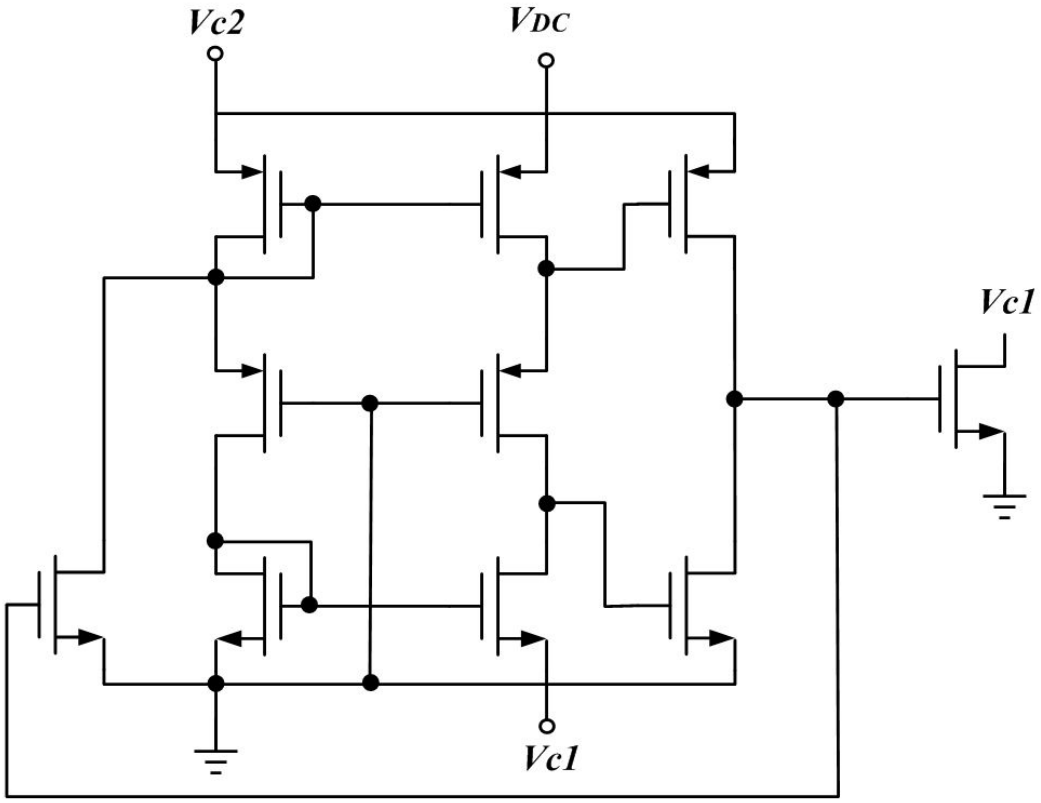


Figure 1.8: Four input comparator with RCC block in [26].

stages are needed to drive large size transistor switch. On the other hand, in order to reduce the minimum operation voltage, both researches use large size transistors to reduce the on-resistance. Another merit of using large size transistors is that the branch current of the comparator can be increased to improve the drivability.

Another application for active diode and active rectifier is wireless power transfer. The concept of active rectifier was firstly proposed in [22]. In [26], the author firstly realizes the concept and proposes a low-loss CMOS active rectifier for powered devices. The idea is based on full wave bridge rectifier and the diode-connected transistors are replaced with two active diode, which is shown in Fig. 1.8. The active diode has four input terminals. The terminal of V_{c2} and V_{DC} work as the supply voltage. The terminal of V_{c1} and V_{GND} compare each other and control the switch M_{N1}. Though a reverse current control transistor is added to block the current from output to input, the performance of this rectifier is not

satisfied. The minimum operation voltage is 1.5 V. The comparator uses three stacked transistors, which increases the supply voltage. Voltage conversion efficiency is 80%@1.5 V and power efficiency is only 60%.

In [27], the author designed an active rectifier with full wave bridge structure. Comparing with the four input comparator, two input comparator was used in the design. Figure 1.9 shows the schematic of the circuit in [27]. Its idea comes from the cross-couple structure. Two of the diode-connected transistors are replaced by active diode. All the four transistors play a role as switches working in the linear region. Voltage drop on each transistor is only one V_{dsp} or V_{dsn}, which can be easily reduced by increasing the transistor size. Switch M_{n2} and M_{n1} are controlled by CMP1 and CMP2 by comparing voltage V_{in1} and V_{in2} with ground potential. Besides the structure improvement, the control circuit in [27] firstly considered the influence of reverse current. In that paper, simulation results of the reverse leakage current in the rectifier are evaluated without any method to solve the problem. The reverse current is caused by the switch turn off delay. Though output voltage is larger than the input voltage. The switch does not turn off immediately. In order to overcome the issue, unbalanced biasing scheme is utilized. Figure 1.10 shows the schematic of the control circuit. The unblanced biasing is realized by setting $I_{s2} < I_{s1}$. Thus, a proper voltage difference between V_{vn-} and V_{in+} is created. This voltage offset can help to compensate the time delay and avoid the reverse current. The delay of $\triangle$V can be properly controlled by adjusting the value of I_{s2} and I_{s1}.

The paper [27] contributed a lot to the development of active rectifier. Since then, many researches are done based on the results of this paper. The minimum operation voltage of this design is 1.2 V. The drivability is also improved a lot. A heavy load of 100Ω is tested with a good performance. The average voltage conversion efficiency can be 84% and power efficiency is about 82%. However, the performance is not good enough. With the development of low power and low voltage design, many systems can work under 1 V or even smaller than 1 V. This trend challenges the design of the active rectifier. On the other hand, though the power efficiency and peak voltage amplitude conversion efficiency has been improved compared with [26], there is still room for the improvement of the

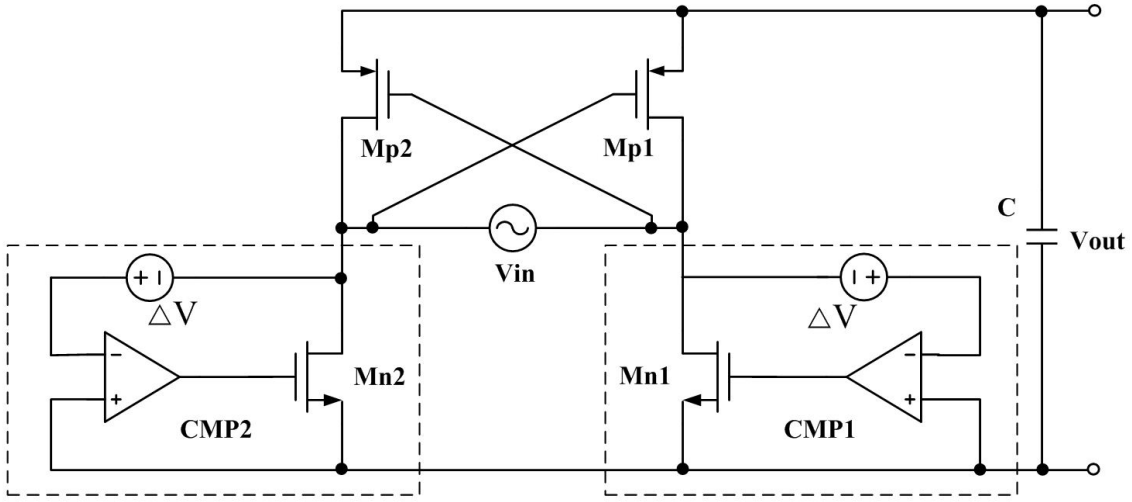


Figure 1.9: Schematic of the proposed rectifier in [27].

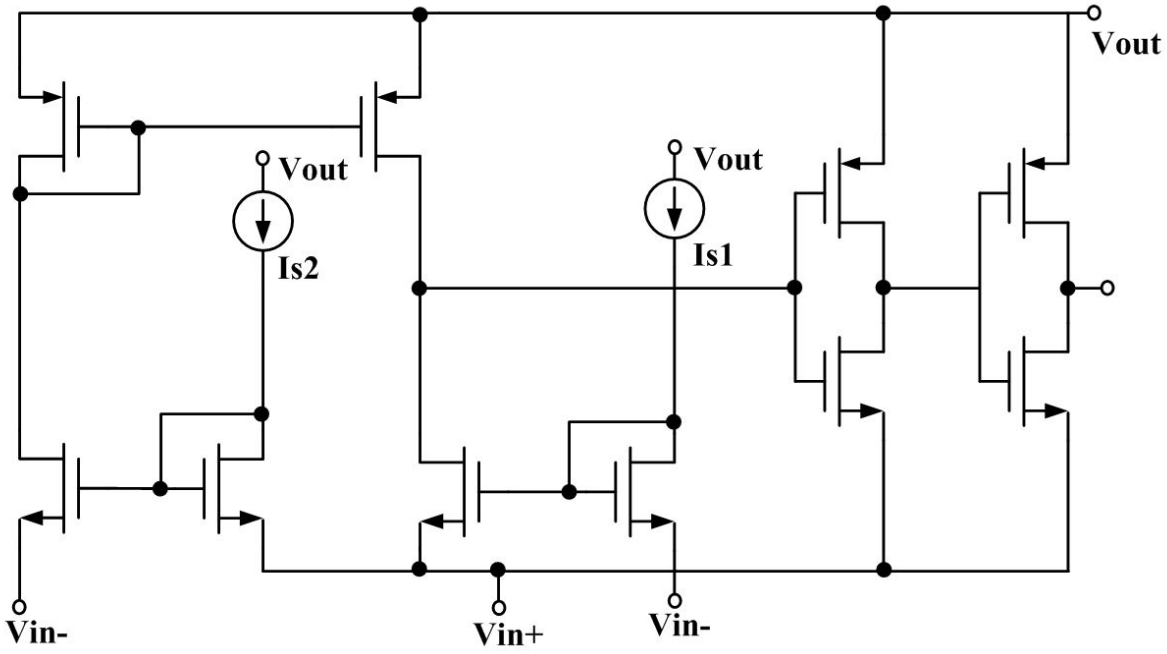


Figure 1.10: Unbalanced comparator in [27].

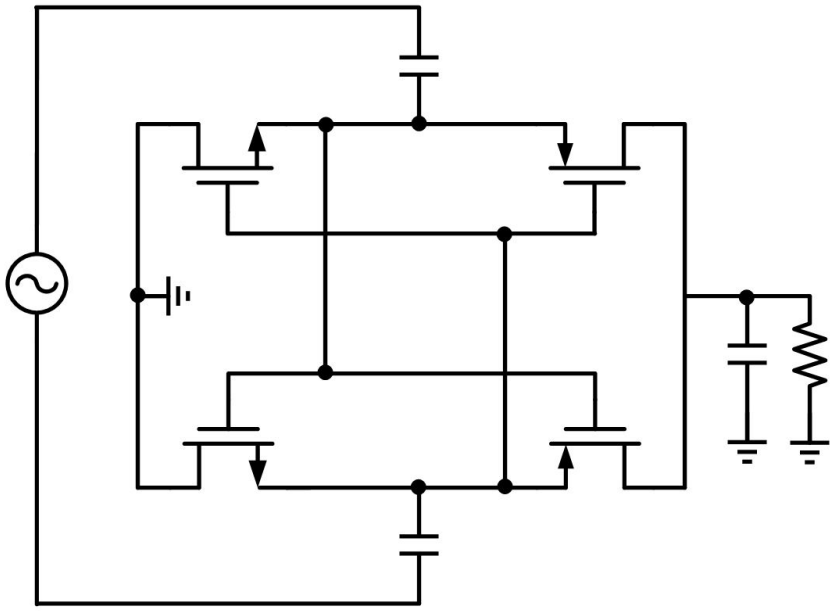


Figure 1.11: Rectifier for UHF application based on negative voltage convertor [28].

conversion efficiency. Besides that, the structure, especially the comparator, used in the design is much complicated. This drawback also limits the power efficiency of the whole circuit.

It should be noted that the rectifier proposed in [27] is a milestone for the development of active rectifier. The working frequency of it is from 100 kHz to 2 MHz. For some higher frequency range, such as 13.56 MHz, the performances of the structure will decrease and are not sufficient to the requirement.

For higher frequency case, both active rectifier and passive rectifier can be found. However, active rectifier is rarely used for the characteristic of frequency dependence. An active rectifier proposed in [61] is suited to the application of 13.56 MHz. The rectifier is designed based on the common gate structure comparator. Two comparators are connected with each other and the gain is improved. However, the operation speed is still not fast enough. Time delay and reverse currents result in a poor voltage conversion efficiency and power efficiency, especially for low input voltage amplitude signal. In [28], the negative voltage convertor used in [29] is studied for UHF applications. The circuit structure is shown in Fig. 1.11. The power efficiency is good with the typical value of input

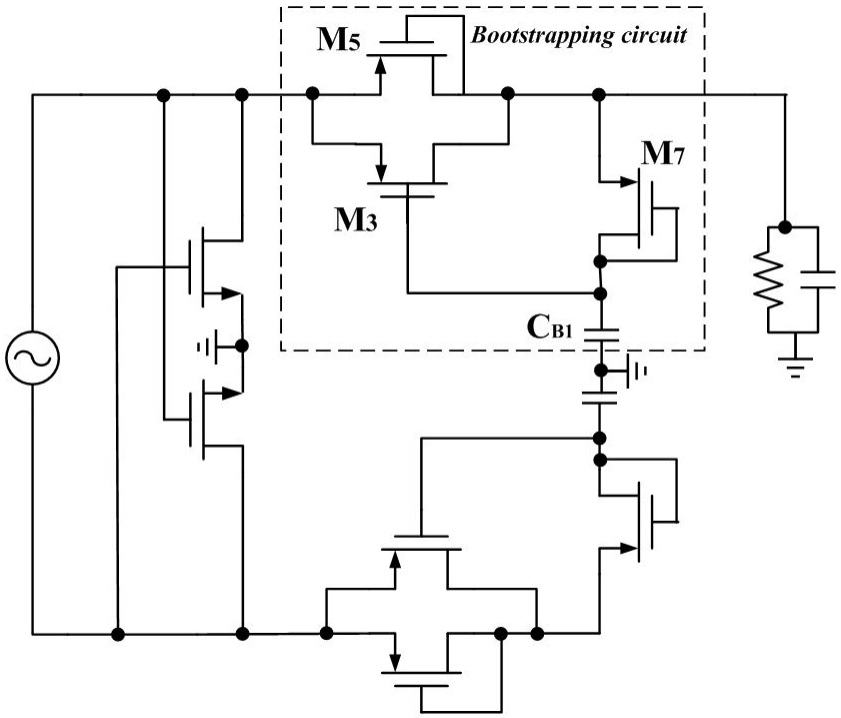


Figure 1.12: V_{th} cancellation rectifier in [30].

power. However, the structure cannot control the reverse current and power efficiency decreases dramatically when input power is larger. This drawback decides that it can be only utilized in some typical applications. Threshold voltage cancellation technologies [30] are commonly used to compensate the passive rectifiers. The idea is to feature a constant bias voltage between gate and drain terminals of the switch diode. Comparing with active diodes, passive rectifier with V_{th} cancellation is less frequency dependent. High voltage conversion efficiency can be achieved by reducing the voltage drop. In [30], the V_{th} cancellation technology by using bootstrapping circuit has been proposed. The schematic of the designed rectifier is given in Fig. 1.12. The proposed circuit is based on the cross-coupled structure. The diode-connected transistors are replaced with bootstrapping circuit. M_5 works as a diode and provides the current through M_7 to charge the bootstrapping capacitor at the start up state. The power stored in capacitor CB1 will be applied to the gate of M_3, which works as a switch. When the V_{in} is larger than V_{out} by one threshold voltage, M_5 will be turned on and the current flows through M_5 and M_7 to charge CB1. For the same

process, we can assume V_{th5}=V_{th7} without considering the body effect. V_{th3} and V_{th7} cancel out each other. Thus, the effective V_{th} can be reduced and lower voltage drop will result in a higher output voltage, which means a higher voltage efficiency.

Circuit structure is simple and no complicated design techniques are needed for this design. Besides that, the merit of frequency independent and its compatibility with standard process are also attracting. The measurement results show that voltage conversion efficiency can be 70% with a 1 V and 10 MHz input source. However, the drawbacks of this structure are also obvious.

1. Though the capacitors used in the circuit can be realized in standard CMOS process, chip area will increase due to the utilization of capacitors. On the other hand, the switch transistor size should be adjusted to optimize the performance of the circuit when the source frequencies are different.

2. Though the minimum operation voltage can be as small as 0.8 V, the voltage conversion efficiency and power efficiency are not high enough, especially the power efficiency, which is only 30% when the input source amplitude is 0.8 V. It is easy to be understood. These circuits are mainly investigated for improving the voltage conversion efficiency and no design strategy has been discussed in terms of reverse current which is considered in [27]. Thus, the reverse current is commonly very large in these rectifiers which results in poor power efficiency, especially for low input voltage amplitude. The total efficiency of the wireless power transfer system is also restrained by this poor performance.

1.2 Motivation and research objective of this dissertation

Based on the above considerations and motivations, the research objectives are proposed. All these aims focus on the drawbacks of previous researches and consider the requirements of vibration energy harvesting and wireless power transfer systems. The objectives are listed as below.

1. The dissertation will design a wide input range rectifier for vibration energy harvesting systems. It can be suited to variable output voltage amplitude of different vibration energy generators. Comparing with previous works, the minimum operation voltage of this work should be smaller than 0.5 V. The voltage conversion efficiency and power efficiency should be larger than 90%. In order to reduce the power consumption and chip area, the author will avoid using large size transistors in the design. The design input source frequency ranges from 10 Hz to 1 kHz, which can meet the requirement for most vibration energy harvesting systems.

2. The rectifier designed for wireless power transfer will be divided into two parts. One is for the input source frequency ranges from 10 kHz to 1.5 MHz. This part focuses on the reducing of minimum operation voltage without influence to the voltage conversion efficiency and power efficiency. The other one is for the frequency of 13.56 MHz applications. Most of structures in the previous design used passive rectifier for the frequency independent characteristic. However the biggest problem is the reverse current in the passive structure. This dissertation will design an active rectifier for 13.56 MHz. This active structure can restrain the reverse current and improve the power efficiency up to 90%.

1.3 Contribution of this dissertation and its organization

As described in section 1.1, rectifier plays a very important role in the field of vibration energy harvesting and wireless power transfer systems. This dissertation includes three proposed novel rectifiers, which solve different issues in above applications. For vibration energy harvesting system, previous published rectifiers can only work in low voltage range. The power efficiency will decrease dramatically when input voltage is larger than 1 V, because the body diode is turned on. In this dissertation, the proposed rectifier for this application solves this issue and enlarges the input voltage amplitude range, which is from 0.45 V to 1.8 V. This makes the rectifier suitable for different kinds of vibration generator

and widens the application field. For wireless power transfer system, the proposed two novel rectifiers dramatically reduce the minimum operation voltage and further improve the voltage conversion efficiency and power efficiency. The working frequency ranges from 100 kHz to 1.5 MHz and 13.56 MHz, which satisfies most of applications.

The organization of this dissertation is shown as below.

In Chapter 1, the application backgrounds and different topologies of previous researches are briefly introduced. And then, the motivations and objectives of this dissertation are described based on the drawbacks of previous designs, followed by the organization of the dissertation in last section.

In Chapter 2, a low voltage CMOS full-wave rectifier is proposed. This structure is designed for transcutaneous power transmission in low power battery-less devices such as biomedical implants. By using a simple comparator-controlled switch which needs a small supply voltage, the lowest input voltage amplitude can be reduced to 0.7 V with a standard CMOS 0.18 μm process, which is much smaller than 1.2 V in previous researches. Comparing with traditional diode bridge structure, the proposed rectifier uses only one comparator and a negative voltage converter. This proposed design dramatically reduces the power loss and the production cost. In combination with current offset bias circuit which blocks the reverse current from output to input terminals, the proposed rectifier can achieve a maximum peak voltage conversion efficiency of more than 94% and a power efficiency of approximately 90.5% with an input source frequency from 100 kHz to 1.5 MHz, which are improved comparing with the voltage conversion efficiency of 86% and power efficiency of 87% in previous published papers. Besides that, the minimum operation voltage is dramatically reduced to 0.7 V, comparing with the previous best result of 1.2 V.

In Chapter 3, a low voltage and highly efficient CMOS rectifier for low power energy harvesting system is proposed. The working frequency is from 10 Hz to 1 kHz. Comparing with previous design with bulk-driven comparator, the proposed rectifier utilizes full bridge structure and source-driven comparator is used in the novel active diode. Body diode is always reverse biased even the input voltage is higher than 1 V, which making the rectifier work at a wide range of input voltage amplitudes of 0.45 V up to 1.8 V under a standard

0.18μm CMOS process. The comparator that consists of common-gate stage and control stage is biased to weak inversion region to control the switch of the active diode. This technology reduced the minimum operation voltage to as low as 0.45 V. The proposed rectifier can achieve a power efficiency over 90% and a voltage conversion efficiency of over 96%. Simulated power consumption of the rectifier is 264.35 nW at 500 mV, which is about 30% smaller than the best recently published results. The size of the power transistors used in the rectifier are only one third of previous design. Smaller transistors result in better efficiency and help to save the chip area.

In Chapter 4, a 1 V, high efficiency comparator-based CMOS rectifier for wireless power transfer, such as biomedical application is presented. A novel active diode controlled by a cross coupled comparator is designed to overcome common-mode voltage limit of traditional structure and improve the conversion efficiency. Reverse current is also reduced by utilizing a switch off response compensation technique considering the charge delay caused by large gate-capacitor of the switch transistors and high frequency. The switch off response compensation technique can not only reduce the reverse current but also maximize the conduction time of the active diode by using a SR latch circuit. The proposed rectifier is verified using a standard 0.18 μm CMOS process with an input source frequency of 13.56 MHz. Results show that the rectifier can achieve a maximum voltage conversion efficiency of 96% and power efficiency about 90%. Power consumption of the rectifier is only 0.259 mW with a 1 V peak input voltage. Though the minimum operation voltage in previous paper can be as low as 0.8 V by using Vth cancellation technology, the voltage efficiency is only 37.5% even with a light load.

In Chapter 5, the conclusions of this dissertation are given.

Chapter 2

Low voltage CMOS rectifier for low power battery-less devices

2.1 Introduction

With the rapid development of microelectronics, high performance low power battery-less devices such as biomedical implant devices [31], [32], [33], [34] play a more and more important role in modern medical treatments [35] such as measurement of internal blood pressure and monitoring of organs. These devices must be small in size to ease the implantation and be free of feedthrough wires to reduce the infection risk while increasing

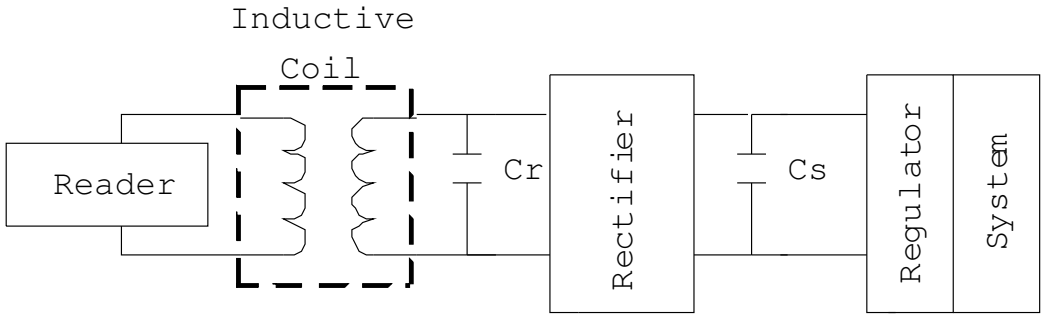


Figure 2.1: Schematic of a power transmission system of biomedical implants.

the portability such as a $4mm \times 5mm$ system [31]. Batteries are not optional choice for implantable devices, because their lifetime is limited, and they are usually large and leaks can pose a hazard to tissues. In recent years, inductive coupling links is commonly used to deliver power and information to these implantable devices [36], [37]. Figure 2.1 shows the block diagram of power transmission of biomedical implants. The inductive coil captures the signal from the reader whose carrier frequencies range from 200 kHz to 1.5 MHz. The working frequency range is a critical issue. High working frequency will result a health danger issue to living things [27] and lower frequency range will reducing the transmission efficiency. The couple energy is then passed to the receiver circuit to generate a high AC voltage, followed by a rectifier to convert it into a DC voltage. Then the regulator such as DC-DC convertor will regulate the output voltage and power the load system. In order to reduce power loss and enhance the efficiency, the power transmission used has to have sufficient power and data rate to be transmitted to the implant. The power transfer efficiency η_s is given as

$$\eta_s = \eta_{link} \times \eta_{rec} \times \eta_{reg}, \tag{2.1}$$

where η_{link}, η_{rec}, η_{reg} are efficiencies of coupling coil, rectifier and regulator, respectively. Thus, the whole system efficiency η_s is also influenced by the rectifier's efficiency η_{rec}. Higher η_s can be achieved with a higher η_{rect}.

Conventional rectifiers are consisted of diodes and capacitor. They are divided into two types: half wave rectifier and full wave rectifier. Conventional diode rectifiers are suitable for high voltage and high power applications. Schottky diodes with a low forward voltage drop can replace the common diode to improve the efficiency. However, the high production cost is a big problem. Transistors with a low threshold voltage can be used to reduce the operation voltage. However, the additional masks and fabrication steps increase the extra cost. In [21], the author used a cross coupled PMOS structure to replace two semiconductor diodes of the diode-bridge structure. However, the voltage drop still exist and voltage efficiency is not optimized.

Recently, in order to optimize the output voltage and voltage conversion efficiency, an active diode [22] is used instead of the diode configured transistors in the conventional rectifier. In [26] and [27], they use two active diodes instead of the diode configured NMOS transistor in [22]. With active diodes instead of passive diodes, high output voltage and high efficiency can be achieved. Aiming at saving the chip area and making the circuit simpler, a rectifier with a negative voltage converter and just one active diode was proposed in [29]. However, there is a major bottleneck in the previous rectifiers. Firstly, for very low AC input voltage systems such as 0.7 V, its rectification will not be feasible by using previous reported works. Secondly, even if rectification is feasible, the forward voltage drops and the reverse currents will cause a large amount of losses and make the power conversion very inefficient.

In this chapter, a low voltage CMOS rectifier is proposed. In order to make the rectifier work with a small input voltage, a simple and low voltage active diode is developed to allow the rectifier to work with just 0.7 V input which is far less than 1.2 V [27]. Wide frequency range of operation makes the rectifier not only suited to biomedical implants but also vibration energy harvest systems [38].

This chapter is organized as follows. In Section 2.2, the principle of a conventional negative voltage converter will be given. In Section 2.3, the principle of the operation of proposed low voltage rectifier is presented, including the low supply voltage active diode, the reverse current consideration and current offset. Simulation results are given in Section 2.4, followed by the summary in Section 2.5.

2.2 The principle of a negative voltage converter

Recently the negative voltage converter published in [29] is utilized to change the negative half period of the input source wave into positive one, which is realized with two PMOS and two NMOS transistors shown in Fig. 2.2. When the input source is in the positive half period ($V_{in1} > V_{in2}$), MP1 and MN1 will be conductive when the input voltage increases and gets larger than $\mid V_{thp} \mid$ and V_{thn}. Thus, terminal 1 will be connected to the high potential

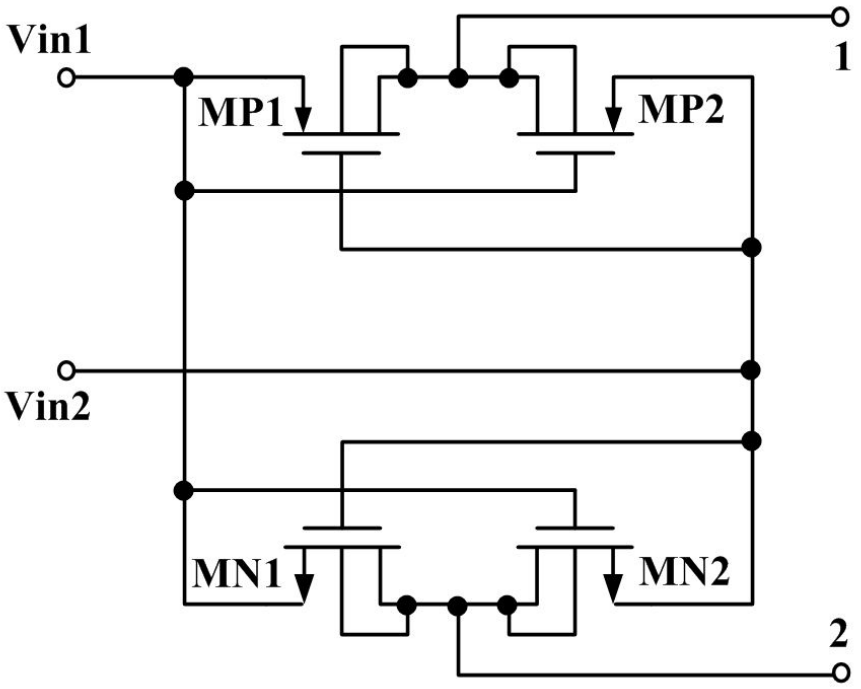


Figure 2.2: Circuit diagram of the negative voltage converter [29].

and terminal 2 to the low potential. When the input wave is in the opposite half, MP2 and MN2 are conductive to connect terminal 1 to V_{in2} and terminal 2 to V_{in1}. Therefore terminal 1 is always the high potential and terminal 2 the low potential. Consequently, the bulk of the PMOS transistor can be directly connected to terminal 1 and the NMOS to terminal 2.

In this case, during each conductive branch, the voltage drop is only $| V_{dsp} | + V_{dsn}$, where $| V_{dsp} |$ and V_{dsn} are the dropout voltages of PMOS transistors MP1/MP2 and NMOS transistors MN1/MN2, respectively. In order to get a small voltage drop, the size of these switch transistors should be as large as possible to decrease the on-resistance, then the $| V_{dsp} |$ and $| V_{dsn} |$ can be minimized. The simulation results show that the voltage drop in this stage can be less than 10 mV. Though the converter has nearly no voltage drop, it cannot control the current direction, therefore an active diode is necessary to block the reverse current.

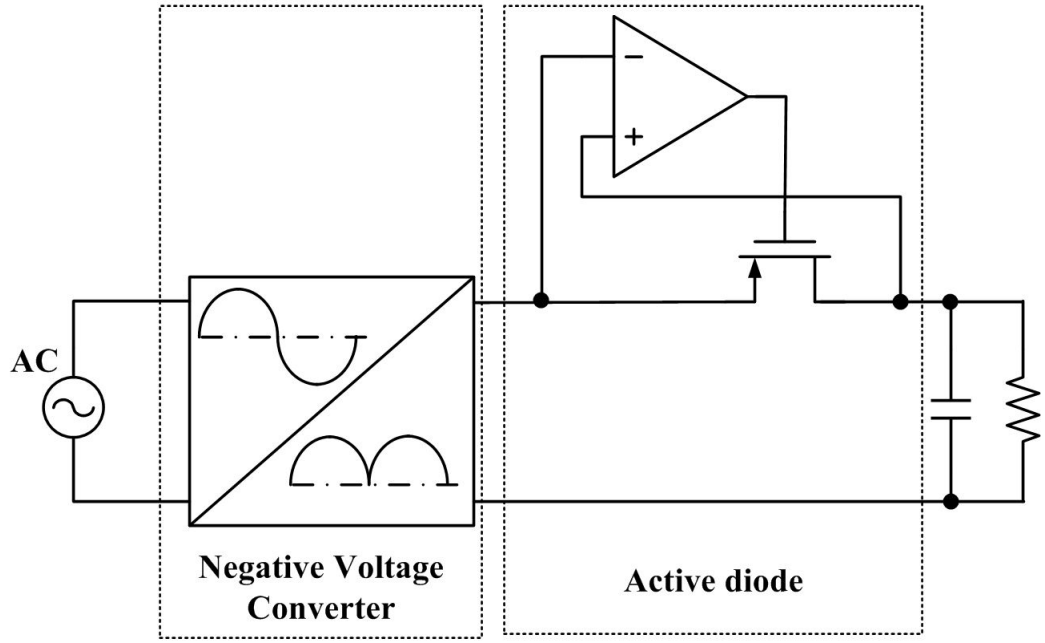


Figure 2.3: Simplified schematic of the proposed rectifier.

2.3 Proposed low voltage rectifier

The main aims of our proposed rectifier are to achieve a lower input voltage amplitude and a much higher voltage and power efficiency. Figure 2.3 shows the simplified structure of our proposed rectifier. This rectifier can be divided into two stages: the negative voltage converter [29] and the simple low voltage active diode. The negative voltage converter has been described in Section 2.2.

2.3.1 Low operation voltage active diode

The main merit of this stage is to control the current direction and to work as a switch with only | V_{dsp} | voltage drop and a low supply voltage as well. The proposed circuit includes a novel comparator controlled switch, making the structure simple and the minimum input voltage smaller. Figure 2.4 II shows the circuit implementation of the proposed simple low voltage active diode. The output voltage V_{con} of the converter serves as an input of the active diode. Transistors M4 - M9 work as a comparator to control the gate voltage of

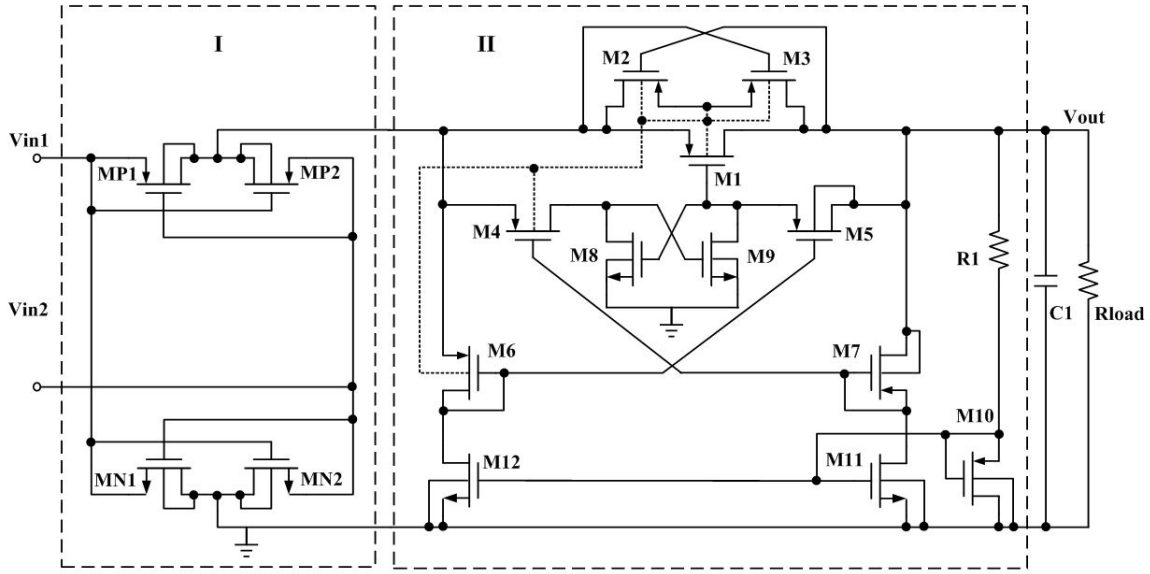


Figure 2.4: Circuit diagram of the proposed rectifier with (I) negative voltage converter, (II) low voltage active diode.

transistor M1. Transistors M10, M11, and M12 are two current mirrors to supply a small and stable current. In order to reduce the voltage drop, M1 is expected to turn on and turn off completely to prevent the reverse current. Set R1 a large resistance (in our design, R1=40 KΩ is used), and then the currents through M10, M11, and M12 are very small. A small I_D (the source to drain current) means $V_{GS} \simeq V_{th}$, where V_{GS} is gate to source voltage and V_{th} is the threshold voltage. The gate voltage of M7 and M4 is around $V_{out} - \mid V_{th7} \mid$, where $\mid V_{th7} \mid$ is the threshold voltage of M7 and V_{out} is the output voltage of the rectifier. Thus, M4 turns on if $V_{con} > V_{out} - \mid V_{th7} \mid + \mid V_{th4} \mid$. Assuming that $\mid V_{th7} \mid = \mid V_{th4} \mid = \mid V_{thp} \mid$, when $V_{con} > V_{out}$, M4 turns on. Meanwhile, M5 turns off and the gate voltage of M9 is pulled high to connect the gate of M1 to the ground. Then M1 turns on to charge the capacitor C1. Similarly, M5 turns on if $V_{out} > V_{con} - \mid V_{th6} \mid + \mid V_{th5} \mid$, and the gate of M1 is connected to V_{out} which is high potential. Thus, M1 turns off to prevent the reverse current from C1 to the input.

A dynamic bulk regulator is added to M1, connecting the substrate of M1, M4, M6 to the highest potential which prevents the parasitic vertical PNP transistors and avoids the chance for latch-up. Furthermore, the body effect on M1 is reduced and meanwhile reduces the rectifier's dropout voltage and power dissipation.

2.3.2 Reverse current consideration and current offset

There will be reverse current from V_{out} to V_{con} if the switch M1 is still on when $V_{out} > V_{con}$. The reverse current has a big influence to the efficiency of the rectifier, and can reduce the power efficiency and voltage conversion efficiency severely.

As shown in Fig. 2.5, when V_{con} decreases and gets smaller than V_{out}, the gate voltage of M1 does not change to high potential until a delay time $\triangle T$. It means M1 is still on in the time interval $\triangle T$ and there will be reverse curent, for $V_{out} > V_{con}$. In order to avoid the time delay $\triangle T$, we set the transistor sizes $W/L_{M12} > W/L_{M11}$, thus the current through the branch of M12 will be larger than that of M11 because of the current mirror. As in the saturation region, a larger I_D makes the overdrive voltage of M6 larger than M7, which

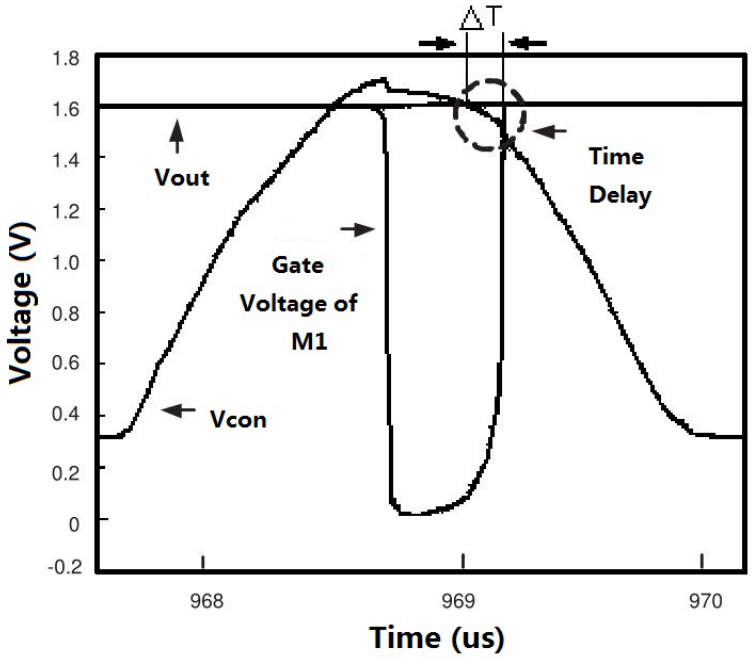


Figure 2.5: Output waveforms of the proposed rectifier with balanced transistor size under $W/L_{M12} = W/L_{M11}$.

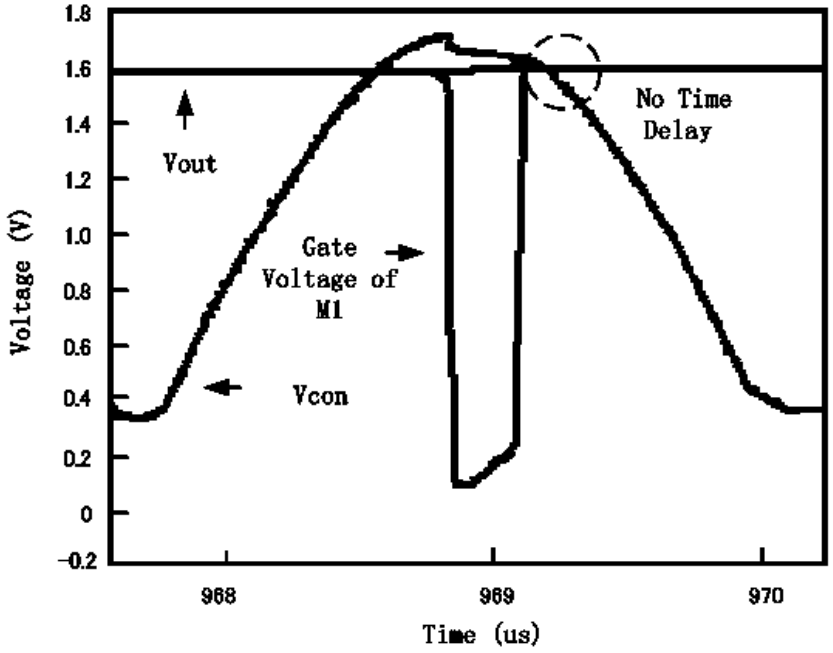


Figure 2.6: Simulated waveforms using current offset when $|V_{in}|_{peak} = 1.7V$.

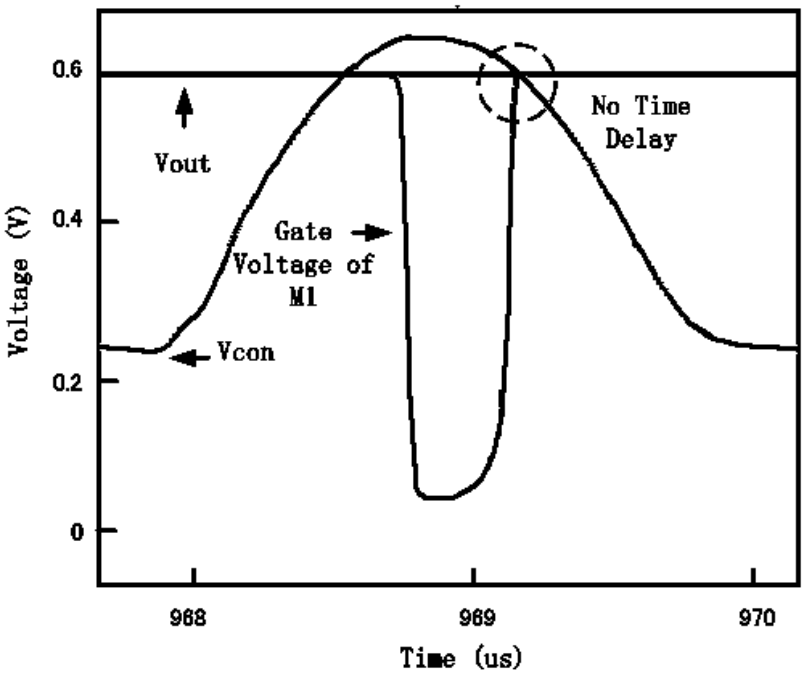


Figure 2.7: Simulated waveforms using current offset when $\mid V_{in} \mid_{peak} = 0.7V$.

makes an offset voltage V_{offset} in the comparator. Thus, the transistor switch turns off when $V_{out} \geq V_{con} + V_{offset}$, where the V_{offset} is negative. This will compensate the $\triangle T$ and eliminate reverse current. When V_{out} changes from 0.7 V to 1.8 V, the current through M11 and M12 will also increase which results in the value increasing of $\mid V_{offset} \mid$. Thus, we should adjust the ratio of $W/L_{M12}/W/L_{M11}$ to promise that there is no time delay with a 0.7V input.

Figures 2.6 and 2.7 show the performances under different input amplitudes. Additionally, taking into account the fabrication tolerances, we set the size of W/L_{M12} a little larger than the required value to compensate this influence. Comparing Figs. 2.6 and 2.7 with Fig. 2.5, the rectifier has even no time to delay. Then, there will be no reverse current in the whole cycle, which helps to reduce to output voltage ripple and maintain the high power efficiency.

Besides the reverse current, the operation voltage of the rectifier is also very important. The minimum operation voltage of the comparator decides the minimum supply voltage

Table 2.1: Circuit transistor sizes.

	Unite Size	Multiply Factor		Unite Size	Multiply Factor
MP1	100μm/0.2μm	100	M5	40μm/0.5μm	50
MP2	100μm/0.2μm	100	M6	40μm/0.5μm	50
MN1	100μm/0.2μm	100	M7	40μm/0.5μm	50
MN2	100μm/0.2μm	100	M8	5μm/0.5μm	1
M1	100μm/0.2μm	50	M9	5μm/0.5μm	1
M2	100μm/0.2μm	50	M10	100μm/1μm	10
M3	100μm/0.2μm	50	M11	100μm/1μm	20
M4	40μm/0.5μm	50	M12	100μm/1μm	40

(input voltage peak amplitude) of our proposed rectifier, since the comparator is supplied by the output dc voltage. In order to promise the operation of comparator, the output voltage of the proposed rectifier must be larger than the minimum operation voltage of the comparator Thus, a small operation voltage comparator is necessary in this design.

As shown in Fig. 2.4 II, in each branch of the source-input stage, there is a pair of NMOS and PMOS transistors from V_{out} or V_{con} to the ground. Consequently, the minimum operation voltage of the comparator is decided by the supply voltage of each branch and can be expressed as

$$V_{out_{min}} = max(\mid V_{thp} \mid + V_{dsn} + V_{ov}, V_{thn} + \mid V_{dsp} \mid), \tag{2.2}$$

where the V_{ov} is the over-dropout voltage of PMOS transistor. It means that the comparator can work well when both the voltages of V_{con} and V_{out} are larger than $V_{out_{min}}$, where $\mid V_{thp} \mid$ is threshold voltage of PMOS and the dropout voltage of NMOS transistor is assumed to V_{dsn}. Since there is also $\mid V_{dsp} \mid + V_{dsn}$ voltage drop through the first stage, the minimum input voltage of the rectifier can be expressed as

$$V_{in_{min}} = V_{out_{min}} + \mid V_{dsp} \mid + V_{dsn}, \tag{2.3}$$

where $\mid V_{dsp} \mid$ is dropout voltage of PMOS transistor.

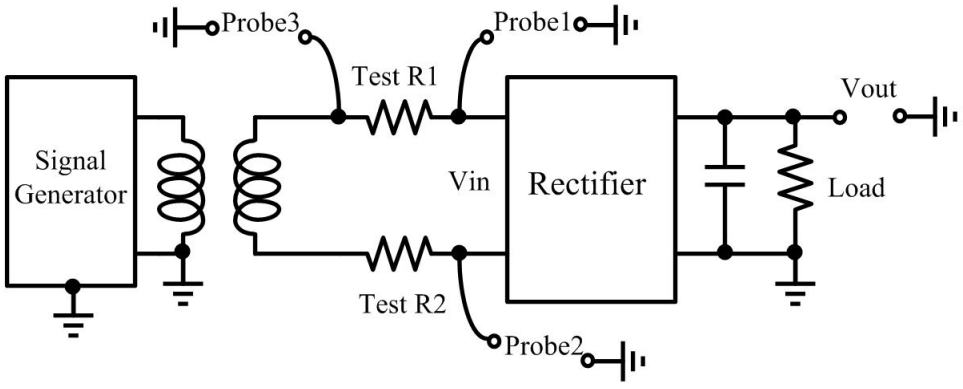


Figure 2.8: Test circuit for chip measurement.

2.4 Simulation and measurement results

The main aspects of the rectifier are minimum input voltage $V_{in_{min}}$, output voltage efficiency, and the power efficiency, which will be discussed respectively.

The circuit has been simulated and fabricated with a standard 0.18 μm CMOS process. The circuit transistors size is shown in Table 2.1. A pure sinusoidal waveform whose frequency changes from 100 kHz to 1.5 MHz is applied to the input of the rectifier in the simulation. Additionally, a capacitance of 1μF and a load of 500 Ω are used. In the chip measurement, the transformer is used as the interface between input source and our proposed rectifier. Besides, the performance of the proposed rectifier under low frequency from 20 Hz to 100 Hz which is suited for vibration energy harvesting systems [13] is also simulated. The test circuit is shown in Fig. 2.8. As the input voltage of the rectifier is floating, inductive coupled coils are used to transfer the signal generated by the generator to rectifier. Probe1 and Probe2 can detect the input voltage amplitude. Probe1 and Probe3 are used to detect the voltage amplitude across the test resistor and calculate the input current. The ration of the coils is 1:1 with 16 turns. Inductance of the coil at 1.5 MHz is 812 μH. Figure 2.9 shows the micrograph of our proposed rectifier, the total chip area is 0.064mm^2 without the pads area.

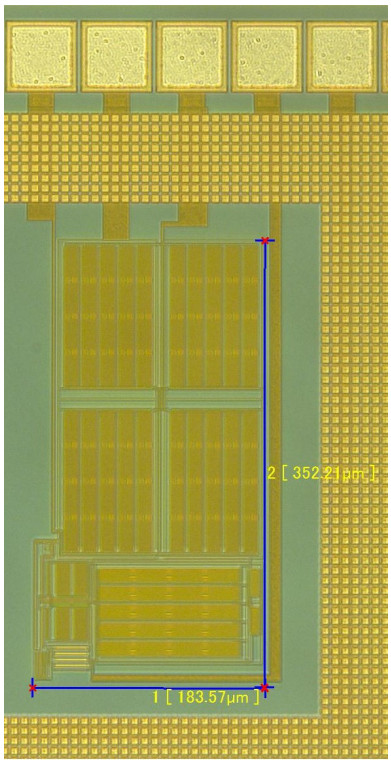


Figure 2.9: Micrograph of the proposed rectifier.

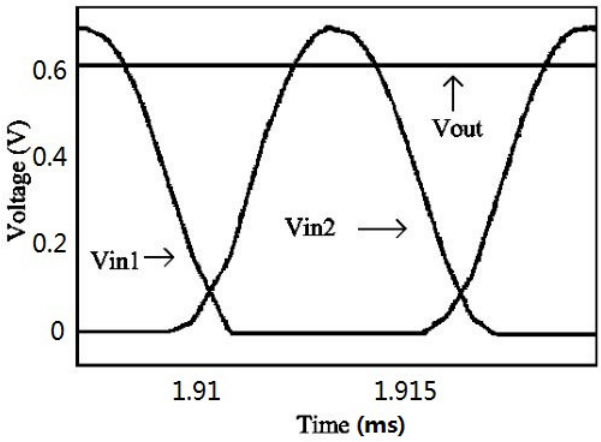


Figure 2.10: Simulated output voltage under 100 kHz, 0.7 V input with RL=500Ω.

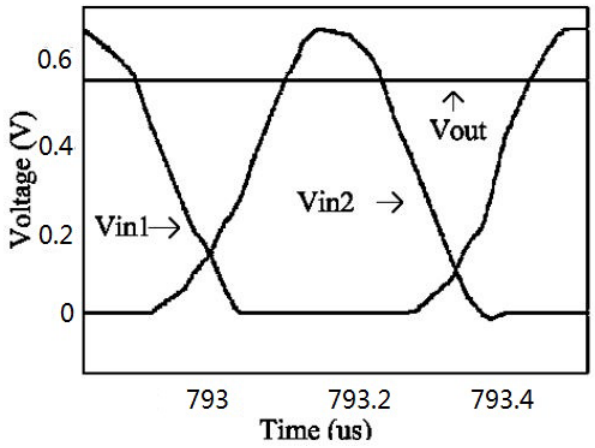


Figure 2.11: Simulated output voltage under 1.5 MHz, 0.7 V input with RL=500Ω.

2.4.1 Minimum input voltage and voltage conversion efficiency

The minimum input voltage is very important especially for some low supply voltage systems. Figures 2.10 and 2.11 show the simulated output voltages. It indicates that the proposed rectifier can work at a minimum input voltage | V_{in} | of 0.7 V from 100 kHz to 1.5 MHz and provides a peak voltage conversion efficiency V_{out}/ | V_{in} | larger than 84%. The chip measurement results given in Fig. 2.12 and Fig. 2.13 also proved the proposed rectifier can work with a 0.7 V input peak amplitude. Figure 2.14 shows the peak voltage conversion efficiency versus different input amplitudes under a 1.5 MHz input. The performance in 100 kHz is shown in Fig. 2.15. Under both two frequencies, the peak voltage conversion rate is above 91% in average when | V_{in} | is from 0.7 V to 1.8 V. The chip measurement results of voltage conversion efficiency are given in Fig. 2.16 and Fig. 2.17. Figure 2.16 shows the voltage efficiency versus different loads, the performance of the unload condition is better than the performance with a load of 500 Ω, which is easy to be understood. The principle is the same as a voltage divider. Large load gets large output voltage. Figure 2.17 shows the voltage efficiency versus different input source frequency of 100 kHz and 1.5 MHz. The performance of 1.5 MHz is poor than 100 kHz due to faster switching of MOS transistors.

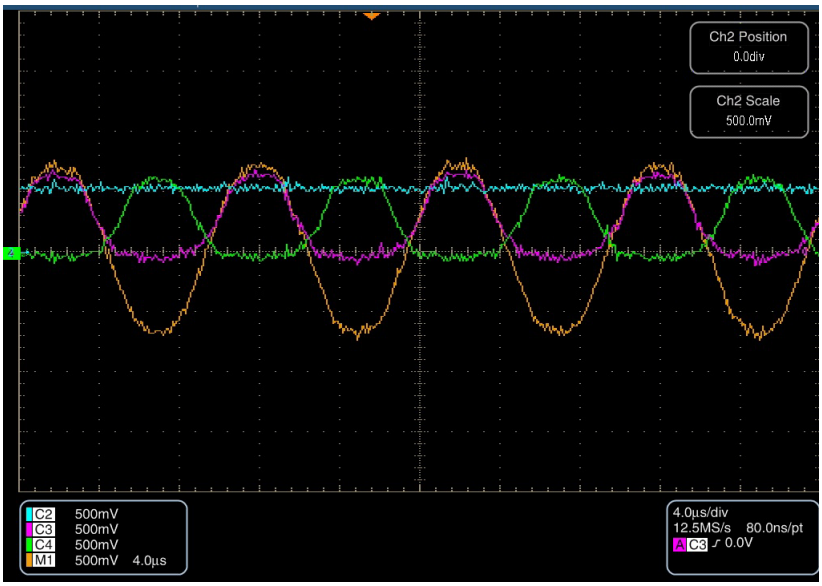


Figure 2.12: Measured output voltage under 100 kHz, 0.7 V input with RL=500Ω.

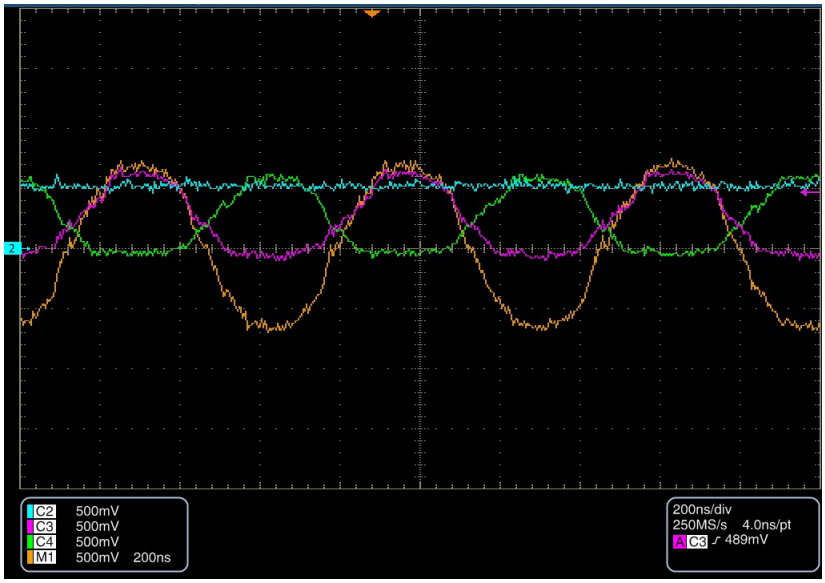


Figure 2.13: Measured output voltage under 1.5 MHz, 0.7 V input with RL=500Ω.

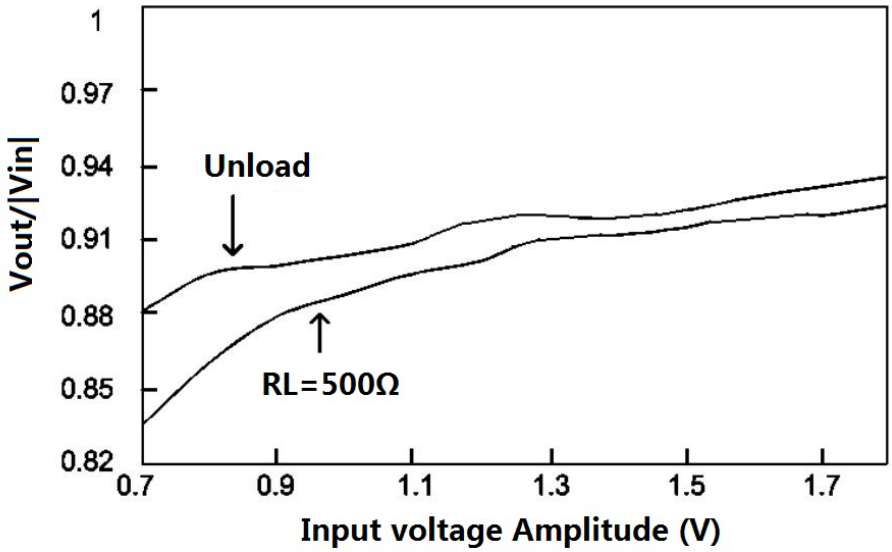


Figure 2.14: Simulated voltage conversion efficiency versus different input amplitudes with a 1.5 MHz input frequency.

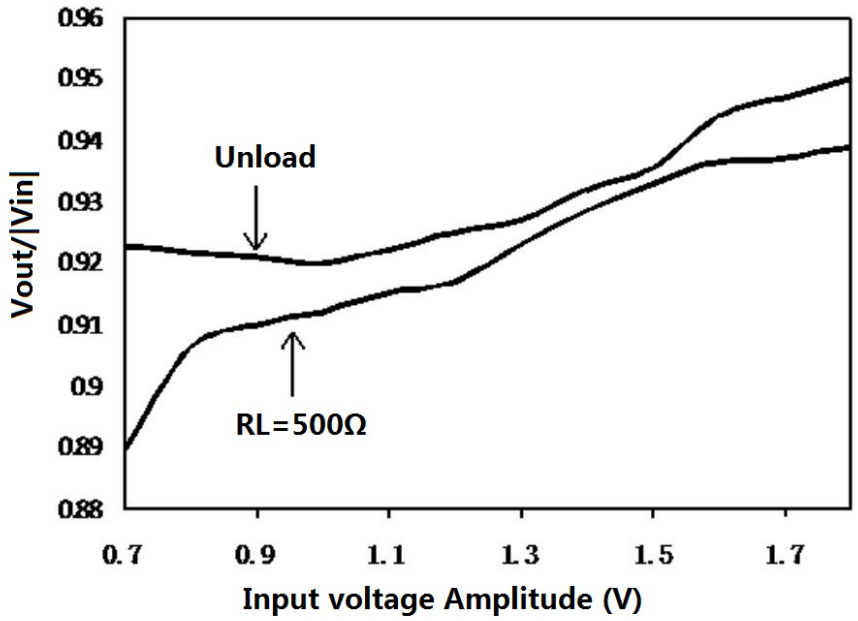


Figure 2.15: Simulated voltage conversion efficiency versus different input amplitudes with a 100 kHz input frequency.

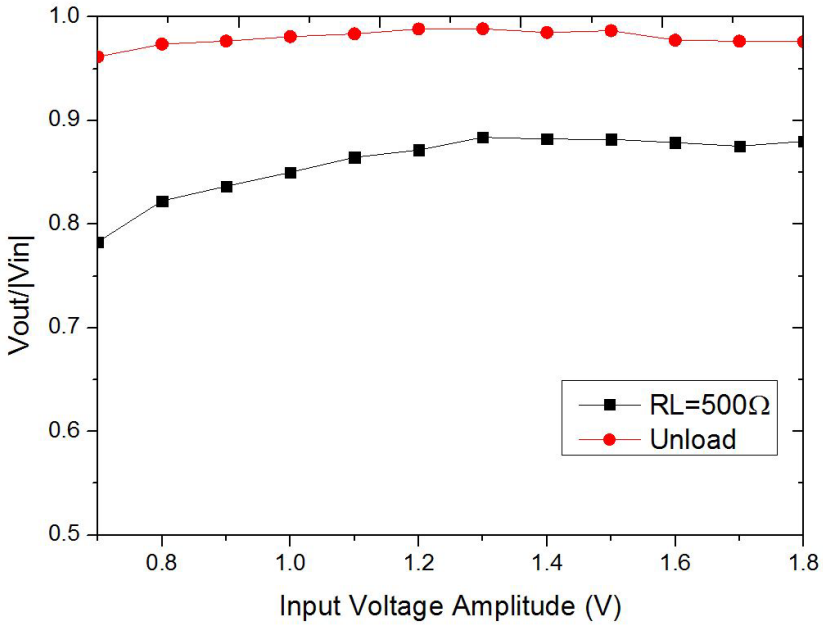


Figure 2.16: Measured peak voltage conversion efficiency versus different input amplitudes with a 100 kHz input frequency.

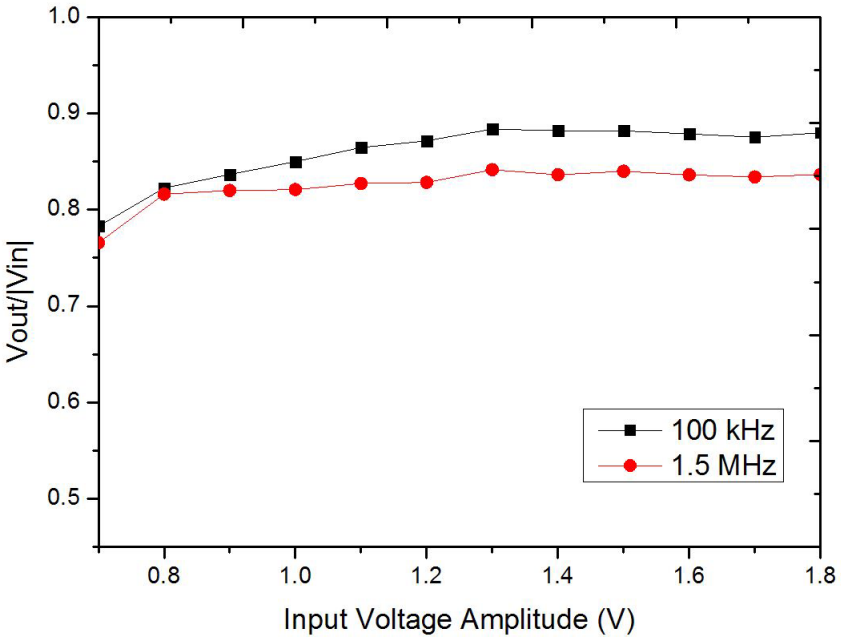


Figure 2.17: Measured peak voltage conversion efficiency versus different input amplitudes with a 500 Ω load.

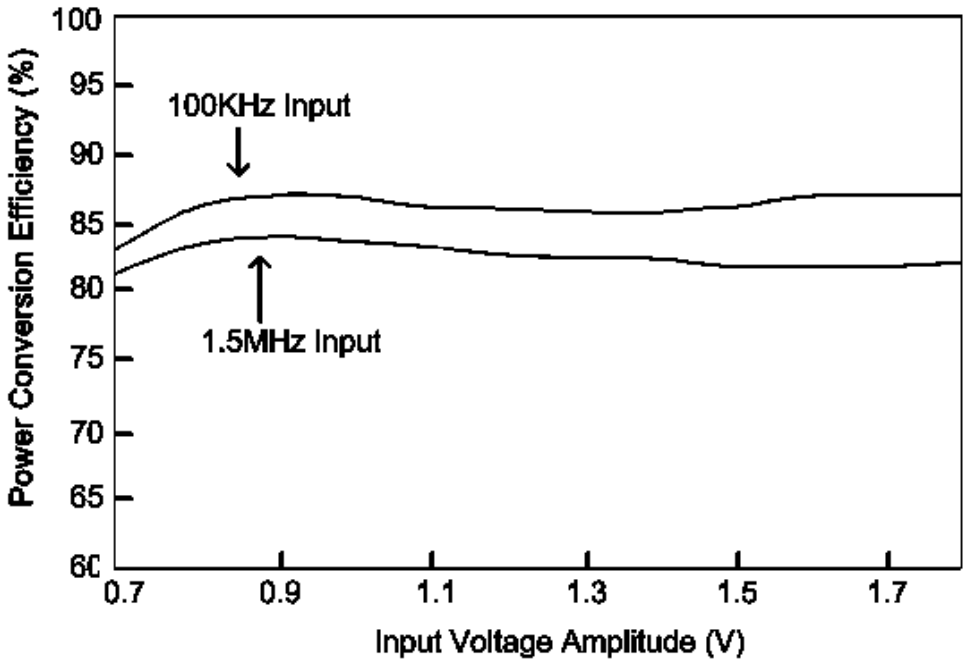


Figure 2.18: Simulated power efficiency versus different input amplitudes.

2.4.2 Power efficiency

The power efficiency of the rectifier is calculated using

$$\eta_p = \frac{\int_{t_1}^{t_1+T} v_{out}(t) \cdot i_{out}(t)dt}{\int_{t_1}^{t_1+T} v_{in}(t) \cdot i_{in}(t)dt}, \tag{2.4}$$

where T is one period. Figure 2.18 shows the simulated power efficiencies of our rectifier versus different frequencies. It indicates that the power efficiency is higher when the input frequency is as low as 100 kHz. The measurement results given in Fig. 2.19 also prove the simulation results. The reason is that the transistor switches of the negative voltage converter and of the comparator-controlled switch work as almost ideal switches. And high frequency will result more power loss in these switches, especially of the negative voltage converter since its large transistor scales. The proposed rectifier can achieve a simulated power efficiency of at least 81% and measurement result of 78% under different frequency references less than or equal to 1.5 MHz.

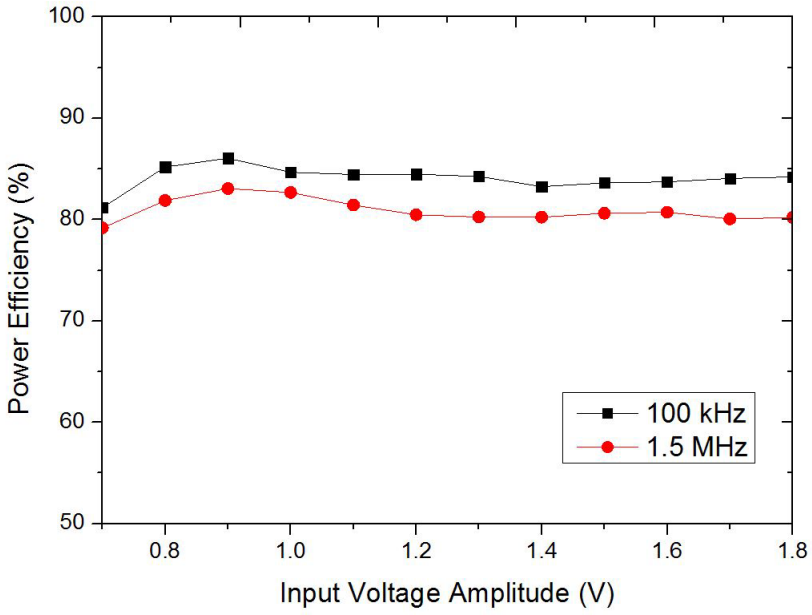


Figure 2.19: Measured power efficiency versus different input amplitudes.

2.4.3 Performance in different process corners

The proposed rectifier has been simulated when the process corners are the typical (TT), fast (FF) and slow (SS) of the 0.18 μm CMOS technology, respectively. The fluctuation of the voltage conversion rate is about ±3% between different process corners which can be accepted.

2.4.4 Performance in low frequency

Simulation results have shown that the proposed rectifier can work well in the frequency range from 100 kHz to 1.5 MHz. Besides biomedical implants devices, rectifiers are also used in some vibration energy harvesting systems to convert an AC power to DC ones. The output of vibration generator such as piezoelectric generator is usually within 100 Hz. In order to verify our design, we also simulate the proposed rectifier in low frequencies from 20 Hz to 100 Hz. Figures 2.20 and 2.21 show that this circuit can work even better in low frequency. Thus, it can be used in some vibration energy harvesting systems as well.

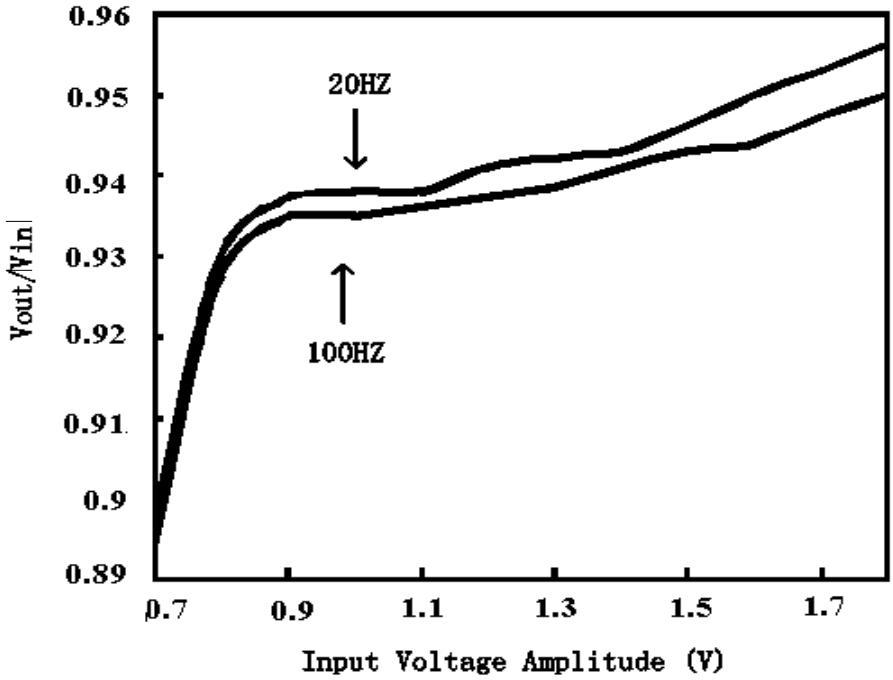


Figure 2.20: Voltage conversion efficiency of under low input source frequencies with RL=500 Ω.

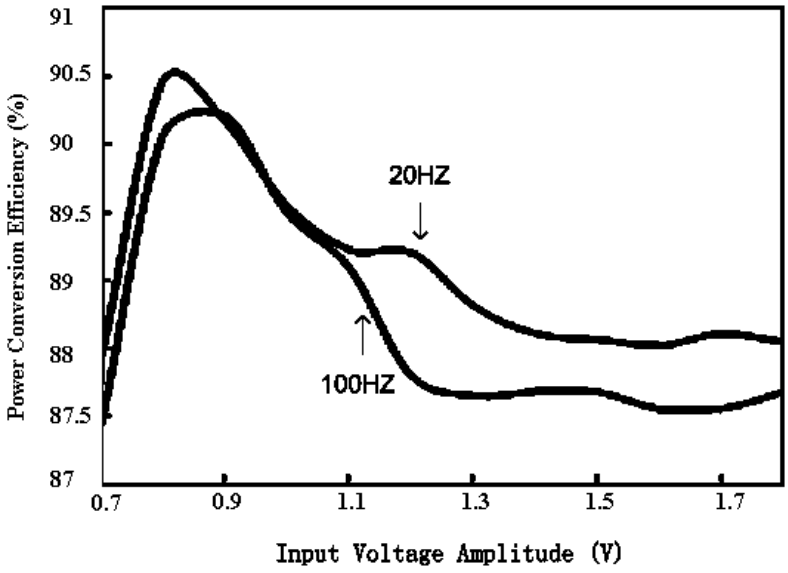


Figure 2.21: Power efficiency under low input frequencies with RL=500 Ω.

Table 2.2: Performance comparisons between rectifiers.

	TCAS II 06 [26]	JSSC09 [27]	This work
Input Amplitude| V_{in} |	1.5 V-3.5 V	1.2 V-2.4 V	0.7 V-1.8 V
Output Voltage	1.27 V-3.45V (unloaded) (Measured)	1.13 V-2.28 V (RL=2 kΩ) (Measured)	0.67 V-1.75 V (unloaded) (Measured)
V_{out}	1.2 V-3.22 V (RL=1.8 kΩ) (Measured)	0.98 V-2.08 V (RL=100 Ω) (Measured)	0.55 V-1.584 V (RL=500 Ω) (Measured)
| V_{in} |$_{min}$	1.5 V	1.2 V	0.7 V
Frequency	13.5 MHz	200 kHz-1.5 MHz	100 kHz-1.5 MHz
Power efficiency	65%-89% (Measured)	82%-87% (Simulated)	78.6%-86.5% (Measured)

2.4.5 Performance comparisons

Table 2.2 shows the performance of our proposed rectifier and other previous published papers. With even the same power efficiency, peak voltage conversion efficiency and range of frequency, the proposed rectifier can operate at a 0.7 V input amplitude which is far smaller than the minimum input voltage proposed in [27]. Moreover, the proposed circuit can also work in low frequency.

2.5 Summary

A low voltage CMOS rectifier for low power battery-less devices is presented. The rectifier is well suited for an input amplitude as low as 0.7 V by using a simple low supply voltage active diode. Additionally, by a small offset added in the comparator, the problem of reverse current is removed, which is important for reducing the voltage drop and improving the power efficiency. The proposed rectifier can achieve a maximum peak voltage conversion efficiency of more than 93% and a power efficiency of approximately 89%. Moreover, it can work better under low frequency input and can work stably in different corner models.

Chapter 3

Wide input amplitude range rectifier for energy harvesting system

3.1 Introduction

The field of energy harvesting technologies has a great development recently, which are stimulated by the advances of different researches [39], [40], [41], [42]. It plays a more and more important role in renewable resources and sensor systems. Comparing with conventional battery power systems, energy harvesting device has a long lifetime and is widely used in the system which is difficult to access to, because no battery replacement is needed. Among different types of energy harvesting technologies [43], [44], [45], [46], vibration energy harvester attracted a great deal of interest and it is well suited for technical environment, such as engines and railroad bridges. In those cases, source energy is harvested to supply low power devices and typical working frequency is between mHz and kHz [47]. Commonly, vibration energy harvesters generate an AC voltage, thus rectifier is needed to change the AC source to DC one which is used to power the load system. Moreover, the output voltage amplitudes of different micro harvesting generators may vary and output power is usually low, and therefore both efficiency and wide input amplitude range are needed for the rectifier design. Figure 3.1 shows the schematic of vibration

energy harvesting circuit interface and rectifier plays a very important role in the system. Based on the previous research, a high efficiency and wide input range rectifier will be presented here.

The chapter is organized as follows. In Section 3.2, the topologies and characteristics of passive and active rectifier are shown. The rectifier is proposed in section 3.3. Simulation results are given in Section 3.4, followed by a summary in Section 3.5.

3.2 Rectifier topologies

Conventional rectifiers consist of diodes and capacitor. The half-wave rectifier is consisted of a single diode and very simple. The full wave rectifier consisted of diode bridge makes full use of the input source, because both the negative and positive period pass to the load. Thus, the output voltage ripple is smaller than the half wave rectifier. Conventional diode rectifiers are suitable for high voltage and high power applications, because the diode forward voltage loss (0.7 V to 1 V) can be ignored in high voltage application without any influence to the efficiency. The large voltage drop decides it cannot be accepted in low voltage systems. Schottky diodes with a low forward voltage drop can replace the common diode to improve the efficiency. However, the high production cost and high reverse leakage current block its uses. In CMOS implementation circuits, diode-connected

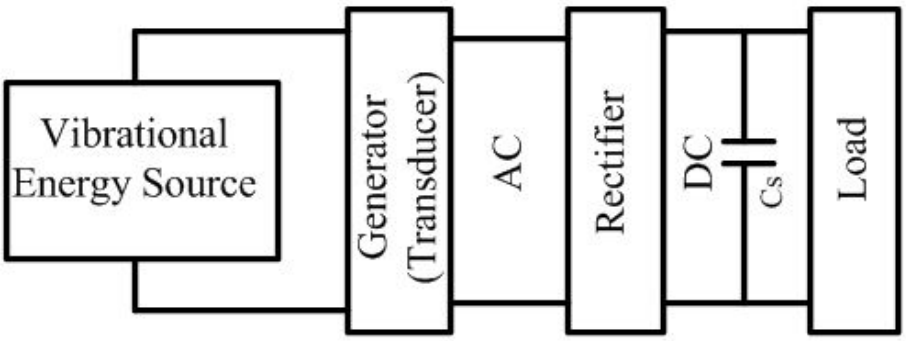


Figure 3.1: Schematic of vibrational energy harvester circuit interface.

CMOS transistor (gate connected to the drain) can be used to replace the semiconductor diode. Transistors with a low threshold voltage can be used to reduce the operation voltage. However, the additional masks and fabrication steps increase the extra cost. In [21], the author used a cross coupled PMOS structure to replace two semiconductor diodes of the diode-bridge structure. Input AC source is directly connected to the gate terminals to drive the PMOS transistors. However, the two switches are still in diode structure connection and voltage loss of a V_{th} still exist on each switch, thus the efficiency is not optimized for the voltage drop on the switch diode.

Although those passive rectifiers' structures are simple, the performances of them are poor. In order to achieve high voltage and power efficiency, active diode was presented and can be found in literatures [48], [26], [27]. It was used instead of the diode configured PMOS and NMOS transistors in the conventional rectifiers. The active diode is composed of a comparator controlled MOS transistor switch, working as an ideal diode without reverse current and voltage drop. In [26], [27], [49], they use two active diodes to replace the diode configured NMOS transistor in [21]. With active diode instead of passive diodes, high output voltage and high efficiency can be achieved. However, the minimum input voltages of some researches were still larger than 1.2 V [26], [27]. Aiming at saving the chip area and making the circuit simpler, rectifier with a negative voltage converter and just one active diode was proposed in [29]. By using the same concept, the minimum input voltage amplitude is further decreased to around 0.7 V [50], [51]. Recently, bulk-input comparator technique is presented in [24], [25] for ultra-low-voltage systems and the rectifier can work well with input voltage smaller than 1 V. However, the pn junction between bulk and source terminal of the input transistor will be turned on and bulk leakage current increase dramatically when operation voltage is larger than 1 V. Besides, the leakage current of the invertors used in them will also increase to the same order of the output current, which results in a poor power efficiency and large output voltage ripple. These drawbacks limit its scope.

In order to overcome these drawbacks, a high efficiency and wide input amplitude range rectifier is presented in this chapter. The minimum operation voltage is lower than previous

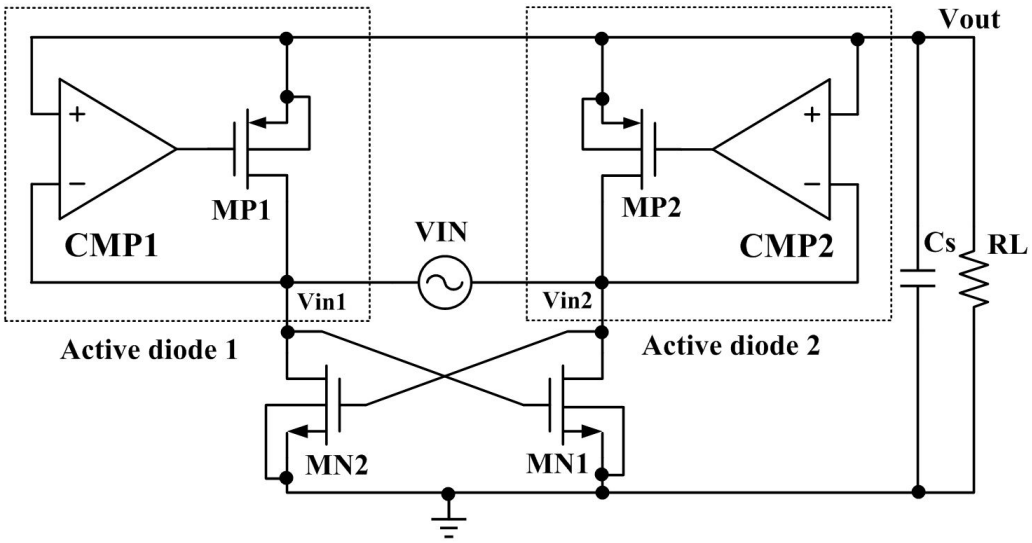


Figure 3.2: Conceptual schematic of the proposed rectifier.

published paper [24] and the rectifier can work at a wide range of input voltage amplitudes of 0.45 V up to 1.8 V compared with 0.5 V to 1 V in [24] and 0.3 V to 0.7 V in [25]. This allows the rectifier to work in different types of vibration energy harvesting systems.

3.3 Proposed rectifier and design consideration

3.3.1 Schematic and work principle

Figure 3.2 shows the proposed schematic of our rectifier. It is composed of a pair of cross-coupled connected NMOS transistors and two active diodes. The cross-coupled transistors work as switches. The voltage drop on each switch is only $|V_{dsn}|$ when the switch is turned on. The active diodes are two comparator controlled switches work as ideal diodes with even no voltage drops and no reverse current. The two-terminals comparator CMP1 and CMP2 control the gate voltage of MP1 and MP2 by comparing voltage V_{in1} (V_{in2}) with V_{out}. Transistors MP1 or MP2 will only be turned on to charge the load capacitor under the condition of V_{in1} (V_{in2})>V_{out}.

The operation principle of proposed structure is given here. An sinusoidal source voltage V_{in} (V_{in1}-V_{in2}) is used as the input signal. When the input source is in the positive cycle,V_{in}=V_{in1}-V_{in2}>0. When V_{in}<|V_{thn}|, MN1 is always off. Since V_{in2}<V_{in1}<V_{out}, MP1 is also off and no current flows to the load RL, thus RL is powered by the charge capacitor C_s. When the V_{in} increases and is larger than |V_{thn}|, MN1 will be turned on and shorts V_{in2} to ground potential. Then any increase of the input voltage will reflect to the increase of V_{in1}. Though V_{in1} is increasing, MP1 will still keep the off status, because V_{in1} is smaller than V_{out}. Thus, the output voltage of CMP1 will be high and no current charges the output capacitor. When V_{in} increases and larger than V_{out}, the output voltage potential of CMP1 is low to turn on the MP1. As the MN1 is still in on status, MN1 and MP1 construct a conductive branch and current flows through the transistors to the output terminal. The switch transistor MP1 will be turned off again when the voltage amplitude of V_{in} decreases and smaller than V_{out}. And both MP1 and MN1 are off when V_{in} decreases to 0<V_{in}<|V_{thn}|. During the negative half cycle of the input (V_{in}<0), MP2 and MN2 will work with the same principle. In each conductive branch, the PMOS transistor and NMOS transistor work at linear region when both two transistors are turned on. In order to reduce the corresponding voltage drops ($\left|V_{dsp}\right|$ and V_{dsn}, where $\left|V_{dsp}\right|$ and V_{dsn} are drain-source dropout voltages of PMOS transistors MP1/MP2 and NMOS transistors MN1/MN2, respectively), the size of both PMOS and NMOS transistors should be large enough to reduce the on resistance. Thus, the output voltage can be expressed as

$$V_{out} = \left|V_{inp}\right| - \left|V_{dsp}\right| - V_{dsn}. \tag{3.1}$$

where $\left|V_{inp}\right|$ is the peak voltage amplitude of the input V_{in}.

3.3.2 Proposed control circuit

Figure 3.3 shows the schematic of the proposed active diode. The active diode is designed to control the current direction and to work nearly as an ideal diode with only $\left|V_{dsp}\right|$ voltage drop. It consists of a PMOS switch which is driven by a low operation-voltage comparator.

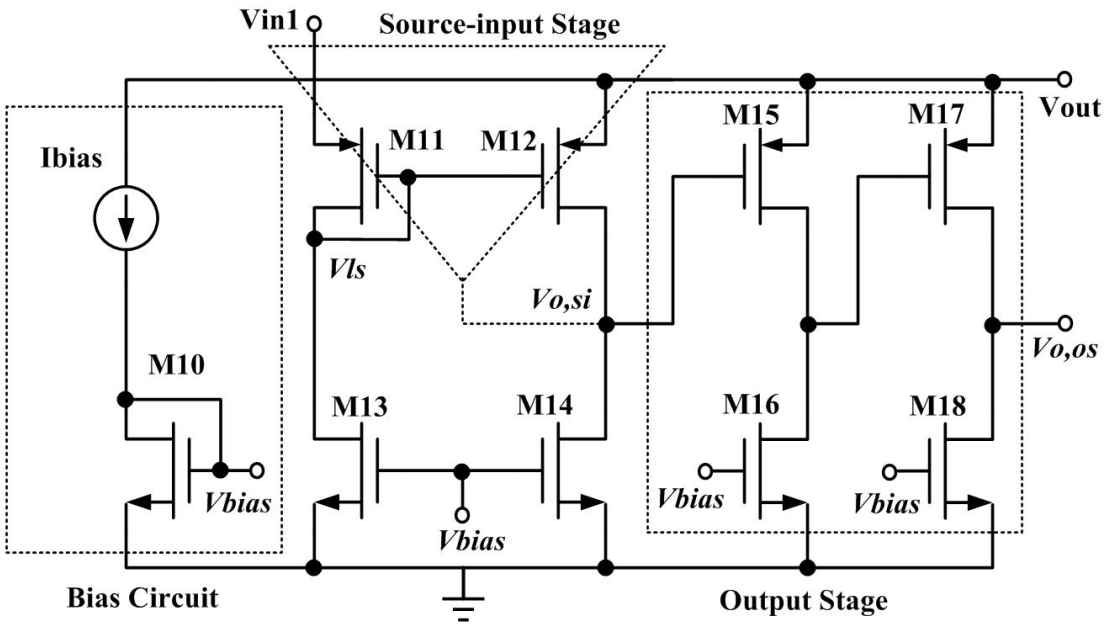


Figure 3.3: Schematic of the proposed active diode.

The key part of the active diode is comparator design. For wide input range case, the comparator should not only work under a low input of 0.45 V but also work well with a high input amplitude. Moreover, the power consumption must be very low due to the fact that the power is supplied by the storage capacitor C_s. Thus, significant efforts are needed to meet those requirements.

The comparator consists of 3 stages as shown in Fig. 3.3: i) Bias circuit; ii) Source-input stage; iii) Output stage. The bias circuit is used to supply a low bias voltage to gate of M13, M14, M16, and M18 and makes them work in the weak inversion region. This can reduce the branch currents and power consumption dramatically. The source input stage consists of a voltage level shifter and a common source amplifier. Two cascade common source amplifiers are used for the output stage to drive large gate capacitance of PMOS switch. When the voltage potential of V_{in1} decreases and is smaller than V_{out}, V_{ls} will decrease and $V_{o,si}$ will be pulled up. Thus, the output voltage potential of the source-input stage will be high. However, $V_{o,si}$ cannot drive the PMOS switch directly, and an output stage consists of two common-source amplifiers is used to enhance the gain and change

the $V_{o,si}$ into a nearly digital output signal $V_{o,os}$. Thus, the potential $V_{o,os}$ will be high and PMOS will be turned off to avoid the reverse current. In the opposite, when the voltage potential of V_{in1} is larger than V_{out}, $V_{o,os}$ will be low and PMOS will be turned on to charge the load system.

Moreover, the minimum operation voltage is also a key index for the proposed rectifier, which is shown in Fig. 3.3. In each branch of the source-input stage, there is a pair of NMOS and PMOS transistors. Since the branch current is very small in our design, the minimum supply voltage of the comparator is mainly decided by threshold voltage of branch transistors. From Eq. 3.1, since $|V_{dsp}|$ and V_{dsn} can be minimized by large scale transistors, the proposed rectifier can operate at even one threshold voltage.

3.3.3 Latch-up consideration

Commonly, the bulk terminals of PMOS and NMOS transistors are connected to the highest and lowest potential. In this case, they are tied to V_{out} and GND, respectively. In the steady state, when MP1 and MP2 are off ($V_{in1}<V_{out}$ and $V_{in2}<V_{out}$), the pn junction between bulk and source terminals of all transistors will in the off status, which can be verified in Fig. 3.4. When MP1 (MP2) is turned on, the input source V_{in} will charge the storage capacitor C_s through the conductive branch MN1 and MP1 (MN2 and MP2). Thus, the voltage differences between GND and the lowest potential V_{in2} (V_{in1}) and the ones between V_{out} and the highest potential V_{in1} (V_{in2}) are V_{dsn} and $|V_{dsp}|$, respectively, which can also be found in Fig. 3.4. $|V_{dsp}|$ and V_{dsn} can be minimized by using large scale transistors. The simulation shows that the $|V_{dsp}|$ and V_{dsn} are less than 10 mV in our case. Thus, the pn junction between bulk and source terminals of all PMOS and NMOS transistors will never be turned on, which means that there will be no latch up in the steady state.

Moreover, the start up state should be also considered. Figure 3.5 shows the waveform of the rectifier in start-up state. In the start-up state, the peak amplitude of V_{in1} is always close to 1.8 V, which turns on the substrate parasitic bipolar junction transistor of MP1. However, the voltage differences between the bulk terminal and source terminal of all

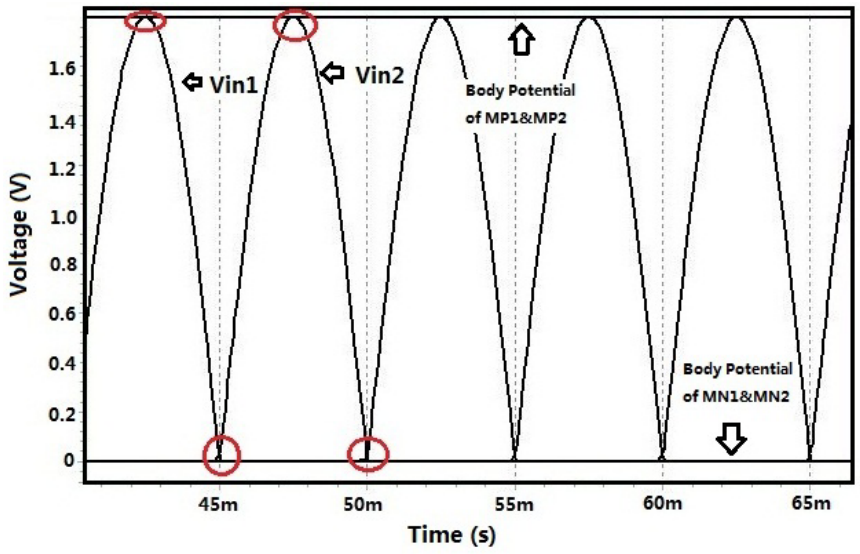


Figure 3.4: Simulated waveform of the rectifier in steady-stage under the input condition of 100 Hz and 1.8 V.

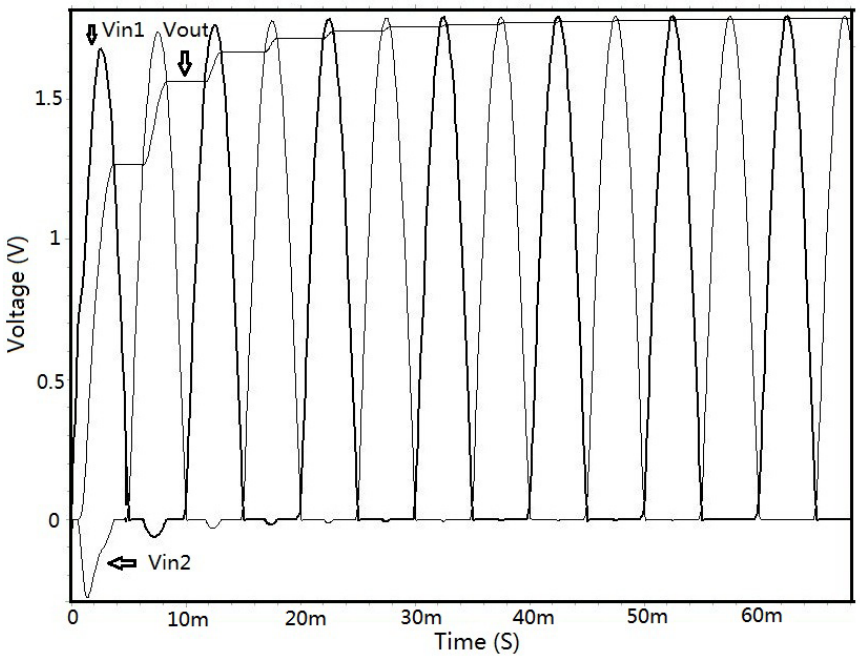


Figure 3.5: Simulated waveform of the rectifier in start-up state under the input condition of 100 Hz and 1.8 V.

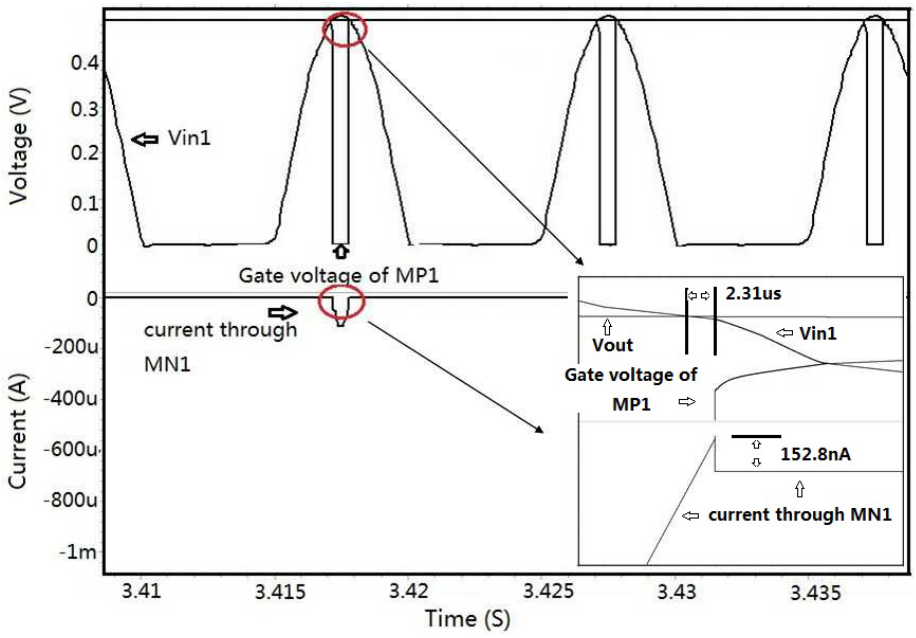


Figure 3.6: Simulated waveform of the CMP1 under the input condition of 0.45 V and 100 Hz.

NMOS transistors are not large enough to turn on the body p-n junction. Thus, the substrate parasitic bipolar junction transistor of the NMOS transistor is off and no latch-up occurs in the start-up state. Hence, there will be no latch up in our proposed rectifier in both the steady-state and start-up state. This mechanism saves the chip area of bulk regulator used in previous published papers [24], [25].

3.3.4 Reverse current consideration

There will be reverse current from V_{out} to V_{in} if the transistor switch is still on when V_{out}>V_{in}. Large reverse current can severely degrade the power efficiency and increase output voltage ripple. Figure 3.6 and Fig. 3.7 show the simulated waveforms of the comparator under the input condition of 0.45 V. In order to verify the phenomena accurately, we did a more precise simulation with a much small time step value and enlarge the part marked with red circle. Results show that the time delays for two comparators are only 2.31 us and 2.32 us, respectively. The peak amplitude of the reverse current is about 153 nA, which is far less than the peak amplitude of the current through MN1 and MN2.

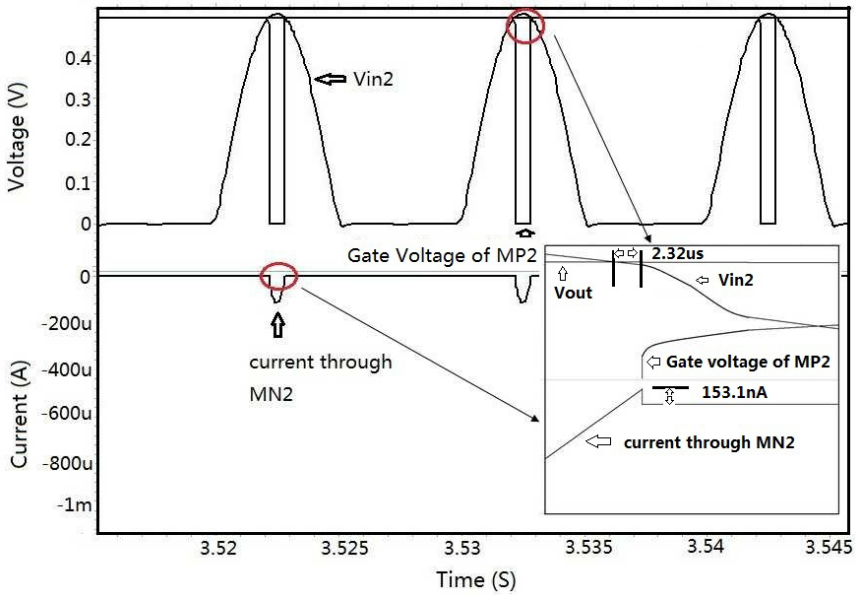


Figure 3.7: Simulated waveform of the CMP2 under the input condition of 0.45 V and 100 Hz.

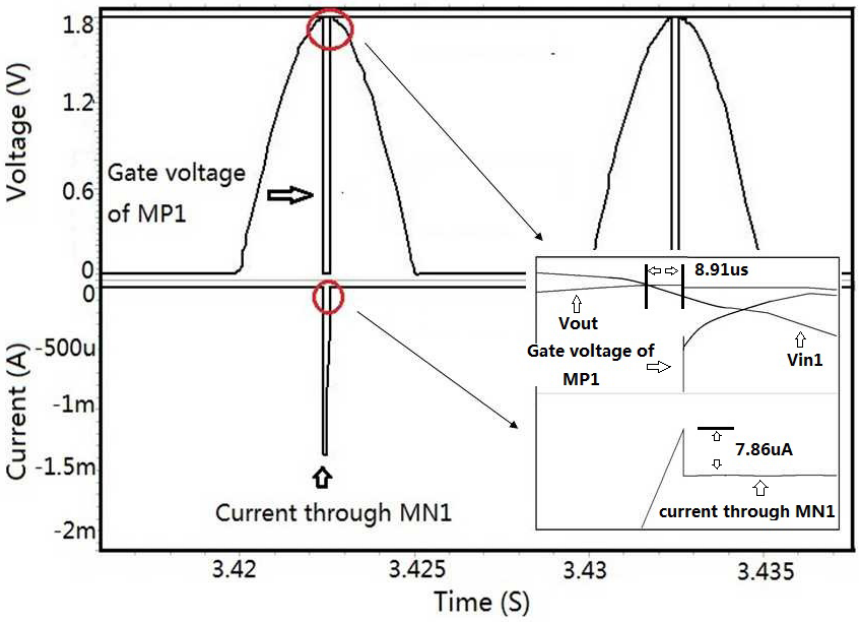


Figure 3.8: Simulated waveform of the CMP1 under the input condition of 1.8 V and 100 Hz.

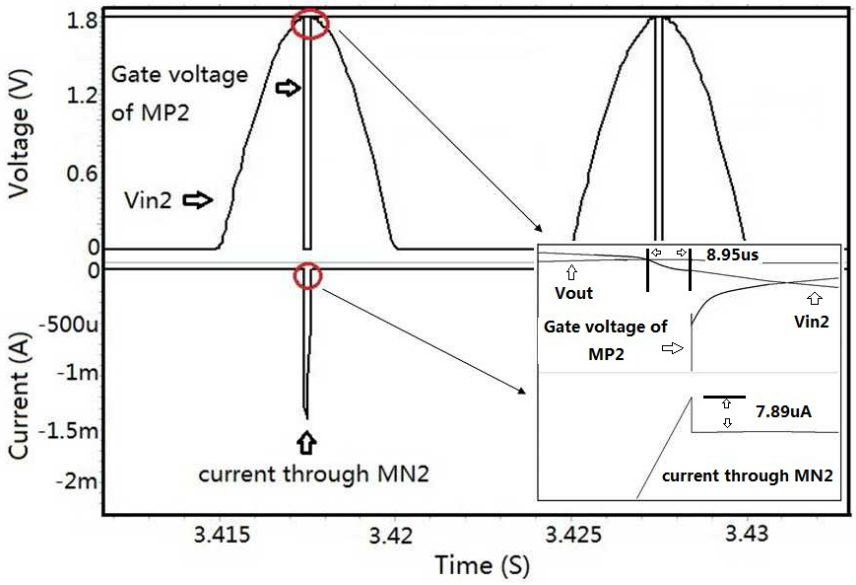


Figure 3.9: Simulated waveform of the CMP2 under the input condition of 1.8 V and 100 Hz.

Figure 3.8 and Fig. 3.9 are results under the condition of 1.8 V, and the reverse current is still much smaller than the currents through MN1 and MN2. Therefore, higher power efficiency can be achieved by reducing the revers current.

3.4 Simulation and measurement results

The main aspects of the rectifier are wide input voltage range, output voltage conversion efficiency, power efficiency, and power consumption, which will be discussed respectively. The proposed rectifier is shown in Fig. 3.10. Table 3.1 shows the size of all transistors used.

In order to verify the proposed rectifier for vibration energy harvesting system, the circuit was simulated and fabricated using a standard 0.18 μm CMOS process. A pure sinusoidal waveform whose frequency changes from 10 Hz to 1 kHz is applied to the input of the rectifier through a transformer. Additionally, a capacitance of 10 μF and a load of 50 kΩ are used for common test. In order to promise the output voltage ripple, capacitances value will be changed according to the input frequency. In our case, 100 μF and 1 μF are

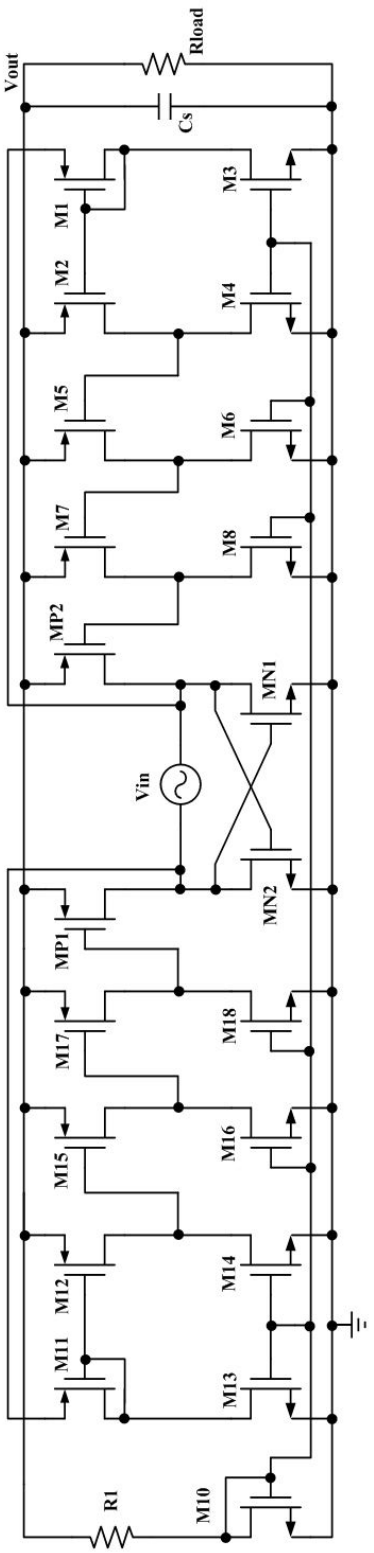


Figure 3.10: Schematic of the proposed rectifier.

Table 3.1: Circuit transistor sizes.

	Unit Size	Multiply Factor		Unit Size	Multiply Factor
MP1	10um/0.18um	150	M8	2.3um/0.18um	1
MP2	10um/0.18um	150	M10	2.3um/0.18um	1
MN1	10um/0.18um	150	M11	1.8um/0.18um	5
MN2	10um/0.18um	150	M12	1.8um/0.18um	5
M1	1.8um/0.18um	5	M13	2.3um/0.18um	1
M2	1.8um/0.18um	5	M14	2.3um/0.18um	1
M3	2.3um/0.18um	1	M15	1.8um/0.18um	5
M4	2.3um/0.18um	1	M16	2.3um/0.18um	1
M5	1.8um/0.18um	5	M17	1.8um/0.18um	5
M6	2.3um/0.18um	1	M18	2.3um/0.18um	1
M7	1.8um/0.18um	5			

chosen for 10 Hz and 1 kHz, respectively. The value of R1 used in the bias circuit is 2 MΩ. Based on the layout estimation with a poly silicon sheet resistance of 2 kΩ, the bias resistor occupied a smaller area compared with the large size power transistors, only 4.2% of the total estimation chip area. It can also be replaced by a off-chip resistor in the circuit implementation. Thus, it is acceptable in our design. The test circuit for chip measurement is same with the circuit in chapter 2. A transformer ST29A is directly utilized to transfer the input source from the signal generator. The ratio of the transformer is 1.28:1. The photograph of our designed low voltage rectifier is given in Fig. 3.11, the total chip area is only 0.026mm^2 without the pads area. This is much smaller and only 36% of state-of-the art in previous rectifiers, where the chip area is 0.072mm^2.

3.4.1 Input range and voltage conversion efficiency

The proposed rectifier can work at a wide range of input voltage amplitudes of 0.45 V up to 1.8 V, which is decided by the threshold voltage and breakdown voltage of the standard 0.18 μm CMOS process. The gate-source breakdown voltage of a standard 0.18 μm CMOS process is 1.8 V, thus the input peak voltage amplitude $\mid V_{inp} \mid$ should be restricted under this value. However, the maximum input voltage amplitude can be easily enlarged by using

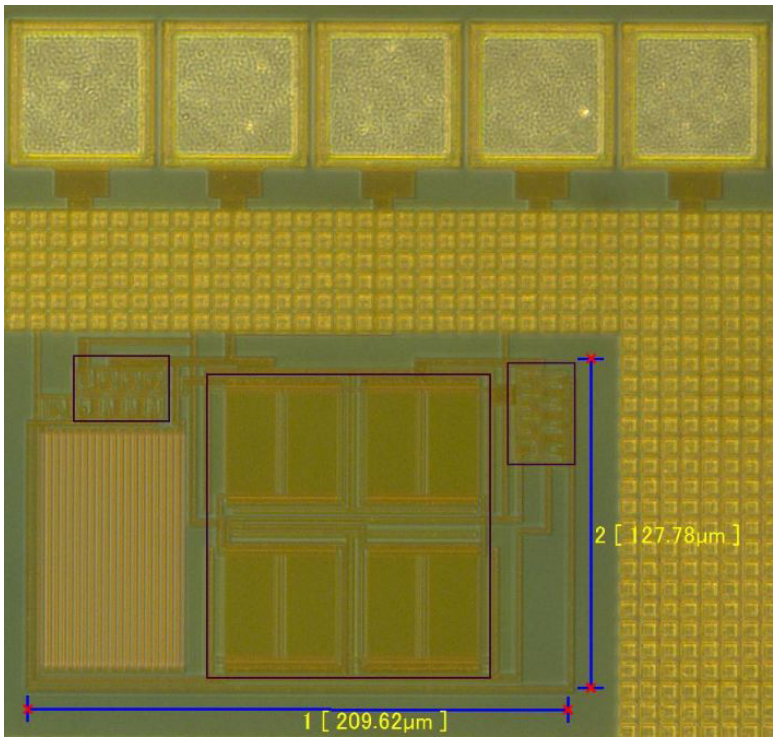


Figure 3.11: Chip photograph of the fabricated rectifier.

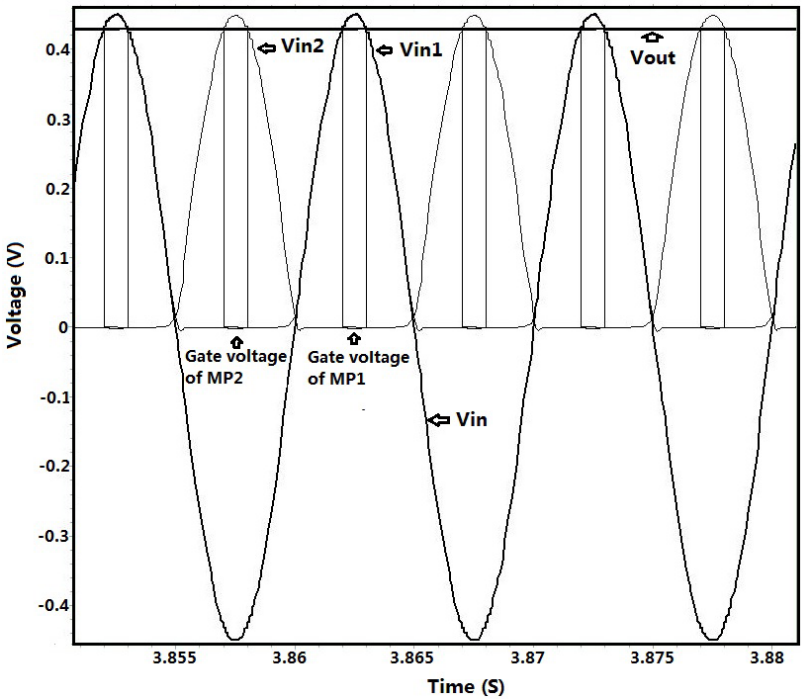


Figure 3.12: Simulated steady-state of the circuit under a minimum input voltage of 0.45 V.

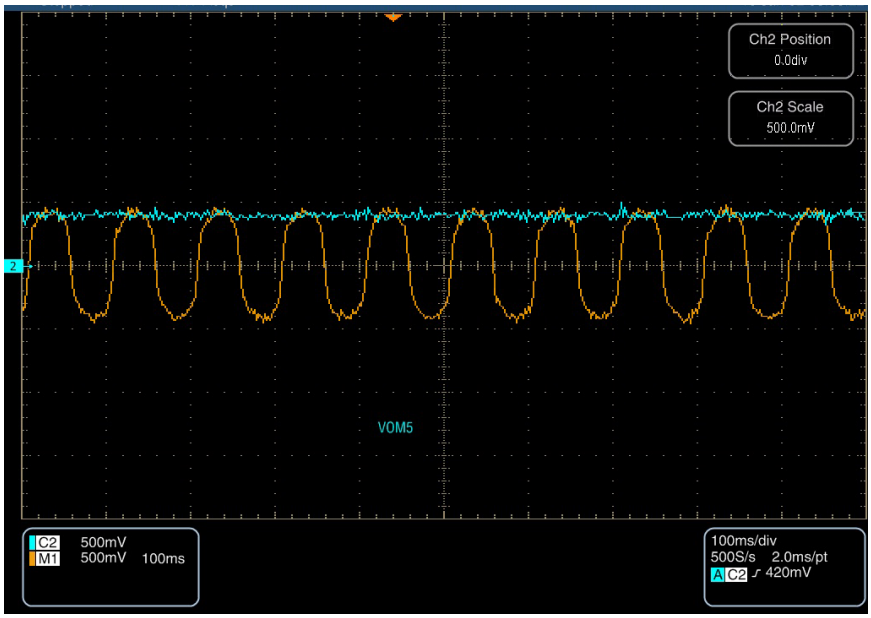


Figure 3.13: Measured steady-state of the rectifier under minimum input voltage 0.45 V and frequency of 10 Hz.

high breakdown voltage process without decreasing the efficiency. Because, the novel structure decides that no bulk-source leakage current exits in the proposed circuit when input voltage amplitude increases. This allows the rectifier to work in different types of vibration energy harvesting system. The voltage efficiency η_v is calculated by the fraction of the output voltage V_{out} and peak voltage amplitude of then input $\mid V_{inp} \mid$, which is shown in Eq. 3.2.

$$\eta_v = \frac{V_{out}}{\mid V_{inp} \mid}. \tag{3.2}$$

Both simulations and measurements are done to verify the performance of our proposed rectifier. Figure 3.12 is the simulation working state under minimum input voltage of 0.45 V and the rectifier can achieve a voltage conversion efficiency of 95%. The measured working states under minimum input voltage of 0.45 V are given in Fig. 3.13 and Fig. 3.14, which show that the proposed rectifier can work well in the frequency range from 10 Hz to 1 kHz even under a low input voltage of 0.45 V. Figure 3.15 shows the input voltage range and simulated voltage conversion efficiency versus different ohmic loads.

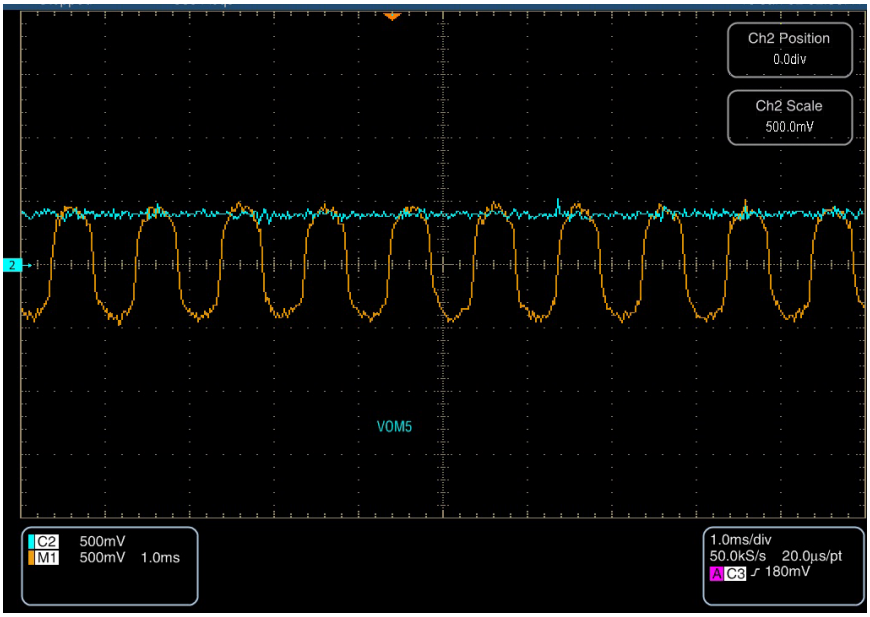


Figure 3.14: Measured steady-state of the rectifier under the minimum input voltage 0.45 V and frequency of 1 kHz.

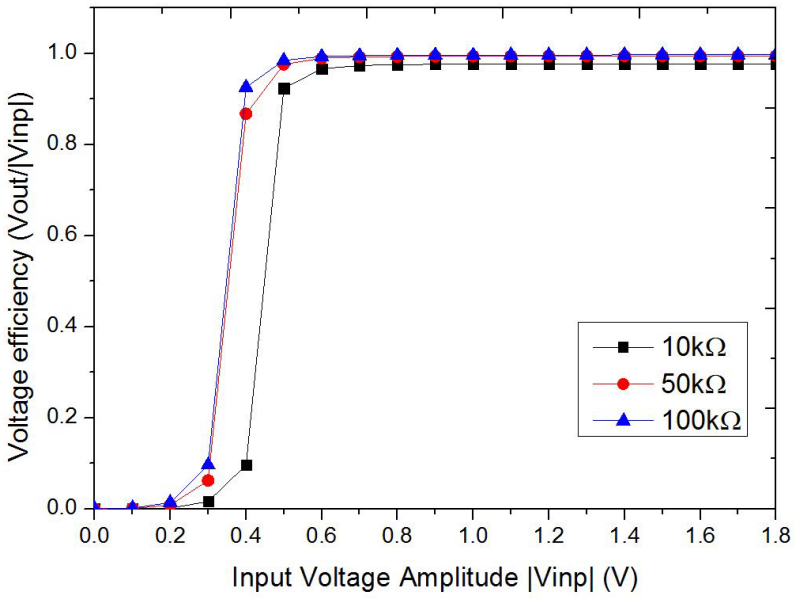


Figure 3.15: Simulated voltage conversion efficiency versus input voltage amplitudes with 100 Hz input source frequency.

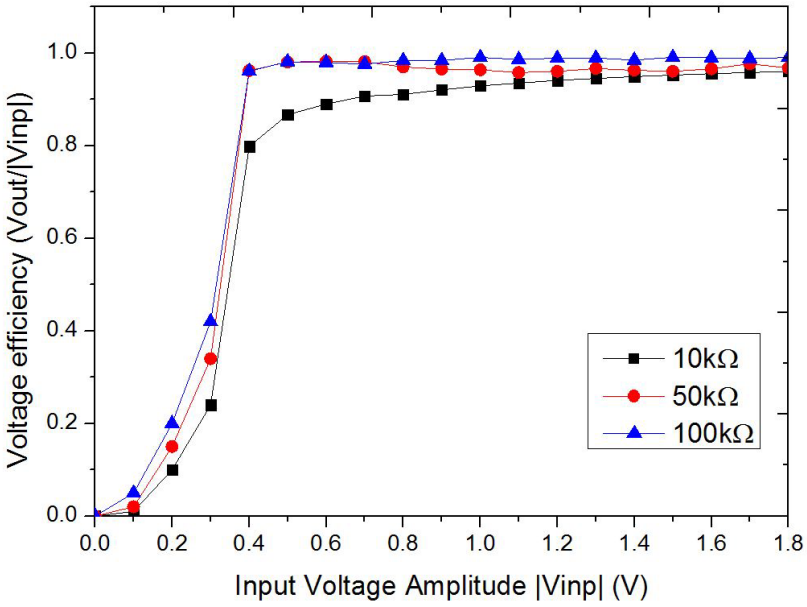


Figure 3.16: Measured voltage conversion efficiency versus input voltage amplitude with a 100 kHz input source.

The average conversion efficiency is above 95% when the input amplitude is larger than 0.45 V. When the amplitude of input voltage decreases down to 0.45 V, the transistors MN1 and MN2 will enter into the weak inversion region, and even cut off. Thus, the voltage conversion efficiency decreases dramatically. Note that output voltage efficiency of the rectifier is higher with larger load resistors, which is easy to be understood as a voltage divider. The measurement results of voltage conversion efficiency in Fig. 3.16 further proves the simulation results. The maximum voltage conversion efficiency is close to 95% with a 100 kΩ load. In Fig. 3.16, we can find that the rectifier can work with even 0.4 V input voltage amplitude. The differences between simulation and measurements can be accepted.

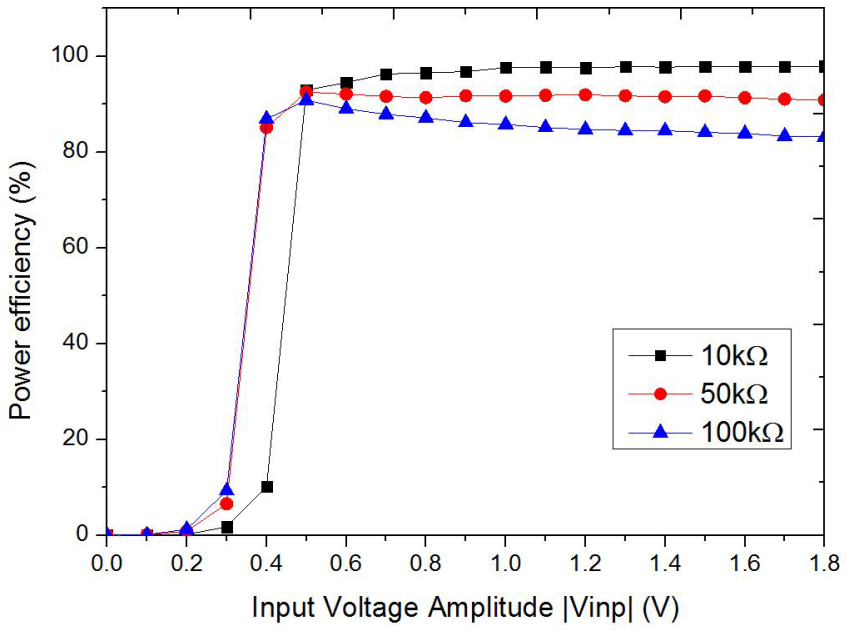


Figure 3.17: Simulated power efficiency versus input voltage amplitudes with a 100 Hz input source.

3.4.2 Power efficiency

The power efficiency of the rectifier is calculated using Eq. 3.3 or Eq. 3.4

$$\eta_p = \frac{\int_{t_1}^{t_1+T} v_{out}(t) \cdot i_{out}(t)dt}{\int_{t_1}^{t_1+T} v_{in}(t) \cdot i_{in}(t)dt}, \tag{3.3}$$

$$\eta_p = \frac{{V_{out}}^2/R_{load}}{\int_{t_1}^{t_1+T} v_{in}(t) \cdot i_{in}(t)dt}, \tag{3.4}$$

where T is one period of the input signal and t_1 is the start time. As the output voltage of the proposed rectifier is constant, thus the Eq. 3.3 is the same as Eq. 3.4. Figure 3.17 shows the simulated power efficiency versus different input voltage amplitudes under three types load condition. With increasing R_{load}, the efficiency decreases, because the current through the ohmic load decreases and tends to the current through the comparator. Power efficiency also varies with different input amplitudes. With low input voltage smaller than the threshold voltage, the power transistors will cut off or work in the weak inversion

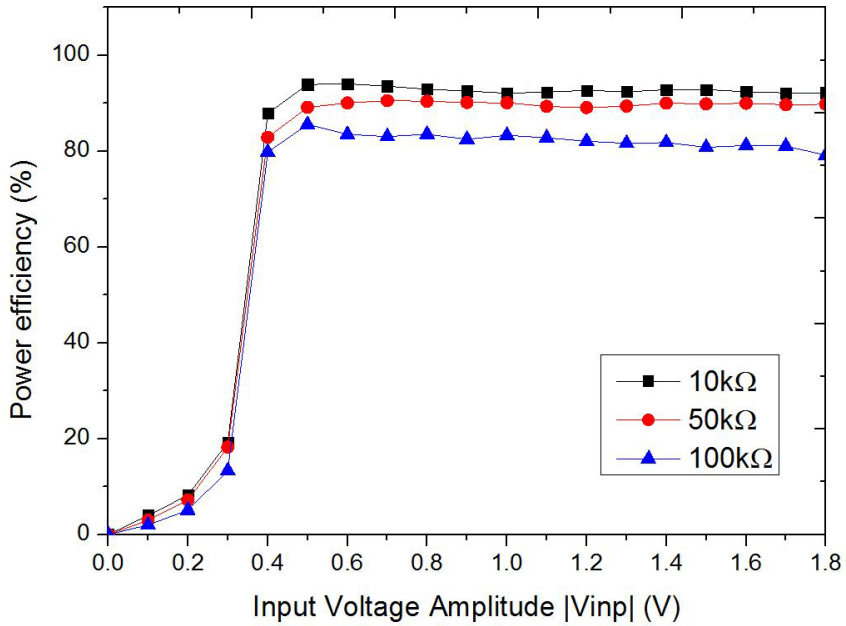


Figure 3.18: Measured power efficiency versus input voltage amplitudes with a 100 Hz input source.

region, which means the output current is very small. Thus, the power efficiency is very poor in the low voltage range. The measurement results in Fig. 3.18 also verified the simulation results. The smaller of the load is, the larger of the power efficiency is.

3.4.3 Working frequency

The voltage conversion efficiency and power efficiency versus the input voltage amplitude for different input frequencies is simulated and shown in Fig. 3.19 and Fig. 3.20. The measurement results of voltage efficiency versus frequency and power efficiency are also given in Fig. 3.21 and Fig. 3.22. Different load capacitors are adapted for the applied frequencies to maintain a small output voltage ripple. At 1 kHz the output voltage at 1.8 V input voltage amplitude is 2% lower compared to the 10 Hz measurement. The power efficiency at high frequency is a little smaller than the performance at low frequency. This is due to the frequent switching of the power transistors, which consuming more power at high frequency. All the simulation and measurement results show that the rectifier can work

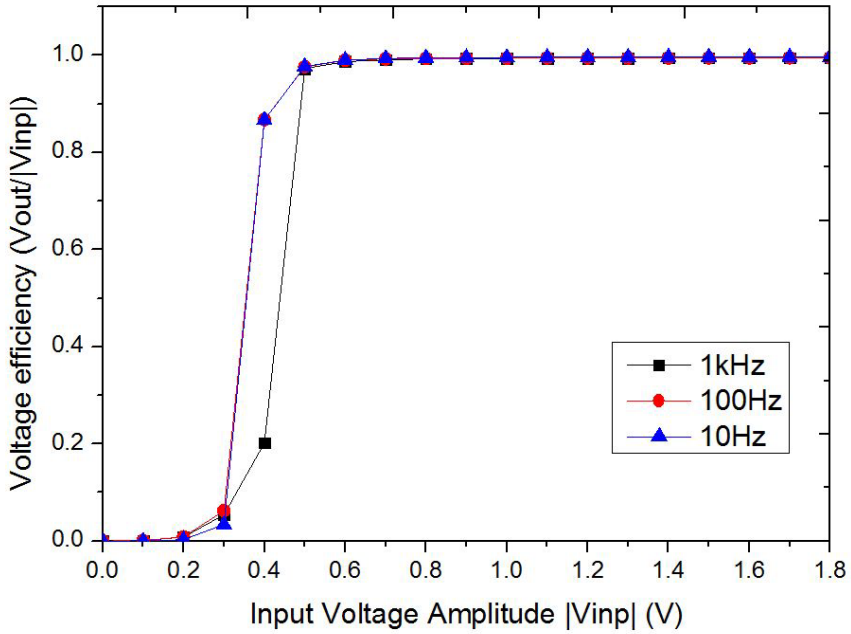


Figure 3.19: Voltage conversion efficiency versus input voltage amplitudes with different frequencies.

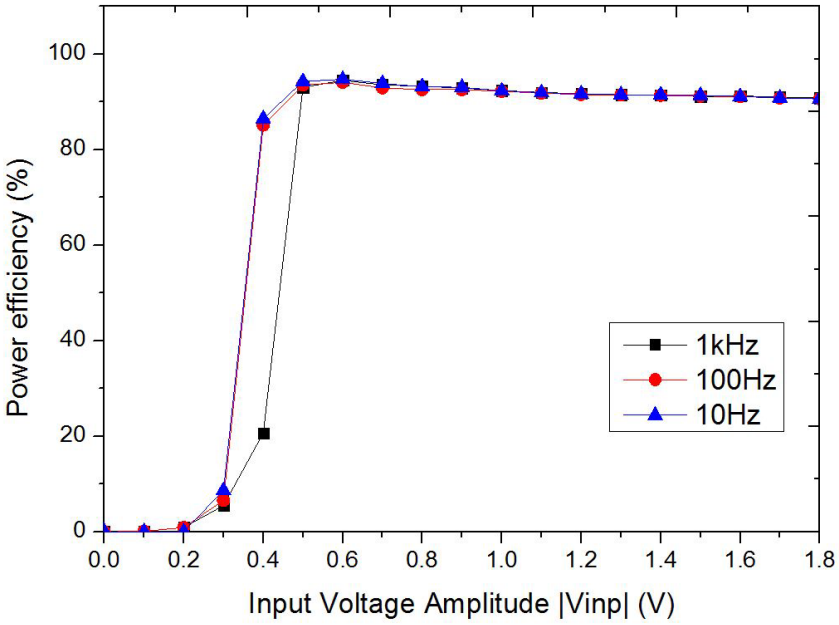


Figure 3.20: Power efficiency versus input voltage amplitudes with different frequencies.

well in the frequency range and the working frequency range of this rectifier is sufficient for most vibration energy harvesting applications.

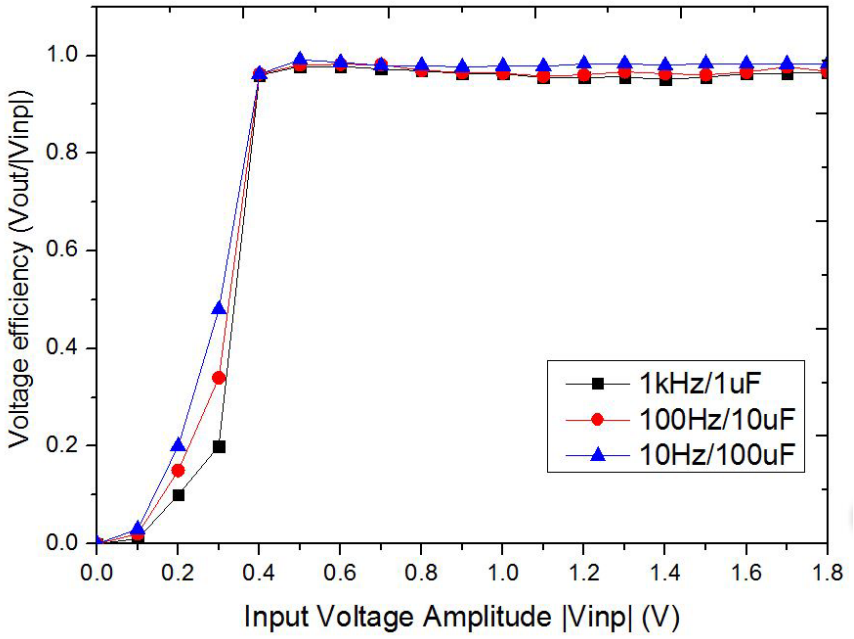


Figure 3.21: Measured voltage conversion efficiency versus different input voltage amplitudes with a 50 kΩ.

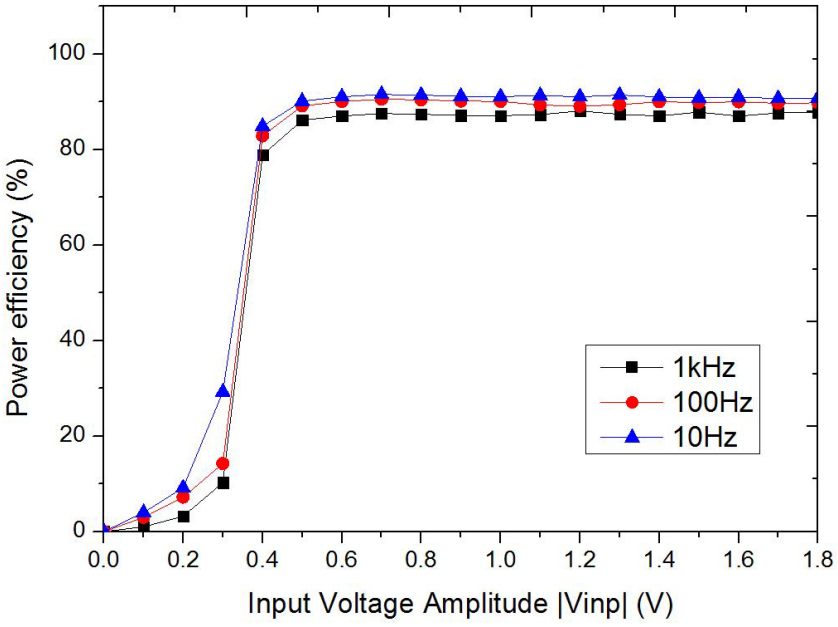


Figure 3.22: Measured power conversion efficiency versus different input voltage amplitudes with a 50 kΩ.

Table 3.2: Power consumption.

STAGE	POWER CONSUMPTION [nW]
CMP1	84.80
CMP2	84.75
MN1	6.41
MN2	6.40
MP1	40.96
MP2	41.03
Total power loss	264.35

3.4.4 Power consumption

The static power consumption of the rectifier is tested. In order to compare with previous published papers, Table 3.2 shows the power consumption of different stages under a 0.5 V input amplitude condition. CMP1 and CMP2 are the main power consumption sources. MP1 and MP2 who play a role of switch also dissipated much power. The results show that the power consumption at 500 mV is only 264.35 nW, which is much smaller than the best recently published result in [24]. Besides the self power consumption, the input power supplied by energy harvesting device and the load power consumption are also very important. Commonly, the electric energy generated by some vibration energy harvesting device is larger than uW, typically larger than 100uW [52], [53], [54]. In the previous published papers, no one consider the relation between the vibration source and power of the load resistor used. The load power of the rectifier should be under the maximum power level supplied by the previous stage. With a 50 kΩ load used in the test, the maximum load power can be reached is 64.1 uW under the input amplitude of 1.8 V, which is far less than the maximum output power of the input source [54].

3.4.5 Corner simulation

The proposed rectifier has been simulated when the process corners are the typical (TT), fast (FF) and slow (SS) of the 0.18 μm CMOS technology, respectively. The fluctuation

of the peak voltage conversion efficiency is about ±4% between different process corners which can be accepted.

3.4.6 Performance comparisons

Table 3.3 shows the performance of our proposed rectifier comparing with other previous designs. From previous designs and comparison, only [24] and [25] are designed for low frequency vibration energy harvesting systems. The lowest operation voltage of previous rectifiers is 0.28 V in [25] with a 0.18 μm CMOS process. However, the bulk input structure decided that it cannot work when the input voltage is larger than 0.7 V and the efficiency is very poor under low input condition, which blocks its application field. A low threshold voltage 0.35 μm CMOS process is used in [24] and makes the highest voltage up to 1 V, but still much smaller than one VDD. The bulk leakage current still exists and decreases the efficiency a lot when input voltage amplitude is larger than 1 V. In order to reduce the voltage drop and minimize the lowest input voltage amplitude, both [24] and [25] use large size power transistors which increase the chip area too much, especially in [25]. The rectifier proposed in this chapter overcame these drawbacks. It can not only work at a 0.45 V input voltage, but also operate at a wide range input voltage amplitudes of 0.45 V up to 1.8 V. Moreover, power efficiency and peak voltage efficiency and are dramatically improved in our design, and power transistor size is also reduced.

Besides the performance comparisons shown in Table 3.3, we also simulated all three rectifiers under the same condition for a fair comparison. In the simulation, a standard 0.18 μm CMOS technology process is used. The load capacitor and resistor are settled to 10 uF and 50 kΩ, respectively. Additionally, the power transistors used in all rectifiers have the same size, considering the drain-source voltage drop. Figure 3.21, Fig. 3.22 and Fig. 3.23 demonstrate the detail comparisons of the rectifiers in terms of voltage conversion efficiency, power efficiency and output voltage ripple under the condition of 100 Hz input source frequency.

Table 3.3: Performance comparisons between rectifiers.

	JSSC 2009 [27]	NOLTA 2011 [25]	TCAS I 2011 [24]	This work
Technology	0.35 μm CMOS	0.18 μm CMOS	0.35 μm Low V_{th} CMOS	0.18 μm CMOS
Input Amplitude $\mid V_{in} \mid$ range	1.2 V-2.4 V	0.28 V-0.7 V	0.5 V-1 V	0.45 V-1.8 V
Voltage efficiency	81.7%-86.7% (RLoad=100 Ω) (Measured)	76%-97% (RLoad=40 kΩ) (Simulated)	90%∼ (RLoad=50 kΩ) (Measured)	95.8%-98.2% (RLoad=50 kΩ) (Measured)
$\mid V_{in} \mid_{min}$	1.2 V	0.28 V	0.5 V	0.45 V
Frequency	200 kHz-1.5 MHz	10 Hz-3 kHz	10 Hz-10 kHz	10 Hz-1 kHz
Power efficiency	82%-87% (Simulated)	78%-95% (Simulated)	70%-95% (Measured)	86%-91.6% (Measured)
Power transistor size W/L	-	50000 um/0.18 um	4500 um/0.35 um	1500 um/0.18 um

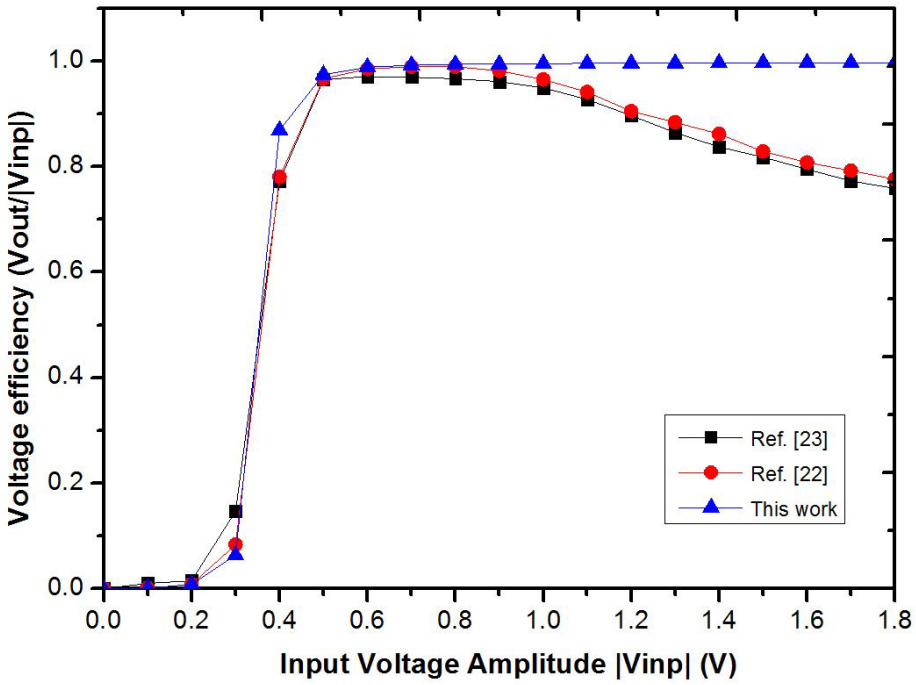


Figure 3.23: Voltage conversion efficiency comparison with previous published papers.

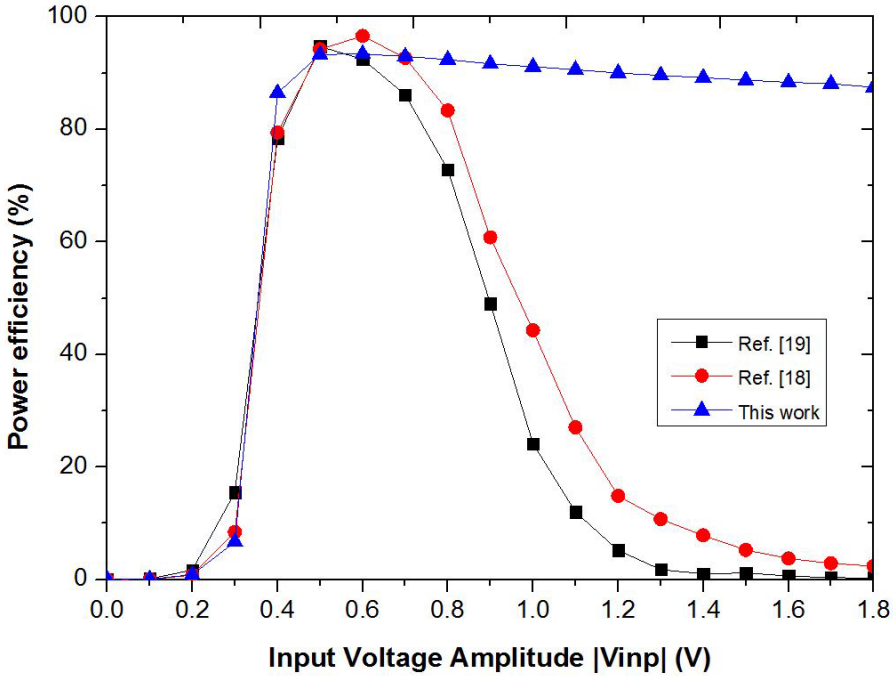


Figure 3.24: Power efficiency comparison with previous published papers.

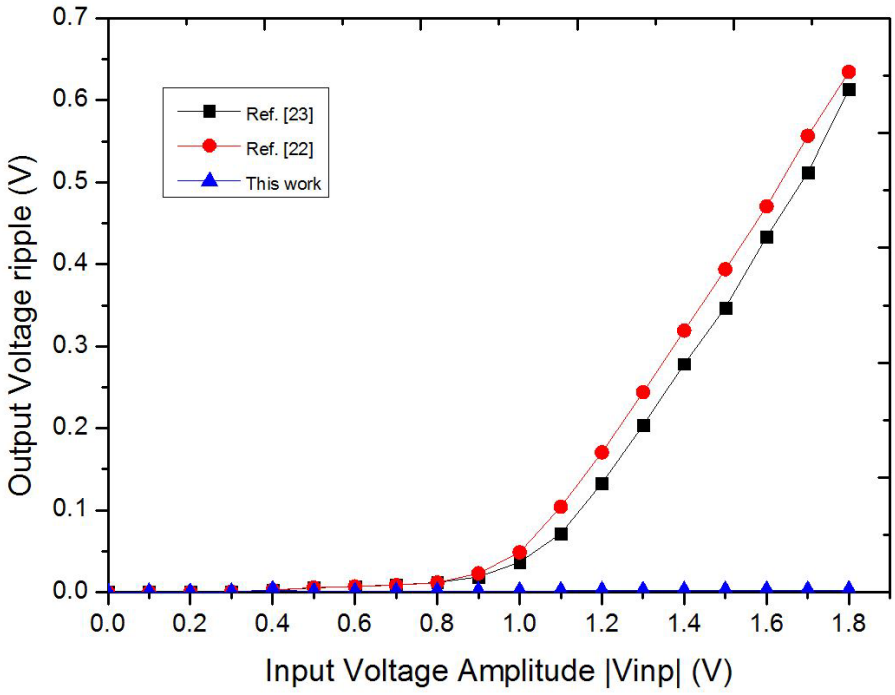


Figure 3.25: Output voltage ripple comparison with previous published papers.

In Fig. 3.21, the input voltage amplitude range is from 0 V to 1.8 V. When the input voltage amplitude is smaller than 0.7 V, the voltage conversion efficiency of all three rectifiers are even the same. With the amplitude increasing, voltage conversion efficiency of the rectifiers in [24], [25] decreased dramatically. The phenomenon also can be found through the Fig. 3.22. This is because reverse current is induced from the output to the bulk input terminal of the comparators in [24], [25] when the voltage amplitude is large enough to turn on the body-source pn junction, which results in large output voltage ripple. Thus, both the voltage conversion efficiency and power efficiency will be influenced and decreased dramatically.

3.5 Summary

In this chapter, a wide input amplitude range and highly efficient for vibration energy harvesting system is proposed. The proposed rectifier is well suitable for an input amplitude

of 0.45 V and can work at a wide range of input voltage amplitudes of 0.45 V up to 1.8 V under a standard 0.18 μm CMOS process. High breakdown voltage process can be used to enlarge the maximum input voltage amplitude to meet the requirement of different kinds of vibration energy harvesting system. By using a three-stage comparator controller, the rectifier can achieve a power efficiency of 92% and a maximum voltage conversion efficiency of 98%. Moreover, the power consumption of the rectifier is only 264.35 nW at 500 mV, which is much smaller than the best recently published results.

Chapter 4

A 1V CMOS rectifier with response compensation for wireless power transfer

4.1 Introduction

Recent years, advances in the fields of neural recording [55], cochlear implants [56], and blood flow sensing enable the development of implantable biomedical devices [57], [58], [59], [60].

A long lifetime and stable power supply to the implantable medical devices has become a bottleneck of these researches [61]. Conventional power supply method of using a battery should be avoided due to the large size and periodical replacement which cause the health risk. As compared to battery, wireless power transfer is widely researched to power the biomedical implant devices [62], [63], [64]. The power is commonly transferred through the coupled inductive coils. Figure 4.1 shows the schematic of a generic wireless power transmission system. In the first stage, power amplifier is used to generate the high frequency electromagnetic field which is needed to realize the coupling. An LC resonant structure is used as the transmitter of the system. Through the coil of the receiver, AC signal

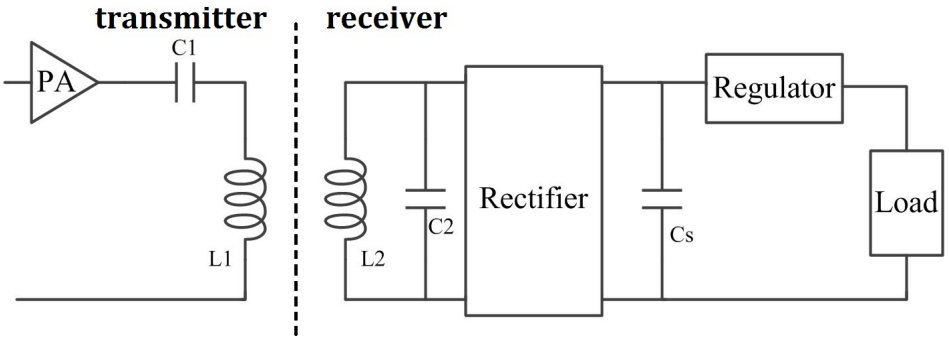


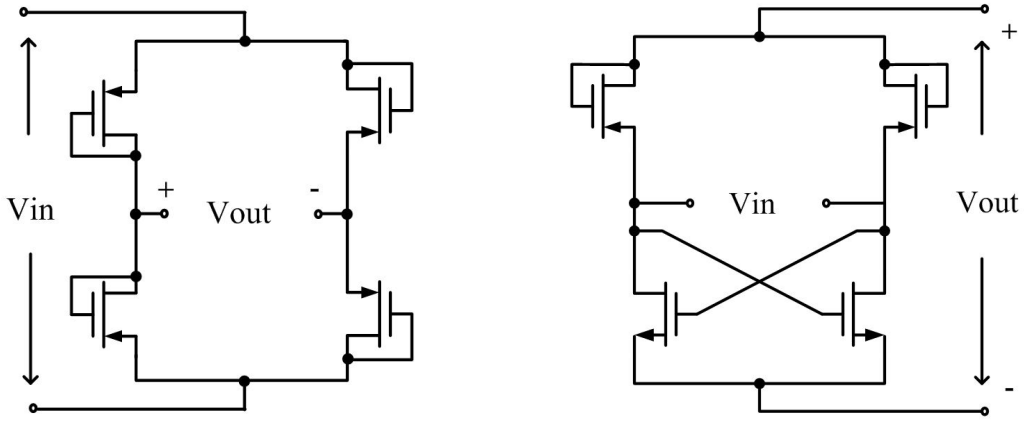
Figure 4.1: Schematic of wireless power transmission system.

is firstly rectified and then regulated to power the load system. The efficiency of the power transmission system should be maximized. The whole power efficiency of transmission system is given in Eq. 4.1

$$\eta_{total} = \eta_{PA} \times \eta_{link} \times \eta_{rec} \times \eta_{reg}, \tag{4.1}$$

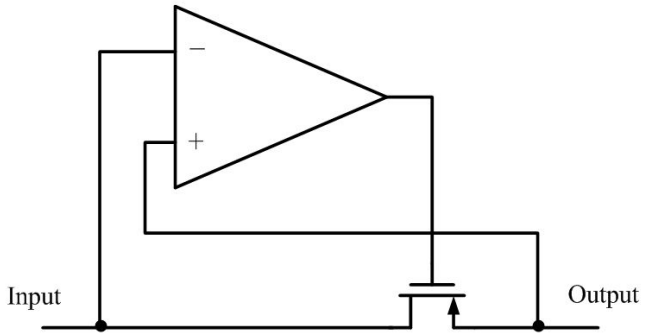
where η_{PA} is the power efficiency of power amplifier, η_{link} is the efficiency of inductive coil, η_{rec} is the efficiency of rectifier and η_{reg} is the efficiency of the regulator. It is important to mention that the efficiency of the rectifier is usually the bottleneck, and the influence from the coupling coefficient and relative distance between the coils decides that a more efficient rectifier is needed to deliver a given amount of power for a lower voltage induced across the coils of the link [65]. In addition, the operation frequency of the system should also be relatively high considering if it is utilized in the biomedical implant devices, because the low frequency will result in a larger size of the coil in the receiver, which is implanted in human body. However, it should also not be too high for avoiding the potential hazards to human safety.

Based on the above consideration, we proposed a high efficiency CMOS rectifier for 13.56 MHz in the readily available ISM (Industrial Scientific Medical) band. The rectifier can work with a low input voltage amplitude of 1 V. In addition, high efficiency can be achieved by using a novel active diode controlled by a cross-coupled comparator and switch off response compensation technology.



(a) diode connected rectifier

(b) cross-couple structure



(c) Active diode

Figure 4.2: Conventional rectifier circuits. (a) full-wave diode connected rectifier, (b) diode connected rectifier with cross-couple structure, (c) active diode.

This chapter is organized as follows. In section 4.2, the conventional CMOS rectifier topologies are addressed. Section 4.3 describes the structure and operation of the proposed rectifier in details. Simulation results, discussions and comparison are given in section 4.4, followed by the summaries in section 4.5.

4.2 Rectifier topologies

Among several choices for the rectifier in previous publications, full-wave diode rectifier is well-known for its simple structure, which is shown in Fig. 4.2a. Both schottky diode

and diode-connected CMOS transistors can be used in this structure. The performance of these integrated passive rectifiers is less frequency dependent and can be used in some far field applications. However, the voltage and power efficiency are commonly not sufficient because of the two diodes forward voltage drop. In Fig. 4.2b, the circuit uses a cross coupled PMOS structure to replace two semiconductor diodes of the diode-bridge structure. Input AC source is directly connected to the gate terminals to drive the PMOS transistors [21]. Comparing with the previous one, the forward voltage drop is reduced to only one V_{th} (threshold voltage of MOS transistor).

For further increasing the peak voltage conversion efficiency and power efficiency, active diodes for energy harvesting system[24], [25], [66] and wireless power transfer [26], [27], [29] are used instead of the diode configured transistors in the conventional rectifiers. The active diode shown in Fig. 4.2c is composed of a comparator controlled switch working nearly as an ideal diode without voltage drop. When input voltage is larger than the output voltage, the comparator will turn on the switch to charge the load. When input voltage is smaller than the output voltage, the switch will be turned off to block the reverse current from output terminal to input terminal. Higher voltage conversion efficiency and power efficiency can be achieved by replacing the passive diode with active diode. In addition, the minimum input voltage amplitudes are also reduced to under 1 V for the application of vibration energy harvesting [24], [25].

However, the performance of these active rectifiers is much frequency dependent. Most of them are working below the frequency of 10 kHz, which is only suitable for energy harvesting. In the wireless power transfer system, the operation frequency is very important to the overall system efficiency. Commonly, the size of inductive coils is limited by the system size. Thus, low operation frequency with small size coil will reduce the total power efficiency of the transfer system. For high frequency case, threshold cancellation technologies are commonly used to compensate the passive rectifiers. The idea is to feature a static bias voltage applied between gate and drain terminals of the diode-connected transistor. Comparing with active diodes, passive rectifier with V_{th} cancellation is less frequency dependent. High voltage conversion efficiency can be achieved by reducing the

voltage drop. In [30], [67] and [68], the V_{th} cancellation technologies have been proposed and modified. However, the utilization of capacitor increases the chip area and all these circuits are mainly investigated for improving the voltage conversion efficiency and no design strategy has been discussed in terms of reverse current which is first considered in [26]. Thus, the reverse current is commonly very large in these rectifiers which results in poor power efficiency, especially for low input voltage amplitude. The total efficiency of the wireless power transfer system is also restrained by this poor performance. Though active rectifier is rarely used in higher frequency case, especially in UHF applications, there are still some researches of the active rectifier. The rectifier proposed in [61] uses the concept of active diode and is designed for 13.56 MHz. Two common gate structure comparators are connected with each other to improve the operation gain. However, the time delay and reverse current still exist and result in a poor efficiency.

In order to overcome the above drawbacks, we present a novel 1 V rectifier which can work well at high frequency range in this chapter. By using a novel active diode controlled by a cross-coupled comparator with a switch off response compensation technique, the reverse current is strongly reduced and the voltage conversion efficiency and power efficiency are enhanced which features the wireless power transfer.

4.3 Circuit implementation and design considerations

4.3.1 Operation principle

Figure 4.3 shows the conceptual schematic of the new full-wave proposed rectifier. It is composed of two proposed active diodes and two cross-coupled NMOS transistors. The active diode employs a pair of source input cross-coupled comparators to control the gate voltage of switch transistors M_{P1} and M_{P2}. Each comparator is composed of two three-input comparators by cross-coupled connection. A switch off response time compensation technique is used in the two comparators to restrain the reverse current. Ideally, the input voltage V_{ac} ($V_{ac} = V_{ac+} - V_{ac-}$) generated from the LC circuit is a sinusoidal waveform.

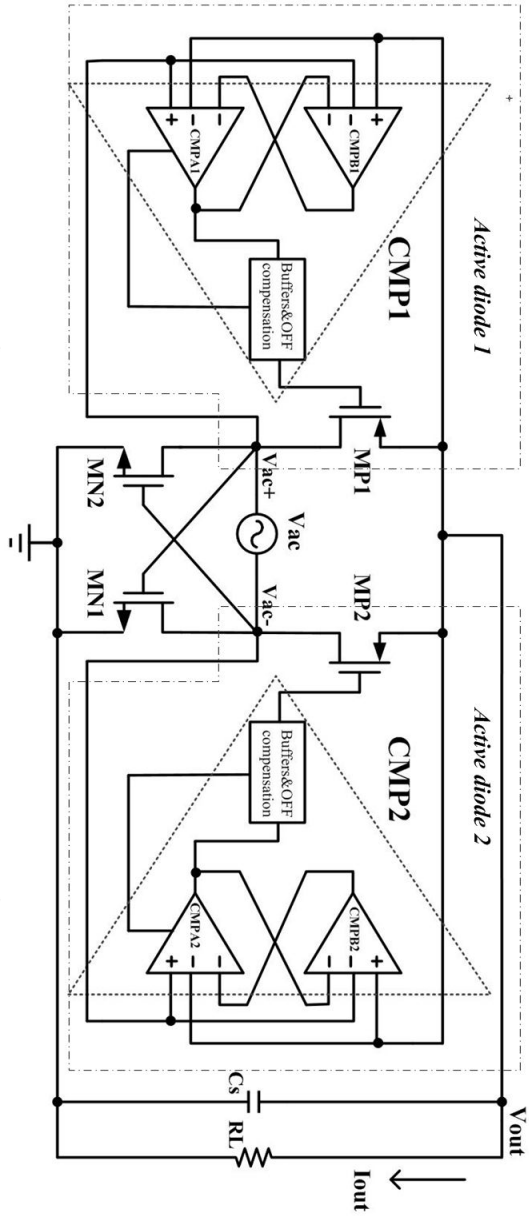


Figure 4.3: Conceptual schematic of proposed rectifier circuit.

Thus, the conductive branches M_{P1}-M_{N1} and M_{P2}-M_{N2} turn on alternatively according to the polarity of V_{ac}.

In positive period of the input source ($V_{ac} > 0$), when $V_{ac} > V_{thn}$ (threshold voltage of NMOS), the cross-coupled NMOS transistor M_{N1} turns on and connects V_{ac-} to the ground potential. The output of comparator CMP_1 remains high as long as $V_{ac+} < V_{out}$. Thus, M_{P1} is always off to avoid the reverse current from V_{out} to V_{ac+}. When $V_{ac+} > V_{out}$, the output voltage of comparator CMP_1 goes down and turns on the switch M_{P1}. The current will flow from the input terminal to the load (R_L and C_s) to charge the load capacitor. In the negative cycle ($V_{ac} < 0$), M_{P2}, M_{N2} and CMP_2 operate similarly with the M_{P1}, M_{N1} and CMP_1 in the positive cycle. M_{N2} is turned on to connect V_{ac+} to the ground when $|V_{ac}| > V_{thn}$, and CMP2 turns on M_{P2} when $|V_{ac-}| > V_{out}$. Then, M_{P2} and M_{N2} compose a conductive branch to charge the load capacitor and resistor.

In each conductive branch, there are one PMOS transistor and one NMOS transistor. Thus, the output voltage can be expressed as

$$V_{out} = |V_{ac}|_{peak} - \left|V_{dsp}\right| - V_{dsn}, \tag{4.2}$$

where $|V_{ac}|_{peak}$ is the peak amplitude of V_{ac}, $\left|V_{dsp}\right|$ is the drain-source voltage of PMOS transistors, and V_{dsn} is the drain-source voltage of NMOS transistors. As both the two transistors work in the linear region, thus the $\left|V_{dsp}\right|$ and V_{dsn} can be easily minimized by increasing the size of PMOS and NMOS power transistors. However, we should note that even though larger size transistor decreases the voltage drop, it increases the switching power loss and the comparator delays due to the larger gate capacitance. Thus, the transistors' size should be traded-off for both voltage conversion efficiency and power efficiency. In our design, it is chosen as W/L=1000/0.18 μm.

The body terminals of M_{N1} and M_{N2} are connected to the ground. Instead of utilizing the auxiliary PMOS transistors [10], the body terminals of M_{P1} and M_{P2} are directly connected to the node of V_{out}. In the steady state, the voltage amplitude of V_{out} is close to the peak voltage of V_{ac}, which is the highest potential. In the start-up state, the initial value of V_{out}

is equal to 0 V and the body-source parasitic diode is turned on when $|V_{ac}|$ is large enough. Thus, the current can still flow into the load capacitor even the comparator cannot work. Therefore, the rectifier can work well without any start-up circuit. When the rectifier enters into the steady state, the parasitic diode is turned off and no leakage current occurs.

4.3.2 Active diode design

The active diode is a switch transistor controlled by a comparator. It works nearly as an ideal diode without reverse current and voltage drop. Considering active diode1 in Fig. 4.3, when $V_{ac+}>V_{out}$, the switch transistor M_{P1} should be turned on by the CMP_1 and turned off when $V_{ac+}<V_{out}$ to avoid the reverse current from V_{out} to V_{ac+}. Because there is no external supply voltage source, the V_{ac+} and V_{out} should not only be the comparison signal but also the supply voltage source. Thus, a self-biased comparator is needed. However, design of the comparator used in the proposed rectifier is challenging. Obviously, the classical design with common source differential input and current tail bias is not suitable. The differential input imposes a common mode voltage limit that disables the use of classical comparator in our proposed circuit. The tail current bias structure also introduces a trade off between response time and power efficiency. The conventional common-gate comparator can be used in this kind of design. However, for high operating frequency of 13.56 MHz, the gain is not enough and the output slew rate is not large enough to do a quick response.

In order to overcome the above drawbacks, we propose a novel high speed comparator with a switch off response compensation control circuit. As shown by the block diagram in Fig. 4.3, the CMP_1 consists of a switch off compensation block and two specially designed comparators (CMP_{A1} and CMP_{B1}) in cross-coupled connection. Figure 4.4 shows the schematic of the proposed comparator. CMP_{A1} is constructed by M_{A11}, M_{A12}, M_{A13} and M_{A23}. CMP_{B1} consists of M_{B11}, M_{B12}, M_{B13} and M_{B23}. Current mirrors of M_{C11}, M_{C12} and M_{C13} are used to supply bias currents to CMP_{A1} and CMP_{B1}. Source terminal of transistors M_{A11}, M_{A12}, M_{B11} and M_{B12} are used as inputs of the comparators to solve the problem of common mode voltage limit. Node voltages of V_{OA} and V_{OB} are the outputs of CMP_{A1}

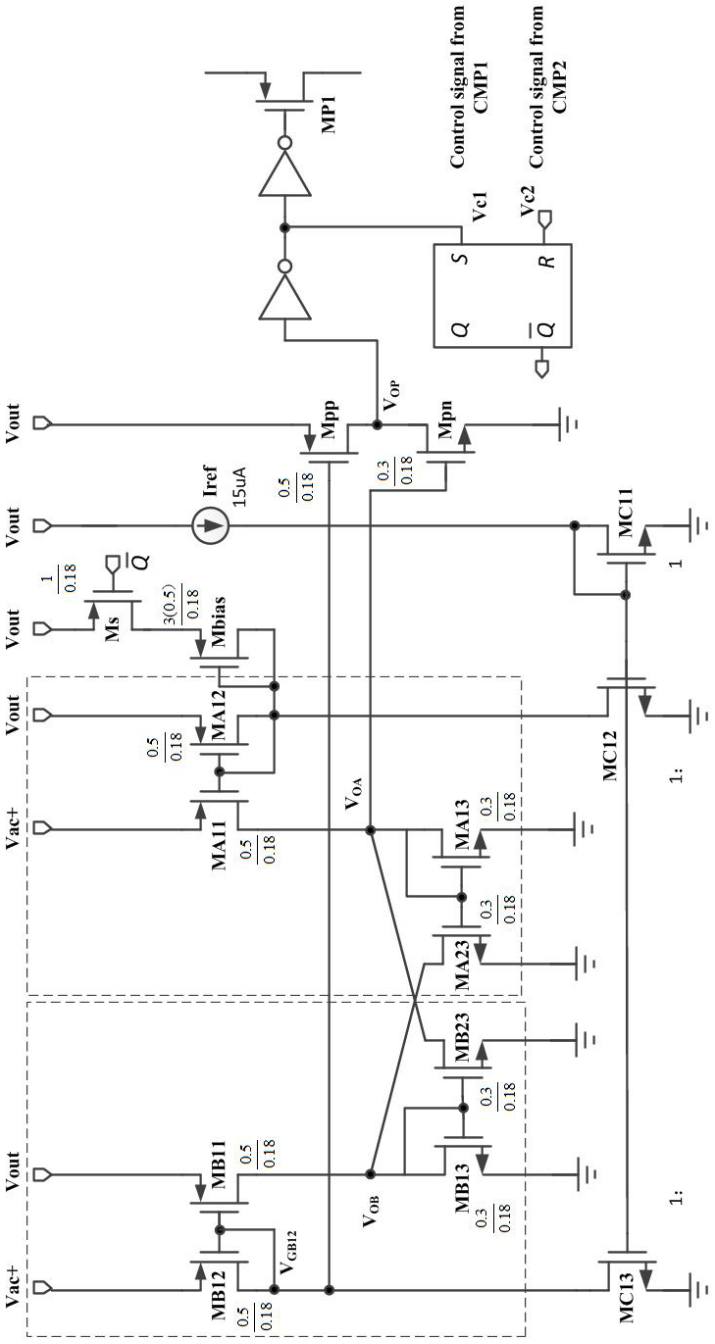


Figure 4.4: Circuit implementation of the comparator CMP_1.

and CMP_{B1}, respectively. Set V_{ac+}=V_{out} as the initial point, when V_{ac+} increases, the drain current of M_{A11} is much larger than the current through M_{A12}, which is supplied by M_{C12}. This drives the voltage potential of V_{OA} to increase. Considering CMP_{B1}, the gate voltage potential of M_{B12} increases as well as V_{ac+}. Thus, V_{OB} decreases when V_{ac+}>V_{out}. However, the gain of CMP_{A1} or CMP_{B1} is not large enough to do a quick response. To enable the high gain and large slew rate, the positive feedback transistors M_{B23} and M_{A23} are added to construct a cross-coupled structure [69], [70]. The size ratio between M_{B13}, M_{A13} and M_{B23}, M_{A23} decides the performance. As long as the K_{23} (W/L ratio) of M_{B23} and M_{A23} is less than K_{13} of M_{B13} and M_{A13}, the positive feedback factor is less than the negative feedback factor. Then the overall feedback will be negative and no hysteresis exists in the transfer function. When K_{23} is larger than K_{13}, the positive feedback factor becomes greater and the overall feedback will be positive, which results in infinity gain and a hysteresis in the transfer curve. However, hysteresis delay will result in large reverse current which reduced the efficiency of the rectifier, since the switch transistor cannot turn on and turn off on time. Thus, the value of K_{23}/K_{13} should be equal to 1, which means that there is no hysteresis and infinity gain can also be achieved.

Though no hysteresis and high gain meet the requirement of active diode, the voltage swing of the V_{OA} is constrained by the diode-connected transistor M_{A13}. Thus, M_{pn} and M_{pp} are added to solve the problem. V_{OA} and V_{GB12} are connected to the gate of M_{pn} and M_{pp} respectively. When V_{ac+} increases, V_{GB12} and V_{OA} change in the same direction. This makes the M_{pn} and M_{pp} work as a push-pull output stage and wide swing output can be achieved. In order to verify the infinity gain and hysteresis value of the proposed comparator, DC simulation in Fig. 4.5 has been done to prove our idea. Node voltage of V_{ac+} increases from 0 V to 3.5 V and decreases from 3.5 V to 0 V again, where V_{out} is constant. From Fig. 4.5, it can be found that by setting K_{23}=K_{13}, infinity gain can be achieved without any hysteresis and the V_{OP} can change in the full voltage range from 0 to V_{out}. Considering the large size switch transistor, a two stage buffer is connected to the output node V_{OP} to improve the current driving ability.

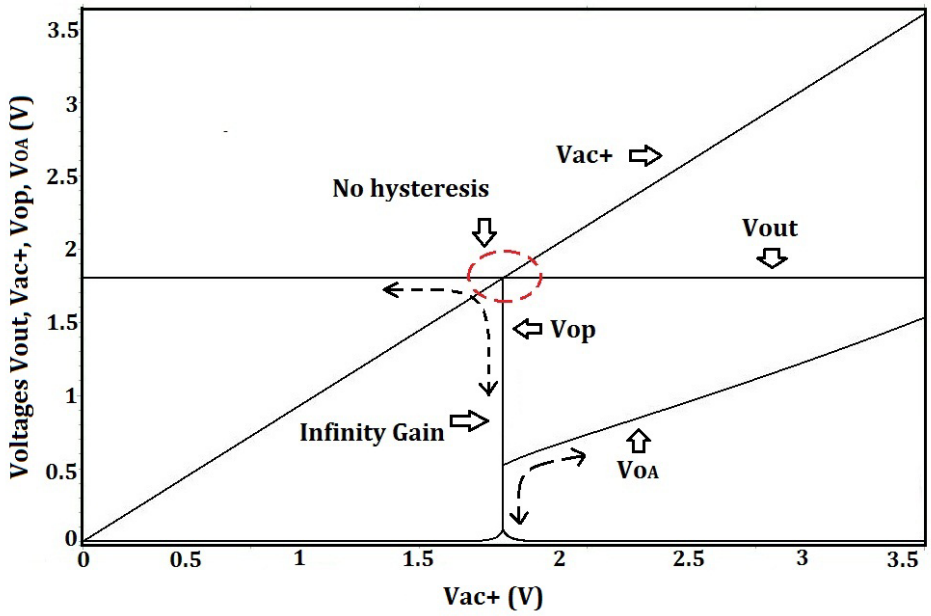


Figure 4.5: Gain and hysteresis verification of the proposed cross-coupled comparator by DC simulation.

As shown in Fig. 4.5, in each branch of the source-input stage, there is a pair of NMOS and PMOS transistors. Thus, the minimum operation voltage of the proposed comparator is decided by the supply voltage of each branch and can be expressed as

$$V_{cmp,min} = max(|V_{thn}|, |V_{thp}|) + 2V_{ov}, \tag{4.3}$$

where $|V_{thp}|$ and $|V_{thn}|$ are threshold voltages of PMOS and NMOS transistors, respectively. Since the comparator is powered by the output voltage V_{out}, the minimum value of V_{out} should be equal to $V_{cmp,min}$. This can be given as

$$V_{out,min} = V_{cmp,min}. \tag{4.4}$$

4.3.3 Reverse current consideration and current reference design

Reverse current will occur and flow from V_{out} to V_{ac+} if M_{P1} is not turned off when V_{out}>V_{ac+}. Though the proposed active diode structure has a high gain and no hysteresis,

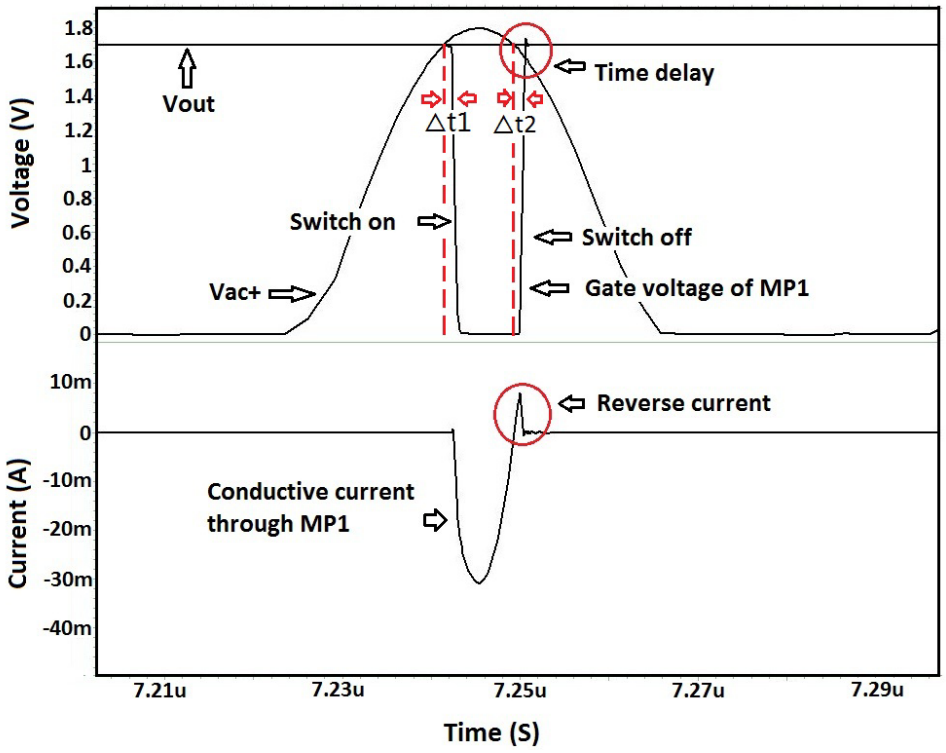


Figure 4.6: Waveform of signals from the proposed CMP_1 without any compensation.

there is still time delay caused by the large size switch transistor and invertor buffers. Figure 4.6 shows the simulation results without any compensation. Ideally, the gate voltage of M_{P1} should change as the dot line. However, time delays of $\triangle t1$ and $\triangle t2$ exist between the ideal and actual case. Thus, reverse current occurs in the period of $\triangle t2$ because the switch transistor M_{P1} is still on even V_{out}>V_{ac+}. Conventional method is to use unbalanced transistors to compensate the switch off delay ($\triangle t2$) [29]. However, this will increase the switch on delay ($\triangle t1$) simultaneously and reduce the effective conduction time. Therefor, a switch off delay compensation circuit is needed to reduce the $\triangle t2$ without any influence to the $\triangle t1$.

A SR latch of NOR Gate version is added in each comparator. The S terminal is connected to control signal from CMP_1 (the output of the first invertor buffer). The R terminal is connected to the control signal from CMP_2 (the output of the first invertor buffer in CMP_2). A bias circuit (M_{bias} and M_s) is in parallel with M_{A12}. M_s works as

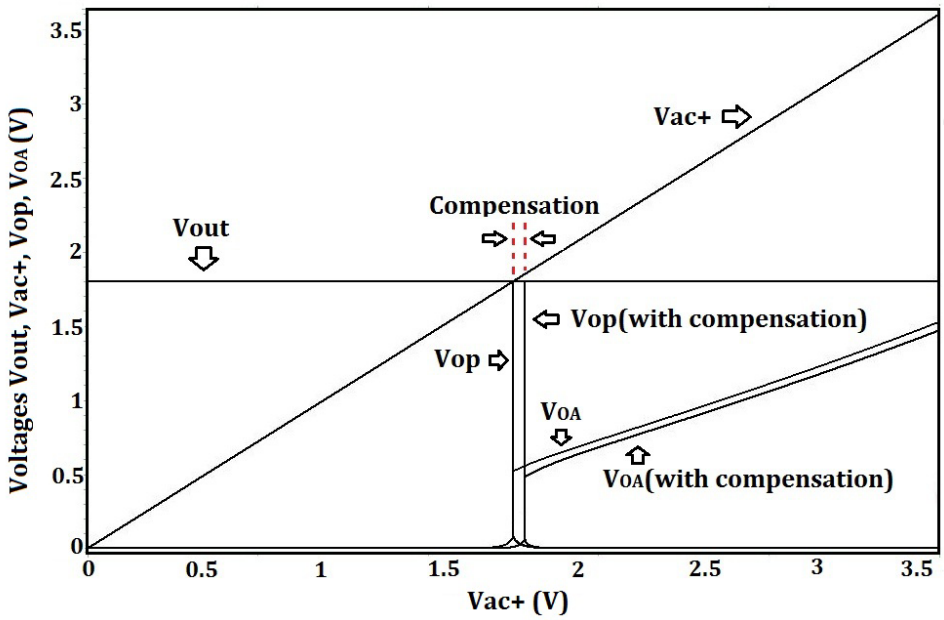


Figure 4.7: Comparator response with/without compensation by DC simulation when V_{ac+} decreases from 3.5 V to 0 V.

a switch which is controlled by the output of the SR latch. M_{bias} is diode connected with the same gate of M_{A12}. When $V_{ac+}>V_{out}$, the switch M_{P1} is turned on after a time delay of $\triangle t1$ and the voltage of V_{c1} is in high potential. At the same time, switch M_{P2} is off and V_{c2} from CMP_2 is still in low potential. Therefore, the output Q of SR latch is low and the control switch M_s turns on to sink current from V_{out}. This makes V_{OA} go down and the gate voltage of M_{P1} increase earlier before $V_{ac+}<V_{out}$ when V_{ac+} decreases from 3.5 V to 0 V , which can be found in Fig. 4.7. Thus, the compensation block creates an offset value to compensate the switch off delay of $\triangle t2$. Table 1 shows the output of SR latch according to different states. It is obvious that the bias circuit only works after M_{P1} is turned on. The compensation function is hold until M_{P2} is turned on. After that, M_s is turned off and no current flows though the auxiliary bias transistor M_{bias}. Therefore, the compensation to $\triangle t2$ has no influence to $\triangle t1$, and both the effective conduction time and switch off delay compensation can be achieved.

Besides the comparator, the current reference used to bias the comparators is also important. The current reference is powered by the load capacitor C_s. In the start-up state

Table 4.1: Output of SR latch with different M_{P1} and M_{P2} state.

	M_{P1}	M_{P2}	$\overline{Q}$
State	ON	OFF	Low
State	OFF	OFF	Low
State	OFF	ON	High
State	OFF	OFF	High

of the rectifier, the initial value of V_{out} is 0 V. The input source V_{ac} charges the C_s through the parasitic diodes of the power PMOS switches. After the load capacitor is charged up to higher than the minimum supply voltage required by the comparator and the current reference, the rectifier could then function as designed. Therefore, it should not only supply a bias current to the comparator, but also can work with a low supply voltage. In addition, the power consumption of the current reference should also be small considering the power efficiency of the rectifier. Figure 4.8 shows the schematic of the designed current reference based on the peaking current source [71]. M_7, M_8 and R_2 constitute the peaking current source, while the transistors M_5, M_6, connected in a current mirror serve as a self-biasing part. The transistors M_7 and M_8 are designed to work in the sub-threshold region. When the peaking condition is satisfied, we can obtain the reference bias current as

$$I_{ref} = \frac{nV_T}{R_2}. \tag{4.5}$$

The simulation results show that the current reference output a stable bias current with a minimum supply voltage of 0.8 V.

4.4 Simulation results and considerations

The aspects of the rectifier are the novel structure and switch off response compensation technique, output voltage conversion efficiency and power efficiency, which will be discussed respectively.

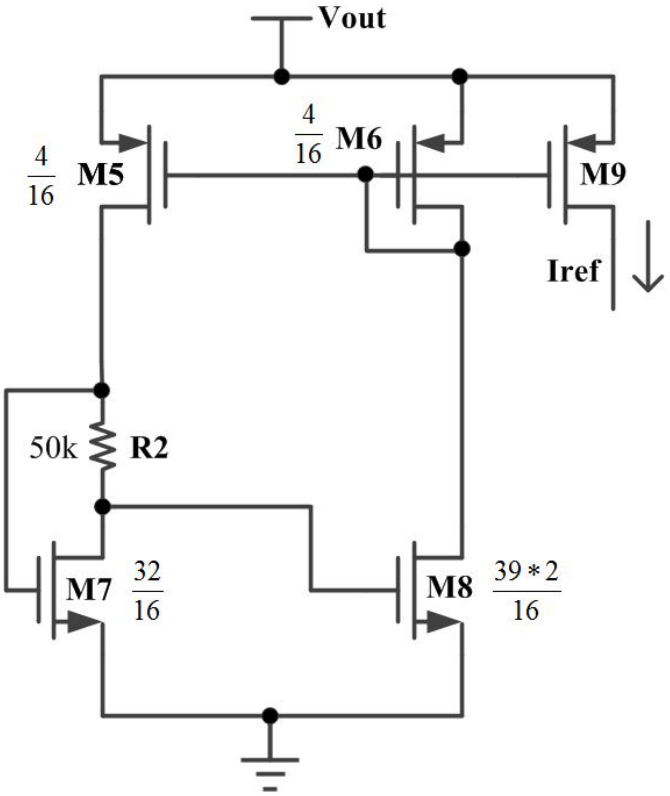


Figure 4.8: Schematic of the bias current reference.

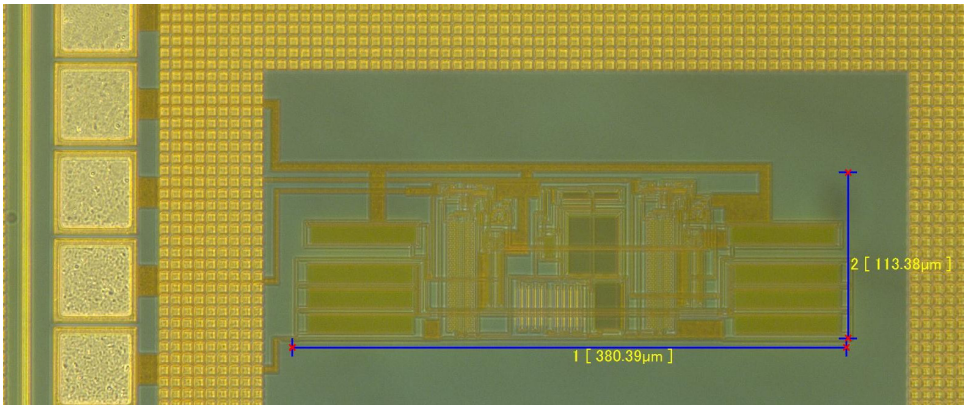


Figure 4.9: Chip micrograph of the proposed rectifier.

The circuit has been verified by standard 0.18 μm CMOS process. A pure 13.56 MHz sinusoidal waveform is applied to the input of the rectifier. R_L varies from 100 Ω to 10 kΩ and C_s is 100 nF. Figure 4.9 shows the micrograph of the proposed rectifier, the total chip area is only 0.043 mm^2. The test circuit for chip measurement is same with the circuit in chapter 2. Coils ratio is 1:1 with 4 turns in this design. The inductance of the coil at 5 MHz is 745 nH.

4.4.1 Switch off delay compensation and minimum operation voltage

In order to avoid the reverse current and maximize the effective conduction time, a novel active diode and switch off response compensation method are described in section 4.3. By utilizing the cross-coupled structure and reverse current control block, high voltage conversion efficiency and power efficiency are achieved. The simulated waveform of proposed novel rectifier with switch off delay compensation is shown in Fig. 4.10. It indicates that the switch off delay has been reduced a lot without any influence to the switch on response comparing with Fig. 4.6. There is even no reverse current and the conduction time has been maximized. Thus, the high conversion efficiency can be achieved.

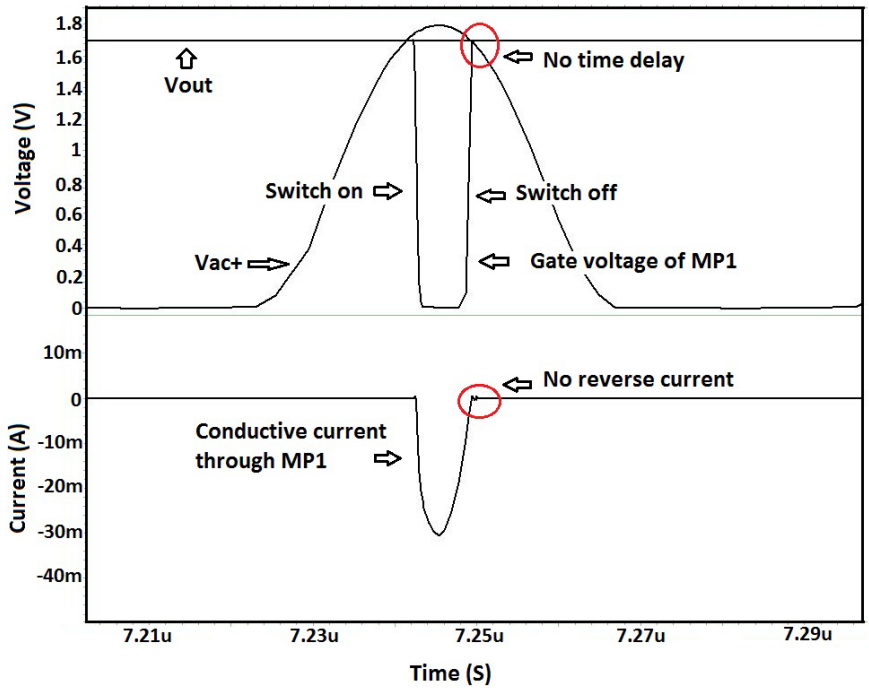


Figure 4.10: Waveform of signals from the proposed CMP_1 with switch off delay compensation.

4.4.2 Voltage conversion efficiency and power efficiency

The proposed rectifier can work at a range of input peak voltage amplitudes of 1 V up to 1.8 V, where the maximum value is decided by the breakdown voltage of the standard 0.18 μm CMOS process. This value can be easily enlarged by implementing higher breakdown voltage process. The minimum input voltage amplitude is decided by V_{out}. The reason is that the comparator is powered by the output voltage of this rectifier. We have analyze and prove the comparator's minimum operation voltage, which is shown in Eq. 4.3. Considering Eq. 4.2, Eq. 4.3 and Eq. 4.4, the lowest input peak voltage amplitude can be expressed as

$$\begin{aligned} |V_{ac}|_{peak,min} = max(|V_{thn}|, |V_{thp}|)+ \\ 2V_{ov} + |V_{dsp}| + V_{dsn}. \end{aligned} \tag{4.6}$$

Suppose max($|V_{thn}|$,$|V_{thp}|$)=0.55 V, V_{ov}=0.15 V and $|V_{dsp}|$+V_{dsn}=0.1 V, the lowest input peak voltage amplitudes is about 0.95 V. Thus, 1 V is enough for the operation of the

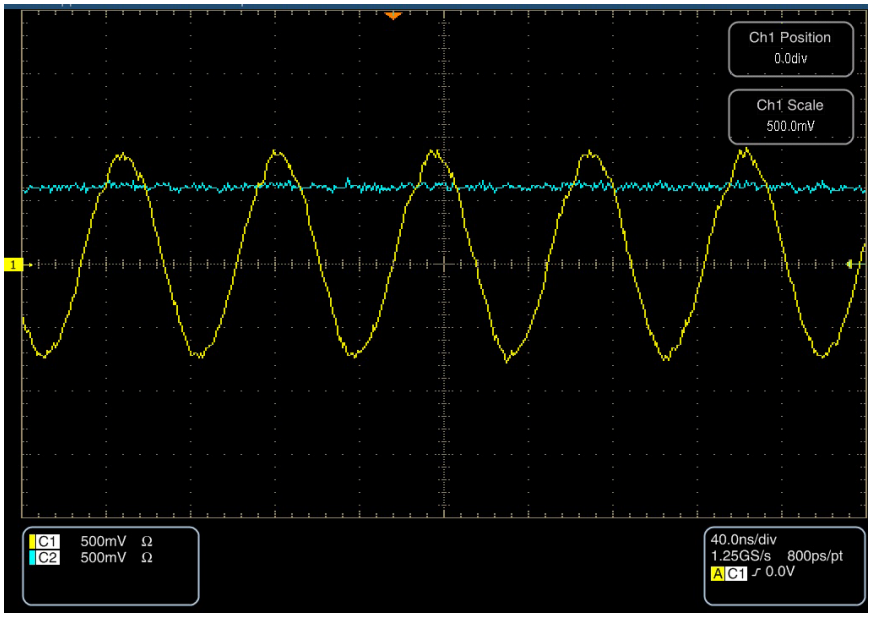


Figure 4.11: Measurement output voltage with an input voltage amplitude of 0.9 V.

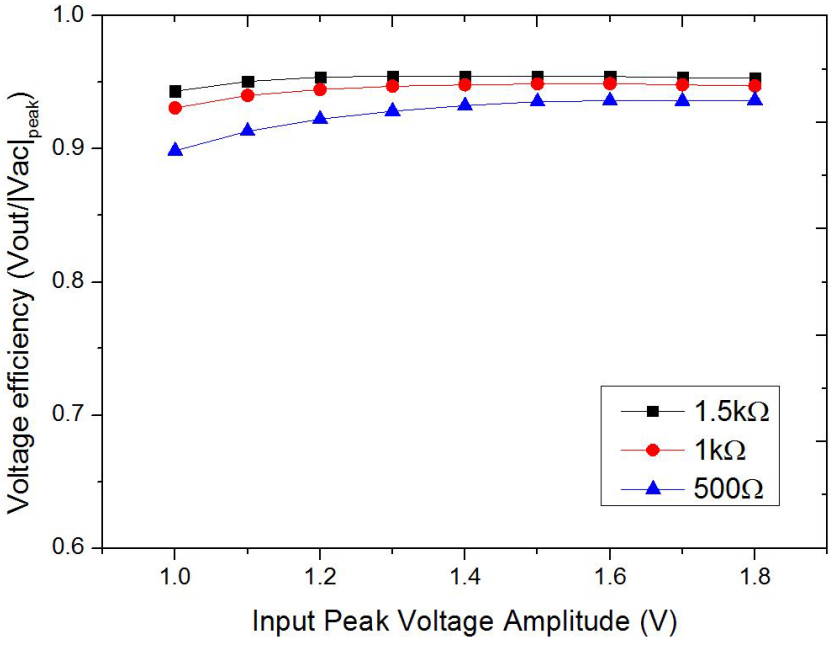


Figure 4.12: Simulated voltage conversion efficiency versus different input voltage amplitudes.

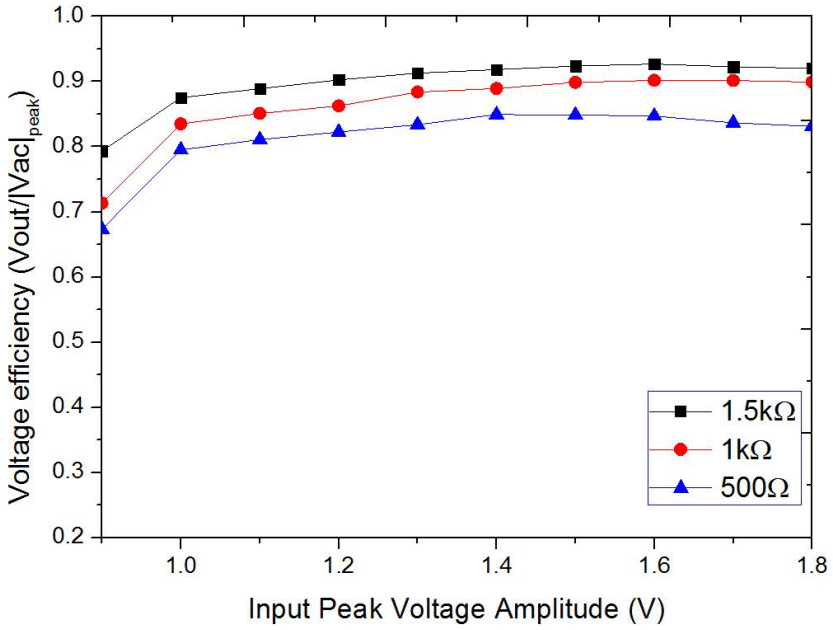


Figure 4.13: Measured voltage conversion efficiency versus different input voltage amplitudes.

proposed rectifier. Figure 4.11 shows that the proposed rectifier can work even with an input voltage amplitude of 0.9 V.

The voltage conversion efficiency η_v is calculated by the fraction of output voltage V_{out} and the peak voltage amplitude of input $|V_{ac}|_{peak}$, which is shown in Eq. 4.7.

$$\eta_v = \frac{V_{out}}{|V_{ac}|_{peak}}. \tag{4.7}$$

Figure 4.12 shows the simulated peak voltage conversion efficiency verse different load values and amplitudes. The average conversion rate is about 93% and the efficiency can reach a maximum value of 96% with a 1.5 kΩ load. The measurement results are given in Fig. 4.13. Though the performance of the measurement is not as good as the simulation, the average of the voltage conversion efficiency is still close to 90%. Note that the output voltage conversion efficiency is higher with larger load resistors, which is easy to be understood as the work principle of resistance divider.

The power efficiency of the rectifier is calculated using

$$\eta_p = \frac{\int_{t_1}^{t_1+T} v_{out}(t)\cdot i_{out}(t)dt}{\int_{t_1}^{t_1+T} v_{in}(t)\cdot i_{in}(t)dt}, \tag{4.8}$$

where T is one period of the input signal and t_1 is the start time. Figure 4.14 and Fig. 4.15 show the simulated and measured power efficiency versus different input voltage amplitudes under three types load condition. The maximum simulated power efficiency is about 90% and can achieve at least 80% under different input peak voltage amplitudes. The measured results are a little poor than the simulation and the maximum efficiency is about 87%. The power efficiency is much better when the load value is smaller. The static power consumption of the rectifier is also tested. In order to compare with previous published papers, Figure 4.16 shows the power consumption composition of the rectifier under a 1 V input peak voltage amplitude condition. It can be seen that 86.1% of the input power has been delivered to the output load. The majority of the power consumption comes from the comparator controlled switch transistors M_{P1} and M_{P2} (8.79%), followed by the comparators (CMP_1 and CMP_2). Power consumption in CMP_1 and CMP_2 include the internal power dissipation of the cross-coupled comparators as well as the switch off delay compensation block. The transistors M_{N1} and M_{N2} also consume 0.47% of input power due to their internal resistance. The results show that the power consumption at 1 V is only 0.259 mW which is much smaller than the best recently published results. Besides the self-power consumption, the rectifier can supply a 5.74 mW output power with a 1.8 V input and 500 Ω load.

Figure 4.17 shows the power efficiency and voltage conversion efficiency verse R_L with a 1.8 V peak voltage amplitude input. As R_L increases, the voltage conversion efficiency also increases because of the higher output voltage. The rectifier can achieved a voltage efficiency of 85% even with a 100 Ω heavy load. In Fig. 4.17, the maximum power efficiency was achieved with R_L=500 Ω. When R_L increases above 500 Ω, I_{RL} drops and P_{RL} for the same V_{out} decreased. Therefore, the internal power consumption of M_{P1}, M_{P2},

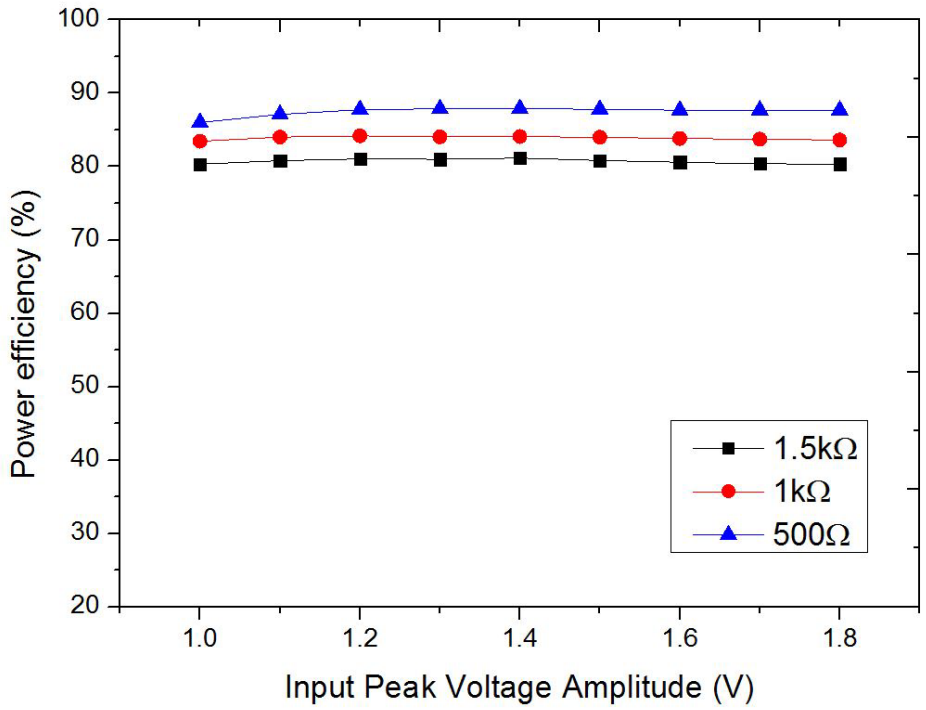


Figure 4.14: Simulated power efficiency verse different input voltage amplitudes.

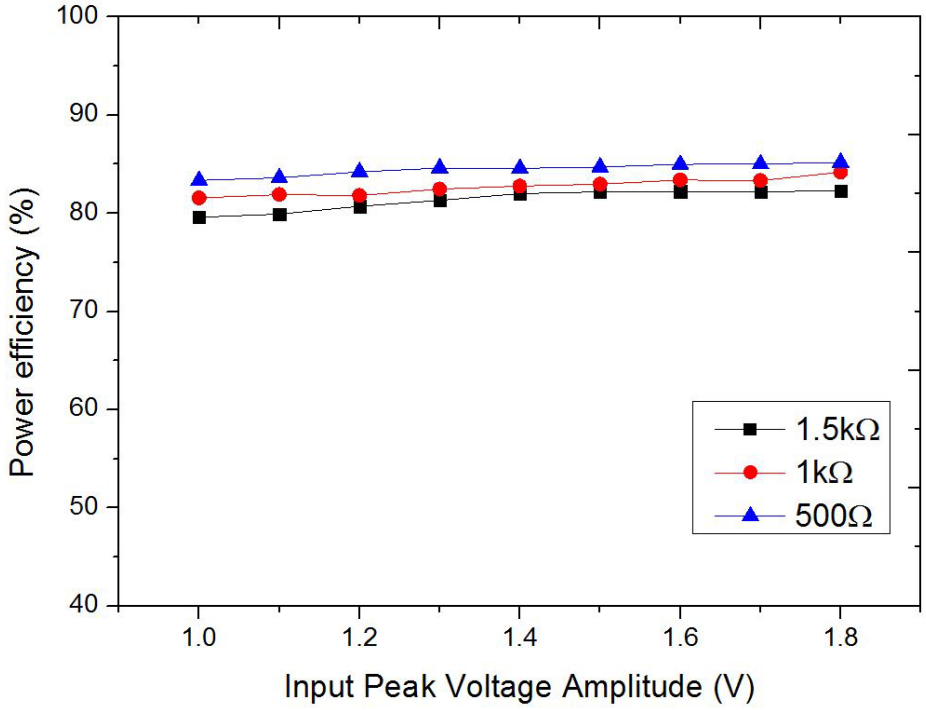


Figure 4.15: Measured power efficiency verse different input voltage amplitudes.

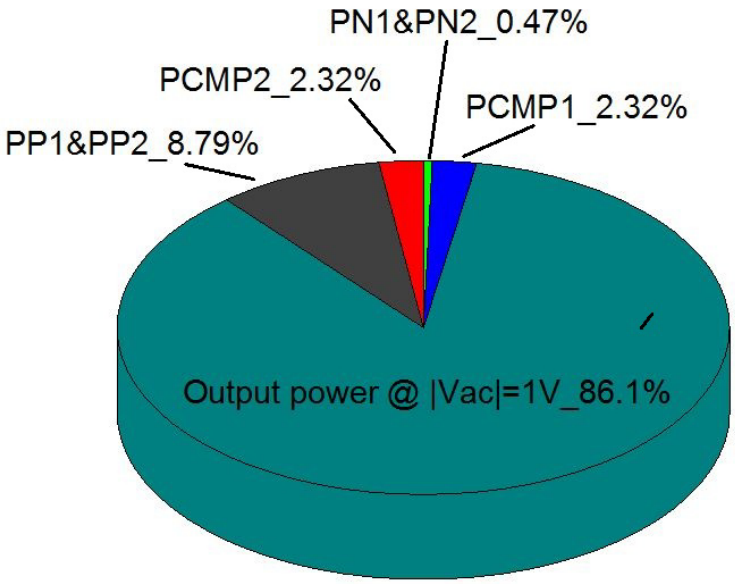


Figure 4.16: Power consumption composition of the proposed rectifier when $|V_{ac}|_{peak}$=1 V and R_L=500 Ω.

CMP_1 and CMP_2 becomes more dominant, reducing the power efficiency. On the other hand, as R_L decreased below 500 Ω, higher input current is required to drive the heavy load, increasing the power consumption of switch transistors and decreasing the amplitude of V_{out}. This results in the power efficiency to decrease.

4.4.3 Performance in different corners

Process variations are generally considered in the design of analog circuit. In order to verify the influence to our proposed circuit, the rectifier has been simulated when the process corners are the typical (TT), fast (FF) and slow (SS) of the 0.18 μm CMOS technology, respectively. Figure 4.18 and Fig. 4.19 show the voltage conversion efficiency and power efficiency under different corners. Both the fluctuation of the power efficiency and voltage efficiency and are within ±2% between different process corners which can be accepted.

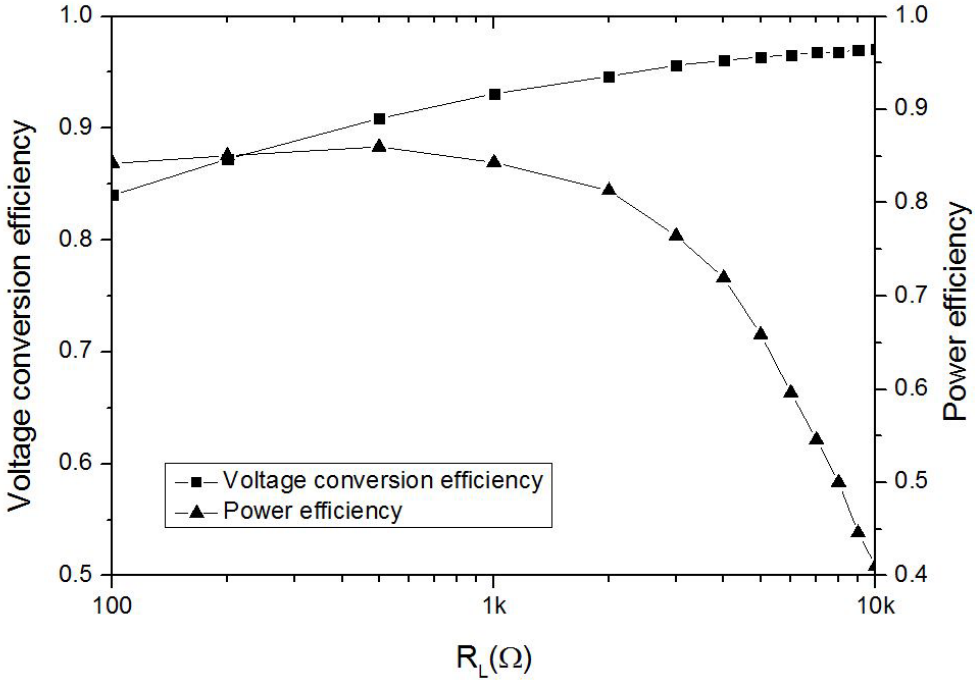


Figure 4.17: Voltage conversion efficiency and power efficiency verse R_L when $|V_{ac}|_{peak}$=1.8 V.

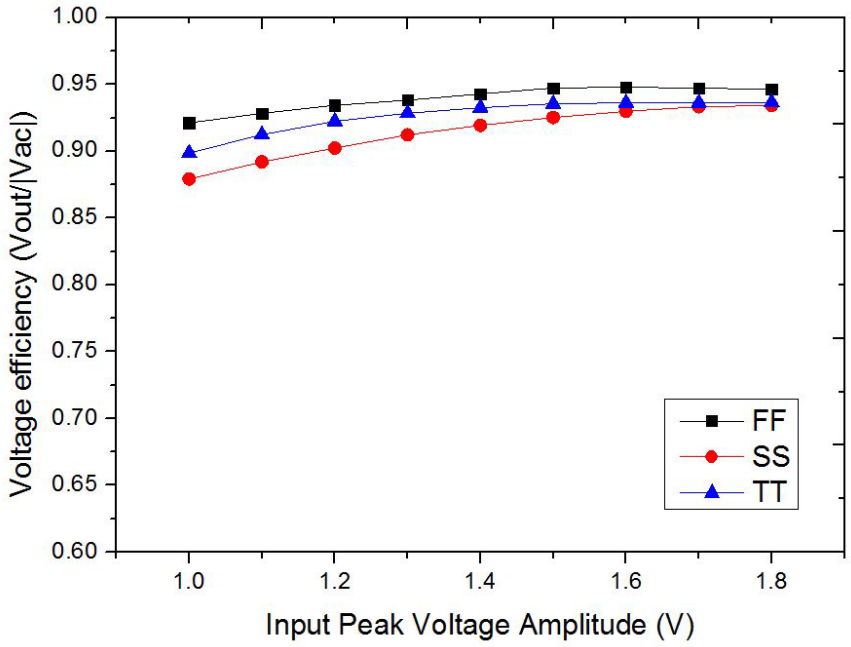


Figure 4.18: Voltage conversion efficiency verse different input voltage amplitudes under different corners with R_L=500 Ω.

Table 4.2: Performance comparisons between rectifiers.

	JSSC 2009 [27]	TCAS II 2006 [26]	TCAS II 2012 [61]	TBCAS 2012 [30]	This work
Technology	0.35 μm CMOS	0.35 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS
Frequency	1.5 MHz	13.56 MHz	13.56 MHz	13.56 MHz	13.56 MHz
Input Amplitude $\mid V_{ac} \mid$ range	1.2 V-2.4 V	1.5 V-3.5 V	0.9 V-2 V	0.8 V-2.7 V	1 V-1.8 V
V_{out}	0.98 V-2.08 V (R_L=100 Ω) 1.13 V-2.28 V (R_L=2 kΩ) (Measured)	1.2 V-3.22 V (R_L=1.8 kΩ) (Measured)	0.45 V-1.78 V (R_L=1 kΩ) (Measured)	0.3 V-2 V (R_L=2 kΩ) (Measured)	0.8 V-1.51 V (R_L=500 Ω) 0.875 V-1.66 V (R_L=1.5 kΩ) (Measured)
P_{out}(max)	43.3 mW	5.76 mW	3.2 mW	2 mW	5.74 mW
Voltage Conversion efficiency	81.7%-86.7% (R_L=100 Ω)	80%-92% (R_L=1.8 kΩ)	50%-89% (R_L=1 kΩ)	37.5%-74% (R_L=2 kΩ)	80%-83.2% (R_L=500 Ω) 87.5%-92% (R_L=1.5 kΩ)
Power efficiency	82%-87% (Simulated) (R_L=100 Ω)	68%-85% (Simulated) (R_L=1.8 kΩ)	60%-81.9% (Measured) (R_L=1 kΩ)	60%-86% (Simulated) 37%-80% (Measured) (R_L=2 kΩ)	83.3%-85.2% (Measured) (R_L=500 Ω)

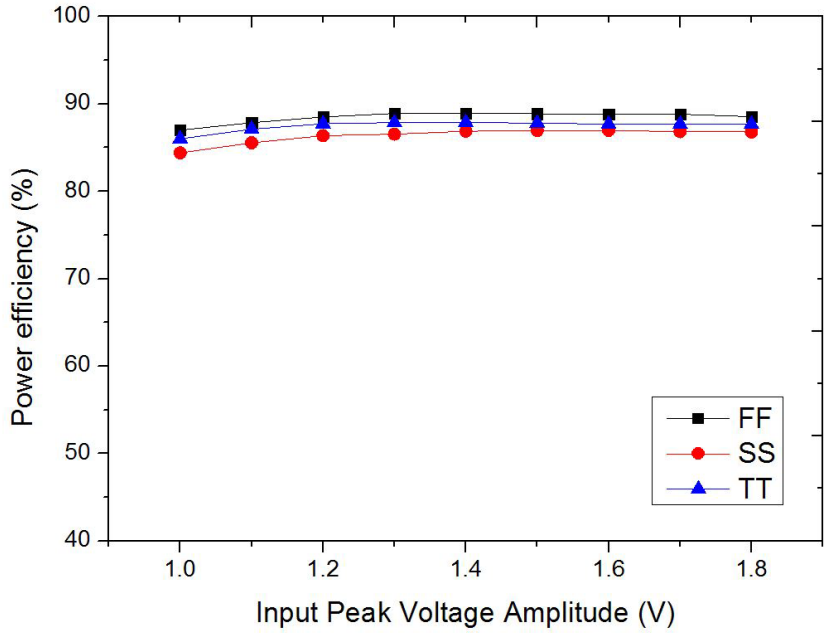


Figure 4.19: Power efficiency verse input voltage amplitudes with R_L=500 Ω.

4.4.4 Performance Comparison

The performance of our proposed rectifier is summarized and compared with previous published papers in Table 4.2. Rectifiers in [26], [30], [61] are designed for 13.56 MHz. Though the minimum operation voltage in [30] can be as low as 0.8 V by using the V_{th} cancellation technology, the voltage efficiency is only 37.5% even with a light load. The rectifier of [61] is even the same as that in [30]. Both these two designs work with poor voltage conversion efficiency and power efficiency without considering the turn on-turn off speed and reverse current. In [26], efficiency of the rectifier was improved at a cost of minimum input voltage. The rectifier in [27] has a better performance. However, it is designed for low frequency of 1.5 MHz and the structure is not suited to the ISM band of 13.56 MHz. By using a novel high speed cross-coupled comparator and switch off response compensation technique, the proposed rectifier can achieve higher voltage conversion efficiency and power efficiency even under low input voltage and heavy load condition. In addition, the minimum power consumption of the rectifier is only 0.259 mW and the output power can be as large as 5.74 mW.

4.5 Summary

A low voltage high efficiency CMOS rectifier for wireless power transmission system in biomedical implant application has been proposed. Switch conduction time is optimized and reverse current is efficiently avoided by using a novel structure comparator and switch off response time compensation technique. Comparing with previous state-of-the-art designs, our proposed rectifier achieved higher voltage and power efficiency. The rectifier can supply a output power of 5.74 mW and the power consumption can be as low as 0.259 mW, which is much smaller than the previous works.

Chapter 5

Conclusions

5.1 Conclusions

This dissertation focuses on design of high efficiency CMOS rectifier for energy harvesting and wireless power transfer systems. Three novel rectifiers with new technologies and structures are proposed based on the requirements of different applications and drawbacks of previous researches. The conclusions and future works are summarized as follows.

Chapter 1 introduced the application backgrounds and previous researches. The motivations and objectives of this dissertation were also summarized based on the drawbacks of previous designs.

Chapter 2 analyzed the drawbacks of previous reported rectifiers in the field of transcutaneous power transmission. A low voltage CMOS full-wave rectifier is proposed in this chapter. By using the novel comparator controlled switch, the proposed rectifier for battery-less devices such as biomedical implants can work with a minimum input voltage amplitude of 0.7 V, comparing with 1.2V in previous design. The proposed rectifier is verified by 0.18μm CMOS process. In combination with current offset bias circuit, the reported design dramatically reduced the voltage loss and power loss. Results show that the maximum peak voltage conversion efficiency is over 88% and power efficiency is more

than 88.5% with a input source frequency from 100 kHz to 1.5 MHz. The comparison confirms that the proposed structure has excellent improvement in kinds of indexes.

Chapter 3 proposed a low voltage and high efficiency rectifier for energy harvesting system. Without using the traditional bulk driven comparator, the proposed rectifier utilized a novel source input comparator to restrain the body reverse current when input voltage is larger than 1 V. Two stage structure in referenced reports were also modified to one stage full wave structure to reduce the voltage lose in the conductive line. The idea is verified using 0.18μm CMOS process. The results show that this structure reduced the minimum operation voltage as low as 0.45 V. The biggest improvement is that the input voltage range has been enlarges from 0.45 V to 1.8 V. This makes the proposed rectifier can be suited to different kinds of vibration power generator. Average voltage conversion efficiency and power efficiency are also improved to 96% and 92%, respectively. Simulated power efficiency of this rectifier is only 264.35 nW@500 mV input, which is 30% smaller than the best published papers.

Chapter 4 focused on the high efficiency rectifier for wireless power transmission such as the biomedical application. A 1 V, high efficiency comparator-based CMOS rectifier for wireless power transfer in biomedical applications is proposed. In this design, a novel active diode controlled by a cross-coupled comparator is designed to overcome the common voltage limit of traditional structure. An SR latch compensation circuit is added to block the reverse current and enlarge the conduction time. The proposed rectifier is verified using 0. 18μm standard CMOS process with a 13.56 MHz input source. By utilizing these new technologies, the rectifier can achieve a maximum voltage conversion efficiency of 88% and power efficiency of 85.2%. However, the power efficiency of traditional rectifier using V_{th} cancellation technology is only 37.5% with 0.8 V input voltage. Simulation power consumption of the rectifier is only 0.259 mW with 1 V peak input voltage.

5.2 Future work

With the development of low voltage, low power circuit, the requirement for a much higher performance rectifier is also growing rapidly. Though all the proposed three rectifiers have better performances comparing with previous researches, there is still room for the improvement.

For vibration energy harvesting application, control circuit of the active rectifier can work in the week inversion region which helps to reduce the minimum operation voltage as small as 0.45 V. However, the minimum voltage of most rectifiers for high frequency application, such as wireless power transmission is still larger than 1 V. This is commonly decided by the minimum start up voltage of the control circuit. Because most of the rectifiers are self-powered, small input voltage is not enough for safe start up. Thus, there are still some issues need to be solved in the research of low voltage rectifier, especially for the application of wireless power transfer.

Bibliography

[1] Morris and P. Robin, *A History of the World Semiconductor Industry*, ISBN 978-0-86341-227-1, 1990.

[2] Y. Rao and D.P. Arnold, "An Input-Powered Vibrational Energy Harvesting Interface Circuit With Zero Standby Power," *IEEE Trans. Power Electronics*, vol. 26, no. 12, pp. 3524-3533, December 2011.

[3] Y.K. Ramadass and A.P. Chandrakasan, "A batteryless thermoelectric energy-harvesting interface circuit with 35mV startup voltage," *IEEE Int. Solid-State Circuits Conf.*, pp. 486-487, Feberay 2010.

[4] X.D. Do, C.J. Jeong, H.H. Nguyen, S.K. Han and S.G. Lee, "A high efficiency piezoelectric energy harvesting system," *Proc. IEEE ISOC'2011.*, pp. 389-392, November 2011.

[5] T.J. Sun, X. Xie, G.L. Li, Y.K. Gu, Y.D. Deng and Z.H. Wang, "A Two-Hop Wireless Power Transfer System With an Efficiency-Enhanced Power Receiver for Motion-Free Capsule Endoscopy Inspection," *IEEE Trans. Biomed. Circuits Syst.*, vol. 59, no. 11, pp. 3247-3254, June 2012.

[6] G.B. Lee, H.C. Gwak, Y.S. Kim and W.S. Park, "Wireless power transfer system for diagnostic sensor on rotating spindle," *Proc. IEEE WPT'2013.*, pp. 100-102, May 2013.

[7] H. Jiang, J.M. Zhang, D. Lan, K.K. Chao, S.S. Liou, H. Shahnasser, R. Fechter, S. Hirose, M. Harrison and S. Roy, "A Low-Frequency Versatile Wireless Power Transfer Technology for Biomedical Implants," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 4, pp. 526-535, December 2012.

[8] J.O. Mur-Miranda, G. Fanti, Y.F. Feng, K. Omanakuttan, R. Ongie, A. Setjoadi and N. Sharpe, "Wireless power transfer using weakly coupled magnetostatic resonators," *Proc. IEEE ECCE'2010.*, pp. 4179-4186, September 2010.

[9] Y.K. Tan and S.K. Panda, "Optimized Wind Energy Harvesting System Using Resistance Emulator and Active Rectifier for Wireless Sensor Nodes," *IEEE Trans. Power Electronics*, vol. 26, no. 1, pp. 38-50, July 2010.

[10] C. Alippi and C. Galperti, "An Adaptive System for Optimal Solar Energy Harvesting in Wireless Sensor Network Nodes," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 6, pp. 1742-1750, April 2008.

[11] J.H. Hu, J. Jong, and C.S. Zhao, "Vibration energy harvesting based on integrated piezoelectric components operating in different modes *IEEE Trans. Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 57, no. 2, pp. 386-394, Febuary 2010.

[12] F.B. Stephen, *Communication-Enabled Intelligence for the Electric Power*, ISBN 1118820231, 2014.

[13] S. Rajakaruna, F. Shahnia and A. Ghosh, *Plug In Electric Vehicles in Smart Grids: Integration Techniques*, ISBN 981287299X, 2014.

[14] N. Shinohara, *Wireless Power Transfer via Radiowaves*, ISBN 1118862961, 2014.

[15] E. Sazonov and M.R. Neuman *Wearable Sensors: Fundamentals, Implementation and Applications. Elsevier*, ISBN 0124186661, 2014.

[16] Agbinya and I. Johnson, *Wireless Power Transfer*, ISBN 8792329233, 2012.

[17] T.J. Sun, X. Xie and Z.H. Wang, *Wireless Power Transfer for Medical Microsystems*, ISBN 1461477026, 2013.

[18] X.D. Zhou, L. Liu, T.Y. Sern, M.K. Je and Y.K. Seng, "Integrated circuits design for neural recording sensor interface," *Proc. IEEE APCCAS'2012.*, pp. 17-20, December 2012.

[19] F.G. Zeng, S. Rebscher, W. Harrison, X.A. Sun and H.H. Feng, "Cochlear Implants: System Design, Integration, and Evaluation," *IEEE Reviews in Biomedical Engineering*, pp. 115-142, Febuary 2008.

[20] Glenn W. Carpenter, "Liquid Rectifier," *US Patent* 1,671,970, June 5, 1928.

[21] M. Sawan, Y. Hu, and J. Coulombe, "Wireless powered and bidirectional data exchanged in smart medical microsystems," *IEEE Custom Integr. Circuits Conf.*, pp. 5-12, September 2005.

[22] T. Lehmann and Y. Moghe, "On-chip active power rectifiers for biomedical applications," *Proc. IEEE ISCAS'2005.*, pp. 732-735, May 2005.

[23] C. Peters, J. Handwerker, D. Maurath and Y. Maoli, "An ultra-low-voltage active rectifier for energy harvesting applications," *Proc. IEEE ISCAS'2010.*, pp. 889-892, May 2010.

[24] C. Peters, J. Handwerker, D. Maurath, Y. Manoli, "A Sub-500 mV Highly Efficient Active Rectifier for Energy Harvesting Applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 7, pp. 1542-1550, July 2011

[25] Dan Niu, Zhangcai Huang, Minglv Jiang, Yasuaki Inoue, "A Sub-0.3V highly efficient CMOS rectifier for energy harvesting applications," *NOLTA*, vol. 3, no. 3, pp. 405-416 July 2012.

[26] Y. H. Lam, W. H. Ki, and C. Y. Tsui, “Integrated low-loss CMOS active rectfier for wirelessly powered devices,” *IEEE Trans. Circuits Syst. II, Expr. Briefs*, vol. 53, no. 12, pp. 1378-1382, December 2006.

[27] Song Guo, Hoi Lee, “An Efficiency-Enhanced CMOS Rectifier With Unbalanced-Biased Comparators for Transcutaneous-Powered High-Current Implants,” *IEEE J.Solid-State Circuits*, vol. 44, no. 6, pp. 1796-1840, June 2009.

[28] K. Kotani, A. Sasaki and I. Takashi, “High-Efficiency Differential-Drive CMOS Rectifier for UHF RFIDs,” *IEEE J.Solid-State Circuits*, vol. 44, no. 11, pp. 3011-3018, November 2009.

[29] C. Peters, O. Kessling, F. Henrici, M. Ortmanns, and Y. Manoli, ”CMOS Integrated Highly Efficient Full Wave Rectifier,” *Proc. IEEE International Symposium on Circuits and Systems*, New Orleans, USA, 2007, pp. 2415-2418.

[30] S. S. Hashemi, M. Sawan, and Y. Savaria, “A high-efficiency low voltage CMOS rectifier for harvesting energy in implantable devices,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 4, pp. 326-335, August 2012

[31] Q. Huang and M. Oberle, ”A 0.5-mW passive telemetry IC of biomedical applications,” *IEEE J. Solid-State Circuits*, vol. 33, no. 7, pp. 937-946, July 1998.

[32] M. Sawan, Y. Hu, and J. Coulombe, ”Wirelessly powered and bidirectional data exchanged in smart medical microsystems,” in *Proc. IEEE Custom Integr. Circuits Conf.*, San Jose, CA, pp. 5-12, Sep. 2005.

[33] Y. Hu and M. Sawan,”A fully integrated low-power BPSK demodulator for implantable medical devices,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 12, pp. 2552-2562, Dec. 2005.

[34] S. Y. Lee and S. C. Lee, ”An implantable wireless bidirectional communication microstimulator for neuromuscular stimulation,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 12, pp. 2526-2538, Dec. 2005.

[35] A. Harb, Y. Hu, and M. Sawan, "Low-power CMOS interface for recording and processing very low amplitude signals," *J. Analog Integr. Circuits Signal Process*, vol. 39, pp. 39-54, 2004.

[36] A. Djemouai, M. A. Sawan, and M. Slamani, "An efficient RF power transfer and bidirectional data transmission to implantable electronic devices," in *Proc. IEEE Int. Symp. Circuits Systems*, pp. 259-262, May 1999.

[37] J. A. Von Arx and K. Najafi, "A wireless single-chip telemetry-powered neural stimulation system," in *Proc. IEEE Int. Solid-State Circuits Conf.*, pp. 214-215, Feb. 1999.

[38] Jun Pan, Yasuaki Inoue, and Zheng Liang, "An Energy Management Circuit for Self-Powered Ubiquitous Sensor Modules Using Vibration-Based Energy," *IEICE Trans. Fundamentals*. vol.E90-A, no.10, pp.2116-2123, Oct. 2007.

[39] G.K.Ottman, H.F.Hofmann, and G.A.Lesieutre, "Optimized piezoelectric energy harvesting circuit using step-down converter in discontinuous conduction mode," *IEEE Trans. Power Electron*, vol. 18, no. 2, pp. 696-703, March 2003.

[40] D.C.Hoang, Y.K.Tan, H.B.Chng, and S.K.Panda, "Thermal energy harvesting from human warmth for wireless body area network in medical healthcare system," *Proc. IEEE PEDS'09*, pp. 1277-1282, November 2009.

[41] Y.K.Ramadass, A.P.Chandrakasan, "An Efficient Piezoelectric Energy Harvesting Interface Circuit Using a Bias-Flip Rectifier and Shared Inductor," *IEEE J.Solid-State Circuits*, vol. 45, no. 1, pp. 189-204, January 2010.

[42] Chao Lu, Sang Phill Park, V.Raghunathan and K.Roy, "Efficient power conversion for ultra low voltage micro scale energy transducers," *Proc. Design, Automation & Test in Europe Conference & Exhibition*, pp. 1602-1607, 2010.

[43] F.Moll, A.Rubio, "An approach to the analysis of wearable body-powered system," *Proc. Mixed Design Integr. Crcuits Syst.*, Gdynia Poland, June 2000.

[44] E.O.Torres, G.A.Rincon-Mora, "Electrostatic Energy-Harvesting and Battery-Charging CMOS System Prototype," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 9, pp. 1938-1948, September 2009.

[45] Yang Guangjun, Bai Cunru, and Sun Jing, "Research on Vibration Source and Transfer Path for Power Section of Low Turbulence Wind Tunnel," *Proc. IEEE ICMTMA'10*, pp. 231-234, March 2010.

[46] A.Cammarano, C.Petrioli, D.Spenza, "Pro-Energy:A novel energy prediction model for solar and wind energy-harvesting wireless sensor networks," *Proc. IEEE 9th International conference on Mobile Adhoc and Sensor Systems*, pp. 75-83, October 2012

[47] C.B.Williams and R.B.Yates, "Analysis of a micro-electric generator for microsystems," *Proc. Transducers/Eurosensors*, vol. 1, pp. 369-372, June 1995

[48] E. Dallago, D. Miatton, G. Venchi, G. Frattini, and G. Ricotti, "Self supplied integrable active high-efficiency AC-DC converter for piezoelectric energy scavenging systems," *Proc. IEEE ISCAS'07*, pp. 1633-1636, May 2007,

[49] Yang Sun, In-young Lee, Chang-jin Jeong, Seok-kyun Han, Sang-gug Lee, "An Integrated High-Performance Active Rectifier for Piezoelectric Vibration Energy Harvesting System," *IEEE Trans. Power Electronics*, vol. 27, no. 2, pp. 623-627, February 2012.

[50] Qiang Li, Renyuan Zhang, Zhangcai Huang, and Y.Inoue, "A low voltage CMOS rectifier for wirelessly powered devices," *Proc. IEEE ISCAS'10*, pp. 873-876, May 2010.

[51] Qiang Li, Zhangcai Huang, Renyuan Zhang, Minglv Jiang, Bin Lin, and Y.Inoue, "A low voltage CMOS rectifier for wirelessly powered devices," *NOLTA*, vol. 1, no. 1, pp. 186-195 October 2010.

[52] D.F.Berdy, P.Srisungsitthisunti, B.Jung, X.Xu, J.Rhoads, and D.Peroulis, "Low-frequency meandering piezoelectric vibration energy harvester," *IEEE Trans. Ultrasonics, Ferroelectrics and Frequency Control*, vol. 59, no. 5, pp. 846-858, May 2012.

[53] J.JaeHyuk, D.F.Berdy, L.Jangjoon, D.Peroulis, J.Byunghoo, "A Wireless Condition Monitoring System Powered by a Sub-100 /spl mu/W Vibration Energy Harvester," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 4, pp. 1082-1093, April 2013

[54] S.E.Jo, M.S.Kim, Y.J.Kim, "Electromagnetic human vibration energy harvester comprising planar coils," *IET Electronics Letters*, vol. 48, no. 14, pp. 874-875, July 2012.

[55] X. D. Zou, L. Liu, J. H. Cheong, L. Yao, P. Li, M. Y. Cheng, W. L. Goh, R. Rajkumar, G. S. Dawe, K. W. Cheng and J. Minkyu, "A 100-channel 1-mW implantable neural recording IC," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 10, pp. 2584-2596, March 2013.

[56] H. Ali, A. P. Lobo and P. C. Loizou, "Design and evaluation of a personal digital assistant-based research platform for cochlear implants," *IEEE Trans. Biomed. Circuits Syst.*, vol. 60, no. 11, pp. 3060-3073, May 2013

[57] P.T. Theilmann and P.M. Asbeck, "An analytical model for inductively coupled implantable biomedical devices with ferrite rods," *IEEE Trans. Biomed. Eng.*, vol. 3, no. 1, pp. 43-52, December 2008.

[58] Q. Hunag and M. Oberle, "A 0.5-mW passive telemetry IC of biomedical applications," *IEEE J.Solid-State Circuits*, vol. 33, no. 7, pp. 973-946, July 1998.

[59] M. Sawan, Y. Hu, and J. Coulombe, "Wireless powered and bidirectional data exchanged in smart medical microsystems," *IEEE Custom Integr. Circuits Conf.*, pp. 5-12, September 2005.

[60] S. Y. Lee and S. C. Lee, "An implantable wireless bidirectional communication microstimulator for neuromuscular stimulation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 12, pp. 2526-2538, December 2005

[61] H. K. Cha, W. T. Park, and M. Je, "A CMOS recitifier with a cross-coupled latched comparator for wireless power transfer in biomedical applications," *IEEE Trans. Circuits Syst. II, Expr. Briefs*, vol. 59, no. 7, pp. 409-413, July 2012.

[62] Ning Yin, Guizhi Xu, Qingxin Yang, Jun zhao, Xuewen Yang, Jiangqiang Jin, Weinong Fu, Mingui Sun, "Analysis of Wireless Energy Transmission for Implantable Device Based on Coupled Magnetic Resonance," *IEEE Trans. Magnetics*, vol. 48, no. 2, pp. 723-726, December 2011.

[63] Ming Yin, D.A. Borton, J.Aceros, W.R. Patterson, A.V. Nurmikko, "A 100-Channel Hermetically Sealed Implantable Device for Chronic Wireless Neurosensing Applications," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 2, pp. 115-128, August 2013

[64] K. Shiba, A. Morimasa, H. Hirano, "Design and Development of Low-Loss Transformer for Powering Small Implantable Medical Devices," *IEEE Trans. Biomed. Circuits Syst.*, vol. 4, no. 2, pp. 77-85, April 2010

[65] C. Peters, M. Ortmanns, and Y. Manoli, "Fully CMOS integrated active rectifier without voltage drop," *IEEE Int. 51st MWSCAS*, pp. 185-188, August 2008.

[66] E. Dallago, D. Miatton, G. Venchi, G. Frattini, and G. Ricotti, "Self supplied integrable active high-efficiency AC-DC converter for piezoelectric energy scavenging systems," *Proc. IEEE ISCAS'07*, pp. 1633-1636, May 2007.

[67] T. Umeda, H. Yoshida, S.Sekine, Y. Fujita, T. Suzuki, and S. Otaka, "A 950MHz rectifier circuit for sensor networks with 10 m-distance," *IEEE J.Solid-State Circuits*, vol. 41, no. 1, pp. 35-41, June 2009..

[68] S. Lange, H. Xu, C. Lang, H. Pless, J. Becker, H. J. Tiedkte, E. Henning, and M. Ortmanns, "An AC-powered optical receiver consuming 270μW for transcutaneous 2Mb/s data transfer," *IEEE Int. Solid-State Circuits Conf.*, pp. 304-305, February 2011.

[69] Peter N. C. Lim, "CMOS latching comparator," *US Patent* 5,245,223, September 14, 1993.

[70] Yasuhiko Tsukikawa, "Complementary differential amplifier in which direct current amplification can be set arbitrarily and semiconductor memory using the same," *US Patent* 5,696,726, December 9, 1997.

[71] P. R. Gray, P. J. Hurst, H. S. Lewis, and R. G. Meyer, *Analysis And Design of Analog Integrated Circuits*, 4th ed. New York, 2001.

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Publications

Journal Papers

1. Qiang Li, Jing Wang, Li Ding and Yasuaki Inoue, “A two-stage MOS integrated highly efficient rectifier for vibration energy harvesting applications, ” Journal of International Council on Electrical Engineering, vol. 4, no. 4, pp. 336-340, November 2014.

2. Qiang Li, Jing Wang, Li Ding and Yasuaki Inoue, “A wide input amplitude range, highly efficient rectifier for low power energy harvesting system, ” IEICE Nonlinear Theory and Its Applications, vol. 5, no. 4, pp. 499-511, October 2014.

3. Minglu Jiang, Zhangcai Huang, Atsushi Kurokawa, Qiang Li, Bin Lin and Yasuaki Inoue, “A non-iterative method for calculating the effective capacitance of CMOS gates with interconnect load effect, ” IEICE Transection on Fundamentals of Electronics, Communications and Computer Sciences, vol. E94-A, no. 5, pp. 1201-1209, May 2011.

4. Qiang Li, Zhangcai Huang, Renyuan Zhang, Minglu Jiang, Bin Lin and Yasuaki Inoue, “A low voltage CMOS rectifier for low power battery-less devices, ” IEICE Nonlinear Theory and Its Applications, vol. 1, no. 1, pp. 186-195, October 2010.

International Conference Papers

1. Qiang Li, Dan Niu and Yasuaki Inoue, “A high efficiency CMOS rectifier with ON-OFF response compensation for wireless power transfer in biomedical applications,

” Proceedings 2013 International Symposium on Integrated Circuits, Singapore, pp. 200-204, October 2014.

2. Hui Zhu, Qiang Li, Jing Wang, Ting Wang and Yasuaki Inoue, “A 1-V rail-to-rail bulk-driven op-amp with enhanced transconductances, ” Proceedings The 29th International Technical Conference on Circuits/Systems, Computer and Communications (ITC-CSCC2014), Phuket, Thailand, pp. 256-259, July 2014.

3. Jing Wang, Qiang Li, Li Ding, Hui Zhu, Ting Wang and Yasuaki Inoue, “A sub-1-V supply-insensitive bandgap reference circuit without resistors, ” Proceedings The 29th International Technical Conference on Circuits/Systems, Computer and Communications (ITC-CSCC2014), Phuket, Thailand, pp. 260-263, July 2014.

4. Ting Wang, Yingqian Dai, Qiang Li, Jing Wang, Hui Zhu and Yasuaki Inoue, “An almost 3VDD rail-to-rail op-amp with constant gm,” Proceedings The 29th International Technical Conference on Circuits/Systems, Computer and Communications (ITC-CSCC2014), Phuket, Thailand, pp. 281-284, July 2014.

5. Qiang Li, Dan Niu and Yasuaki Inoue, “A wide input amplitude range, highly efficient rectifier for energy harvesting systems, ” Proceedings 2013 International Conference on Analog VLSI Circuits, Montreal, Canada, pp. 31-35, October 2013.

6. Yawen Yang, Qiang Li and Yasuaki Inoue, “Optimum capacitance ratio for cockcroft-walton charge pump,” Proceedings The 28th International Technical Conference on Circuits/Systems, Computer and Communications (ITC-CSCC2013), Yeosu, Korea, pp. 208-211, June 2013.

7. Qiang Li, Jing Wang, Dan Niu and Yasuaki Inoue, “A two-stage wide input amplitude range highly efficient rectifier for low power energy harvesting systems, ” Proceedings 2013 International Conference on Electrical Engineering (ICEE), Xiamen, China, pp. 199-203, July 2013.

8. Minglu Jiang, Qiang Li, Zhangcai Huang and Yasuaki Inoue, “A non-iterative effective capacitance model for CMOS gate delay computing, ” Proceedings IEEE International Conference on Communications, Circuits and Systems (ICCCAS), Chengdu, China, pp. 896-900, July 2010.

9. Qiang Li, Renyuan Zhang, Zhangcai Huang and Yasuaki Inoue, “A low voltage CMOS rectifier for wirelessly powered devices, ” Proceedings 2010 IEEE International Symposium on Circuits and Systems (ISCAS), Paris, France, pp. 4069-4072, May 2010.

Domestic Conference Papers

1. Qiang Li, Zhangcai Huang, Minglv Jiang, Renyuan Zhangand Yasuaki Inoue, “A low voltage CMOS rectifier for low power battery-less devices, ” The 23rd Workshop on Circuits and Systems in Karuizawa, pp. 306-311, April 2010.

2. Renyuan Zhang, Qiang Li, Zhangcai Huang, Minglv Jiang and Yasuaki Inoue, “An efficient charge pump based on cockcroft-walton structure, ” The 23rd Workshop on Circuits and Systems in Karuizawa, pp. 316-321, April 2010.

Domestic Reports

1. Yingqian Dai, Qiang Li and Yasuaki Inoue, “An almost 3VDD rail-to-rail output amplifier using VDD CMOSFETs, ” The 21th IEICE Kyushu Section Gakusekaikonenkai, C-29, September 2013.

2. Wei Zhou, Zhangcai Huang, Jing Wang, Qiang Li and Yasuaki Inoue, “A low temperature coefficient low-voltage CMOS voltage reference, ” The 21th IEICE Kyushu Section Gakusekaikonenkai, C-23, September 2013.