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博 士 論 文 概 要

論 文 題 目

A STUDY OF ROUTING ALGORITHMS FOR PCB DESIGN

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A printed circuit board (PCB) supplies the connections of electronic components with tracks, pads and other features. It is almost used in all the electronic products and plays a very important role. The complexity of PCB becomes higher and higher since the integrated circuit technology advances rapidly. Such high density of pins makes the routing of PCB a time consuming and error-prone work. Therefore the routing in PCB design is usually dealt with by electronic design automation (EDA) tools to achieve optimizations.

In recent PCB design, due to the high density of integration, the signal propagation delay or skew has become an important factor for a circuit performance. We can control the signal propagation delay by adjusting the wire-length. If the routing area is large enough, it is not difficult to control the wire-length of the net. However, the routing area is usually limited and multiple nets should be considered in the dense area. Hence, how to balance the wire-length of the multiple nets becomes a very difficult problem. Moreover, for river routing problems, in general the positions of pins are fixed on the components, and usually the source and target pins are disordered. Therefore, multi-layers are used for routing disordered pins, and a practical problem that how to assign layers for these pins and in what order to route them needs to be solved.

Besides, in a modern PCB, a flip-chip package is widely used to meet the higher integration density and the larger I/O counts of circuits. In the flip-chip design, redistribution layer (RDL) is often used to redistribute the I/O pads to the bump balls without changing the placement of them. For the pre-assignment RDL routing problem, how to assign the I/O pads to bump balls and minimize the total wire-length are usually focused on. Furthermore, 3D IC has become the good choice for high-performance circuits, since recently it is hard to solve some interconnection problems by traditional 2D IC. Thus, the I/O pad assignment and RDL routing problem in both 2D and 3D IC should be solved to improve the whole circuit performance.

In this research, we propose a series of routing algorithms for PCB design to solve the above-mentioned different problems. This thesis mainly includes the following three points.

Firstly, to assign layers for disordered pins and get equal-length routing results, a region-aware routing algorithm in PCB design is proposed. In the layer assignment process, the longest common subsequence (LCS) algorithm is adopted between source and target pin sets to determine the layers for pins. In the routing process, virtual boundaries need to be set if the pins sequence does not satisfy trunk routing topology condition. The base routes for multiple nets are generated by the single commodity flow method. In addition, considering target length

requirement and routing region coefficient α, R-flip and C-flip techniques are used to adjust the wire-length. This proposed routing algorithm is able to obtain the routes with better wire-length balance and smaller worst length error in reasonable CPU time.

Secondly, to minimize the total wire-length, a sorting-based I/O pad assignment and non-Manhattan RDL routing algorithm are proposed for area I/O flip-chip design. By sorting the Manhattan distance between I/O pads and bump balls, the pre-assignment and its revision are carried out to determine the initial assignment. Three kinds of pair-exchange procedures for shortening wire-length, overlapping and crossing connections are proceeded out respectively to improve the initial assignment. The exchange order is according to the descending Manhattan distance between the assigned I/O pad and bump ball pairs. To shorten the wire-length, non-Manhattan RDL routing with 90 degrees and 45 degrees wire segments is adopted to connect the I/O pads and bump balls. Moreover, some un-routed connections should be ripped-up and rerouted. The proposed design method is effective on reducing total wire-length no matter of the I/O pad locations and package sizes, and improves the routability.

Finally, we apply the same sorting method in the above to the I/O pad assignment and RDL routing method in 3D IC design. Similarly, we assign the same numbered I/O pads in two RDLs to micro-bumps by sorting the sum of Manhattan distance between them. A pair exchange modification of a route is considered for shortening wire-length, and the single layer routing in two RDLs are carried out respectively. Some un-routed connections are ripped-up and rerouted at last. This method for 3D IC is also able to obtain the routes with shorter total wire-length in reasonable CPU time.

In conclusion, the equal-length routing problem for disordered pins and the RDL routing problem for flip-chip in PCB design can be well solved using the proposed routing algorithms. Furthermore, some optimizations, such as better wire-length balance, smaller worst length error and shorter total wire-length, can be well realized by using them.

This thesis is organized as follows:

In Chapter 1, the architecture and package of PCB and the structure of RDL are firstly summarized. Then three typical routing problems in PCB design are introduced, and the research proposals of this paper are given.

Chapter 2 reviews some fundamentals of PCB routing for discussion at the succeeding chapters. Firstly, four types of signal net routing problems are explained. Then, two kinds of basic routing method and their representative algorithms are respectively discussed.

Chapter 3 describes a proposed routing method called a region-aware layer assignment and equal-length routing method for disordered pins in PCB design. By using this algorithm, it is able to obtain the routes with better wire-length balance and smaller worst length error. The experimental results show that, the proposed method could be applied in both no-obstacle routing and obstacle-ware routing problems. Compared with another greedy method for disordered pins, the proposed method gets a smaller standard deviation, in other words, a better wire-length balance among the nets, by adopting coefficient α to adjust the wire-length skew. Besides, our method is effective in reducing worst length error, and the average reduction is 36.69%.

Chapter 4 introduces the second proposed method which is a sorting-based I/O pad assignment and non-Manhattan RDL routing method for area I/O flip-chip design. Our proposed method is effective on reducing wire-length no matter of the I/O pad locations and package sizes. Compared with a partition-based method, the proposed method can reduce the total wire-length by 23.4% using Manhattan routing, and 39.6% using non-Manhattan routing. Compared with another Delaunay-triangulation method, the proposed method can reduce the total wire-length by 3.8% using Manhattan routing, and 20.0% using non-Manhattan routing in the reasonable CPU time.

Chapter 5 presents an application of I/O pad assignment and RDL routing method to 3D IC, on the basis of the sorting method in Chapter 4. Compared with a matching-based method, the proposed method is able to obtain the routes with shorter total wire-length in reasonable CPU times. For small scale package, the average wire-length reduction is 17.52%. Then for large scale packages, the maximum and minimum wire-length reductions are 23.66% and 14.87%, respectively.

Chapter 6 concludes this thesis and discusses the future work.