Graduate School of Fundamental Science and Engineering
Waseda University

博 士 論 文 概 要
Doctoral Thesis Synopsis

論 文 題 目
Thesis Theme

Energy-efficient High-level Synthesis Algorithms for Floorplan-driven SoC Architectures
フロアプラン指向集積回路アーキテクチャを対象とした低エネルギー高位合成に関する研究

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November, 2014 (when *Shuninkai* is held)

Recently, system-on-a-chip (SoC), which contains all the necessary electronic circuits and parts for a system on a single integrated circuit, is widely used in various ICT devices and becomes the important ICT core technologies. SoC design has already been switching from large-lot production of narrow-ranging products to small-lot production of wider-ranging products. Therefore, SoC designers should reduce non-recurring engineering (NRE) costs rather than recurring manufacturing costs. Increasing design abstraction level is one of the most effective strategies for improvements in design productivity. High-level synthesis (HLS) is the LSI design automation technique which obtains circuits from a behavior level description whose design abstraction level is much higher than currently used level, such as register transfer level (RTL) and logic level. HLS tools and the algorithms are evaluated by the performance of the output SoC. In recent SoC design, energy-efficiency has become one of the most important factors due to the growth of battery-powered portable devices. For obtaining low-energy SoC design, (1) HLS should deal with energy-efficient LSI design techniques and (2) module floorplanning in SoC should be considered during HLS.

There are several energy-efficient LSI design techniques such as multiple supply voltages (MSV), dynamic multiple supply voltages (DMSV), and multiple clock domains (MCD). Since any design decision made at earlier stages has higher impacts on the final result, these energy-efficient techniques should be applied during HLS. Several energy-aware high-level synthesis algorithms have been proposed which deal with MSV, DMSV, and MCD. However, the conventional methods cannot reduce energy effectively because they do not consider module floorplanning. First, they cannot estimate circuit delay accurately. As device feature size decreases, an interconnection delay, which is a delay necessary for the communication between modules inside an LSI chip, becomes the dominant factor of circuit total delay. Since the existing works only consider a gate delay which is a delay necessary for the transistors to charge or discharge, energy consumption of circuits cannot reduce as expected or the circuits may be inoperable. Second, they cannot estimate energy consumption sufficiently. For example, the energy consumption of clock signal cannot be estimated when the module placement inside an LSI chip is unknown. In order to solve the problems and reduce further energy consumption, we should integrate module floorplanning into HLS algorithms.

Interconnection delay is another important issue in HLS because interconnection delay accounts for a large percentage of circuit delay as device feature size decreases. There are several HLS algorithms which consider interconnection delay effects. They are not based on a traditional centralized-register architecture, but they are based on

distributed-register architecture (DR architecture) families. In DR architectures, chip area is divided into sufficiently small partitions such that the interconnection delay inside each partition can be assumed to be zero. The interconnection delay between the partitions is estimated by placement information which can be obtained by floorplanning the partitions during HLS. Furthermore, more various kinds of energy consumption, such as clock signal energy and interconnection energy, can be estimated if we use DR architectures. However, the objective of conventional DR architectures and synthesis algorithms is the optimization of circuit latency and they do not consider energy efficiency. Conventional methods are not suitable to adopt energy-efficient LSI design techniques such as MSV, DMSV, and MCD.

In this dissertation, I propose new floorplan-driven SoC architectures to which energy-efficient LSI design techniques, such as MSV, DMSV, and MCD, are easily applicable. Furthermore, the associated HLS algorithms are proposed for energy reduction based on the proposed the architectures. The proposed algorithms can reflect floorplanning information in HLS by using iterative synthesis flows. By using a floorplanning result, interconnection delay and energy consumption can be estimated, and then optimized supply voltages and/or clock periods can be assigned for energy reduction. Experimental results show that the proposed methods achieve 22.4% energy-saving by applying MSV, 43.9% energy-saving by applying DMSV, and 57.0% energy-saving by applying MCD and MSV compared with the existing methods.

Chapter 1 [Introduction] describes the background on the proposed research and the outline of this dissertation.

Chapter 2 [Related Works] briefly discusses the related works. First, I preview the low-power and low-energy LSI design techniques and energy-efficient HLS algorithms which consider the techniques such as MSV, power gating (PG), DMSV, and MCD. Next, I preview the DR architecture families and the HLS algorithms for the architectures which can consider floorplanning during HLS.

Chapter 3 [A Multiple Supply Voltages Aware High-level Synthesis Algorithm for HDR Architecture] proposes the huddle-based distributed-register architecture (HDR architecture) and an HLS algorithm associated with HDR architecture. HDR architecture divides chip area into several partitions called *huddles*. Huddles enable us to estimate interconnection delay effects easily and assign supply voltages effectively. The proposed HLS algorithm can automatically apply MSV to SoC by assigning voltages to huddles and outputs energy-efficient SoC designs. Experimental results show that the proposed method achieves 22.4% energy-saving compared with the conventional methods.

Chapter 4 [MH^4: Multiple Supply Voltages Aware High-speed and High-efficiency High-level Synthesis Algorithm for HDR architecture] proposes the improved HLS algorithm for HDR architecture called MH^4. The algorithm proposed in Chapter 3 has the two severe problems: (A) the huddle-area and interconnection-delay oscillation during iterations and (B) the insufficient huddle construction methods. In this chapter, I propose three new techniques, virtual area estimation, virtual area adaptation, and floorplanning-directed huddling to resolve the problems (A) and (B) and then I propose a new multiple-supply-voltages aware high-speed and high-efficiency high-level synthesis algorithm for HDR architecture. Experimental results show that the proposed algorithm achieves 29.1% run-time-saving compared with the algorithm in Chapter 3, and successfully obtains a solution which cannot converge when the algorithm in Chapter 3 is used. This is because MH^4 improves the convergence of the solution by the proposed area estimation and the huddle configuration method.

Chapter 5 [SAAV: Dynamic Multiple Supply Voltages Aware High-level Synthesis Algorithm for AVHDR Architecture] proposes the adaptive voltage huddle-based distributed-register architecture (AVHDR architecture) and an HLS algorithm associated with AVHDR architecture. First, I propose new distributed-register architecture called AVHDR architecture which can apply DMSV. Next, I propose the new HLS algorithm for AVHDR architecture called SAAV. In the AVHDR architecture and SAAV, low supply voltages can be assigned to non-critical operations and leakage power can be cut off through PG. Experimental results show that the proposed method achieves 43.9% energy-saving compared with the conventional methods.

Chapter 6 [SAMCID: Multiple Clock Domains Aware High-level Synthesis Algorithm for HDR-mcd Architecture] proposes the HDR-mcd architecture and an HLS algorithm associated with HDR-mcd architecture. First, I propose new distributed-register architecture called HDR-mcd architecture which can apply MCD. Next, I propose the new HLS algorithm for HDR-mcd architecture called SAMCID. Experimental results show that the proposed method which only considers MCD achieves 32.5% energy-saving compared with the conventional methods. Furthermore, the proposed method which can apply MCD and MSV simultaneously achieves 57.0% energy-saving compared with the conventional methods.

Chapter 7 [Conclusion] summarizes the research and indicates future works.

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(List of research achievements for application of doctorate (Dr. of Engineering), Waseda University)

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（As of Feb., 2015）

種 類 別 (By Type)	題名、　発表・発行掲載誌名、　発表・発行年月、　連名者（申請者含む）(theme, journal name, date & year of publication, name of authors inc. yourself)
a. 論文 学術誌原著論文 第一著者	○**S. Abe,** Y. Shi, K. Usami, M. Yanagisawa, and N. Togawa, "Floorplan Driven Architecture and High-level Synthesis Algorithm for Dynamic Multiple Supply Voltages," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, vol. E96-A, no. 12, pp. 2597-2611, Dec. 2013. ○**S. Abe,** Y. Shi, M. Yanagisawa, and N. T [4] : multiple-supply-voltages aware high-level synthesis for high-integrated and high-frequency circuits for hdr architectures," IEICE Electronics Express, vol.9, no.17, pp.1414–1422, Sept., 2012. ○**S. Abe,** M. Yanagisawa, and N. T -efficient high-level synthesis for hdr architectures," IPSJ Trans. on System LSI Design Methodology, vol.5, pp.106–117, Aug, 2012.
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(List of research achievements for application of doctorate (Dr. of Engineering), Waseda University)

種 類 別 By Type	題名、　発表・発行掲載誌名、　発表・発行年月、　連名者（申請者含む）(theme, journal name, date & year of publication, name of authors inc. yourself)
c. 講演 国内学会 (査読付き)	**阿部晋矢,** 史又華, 宇佐美公良, 柳澤政生, 戸川望, “フロアプラン統合化アーキテクチャを対象とした複数クロックドメインおよび複数電源電圧による低電力化高位合成手法,” 情報処理学会 DA シンポジウム 2013 論文集, pp.139-144, 下呂市, 2013 年 8 月 22 日. 赤坂宏行, **阿部晋矢,** 柳澤政生, 戸川望, “HDR アーキテクチャを対象とした多段階クロックゲーティングを用いた低電力化高位合成手法,” 情報処理学会 DA シンポジウム 2013 論文集, pp.43-48, 下呂市. **阿部晋矢,** 史又華, 宇佐美公良, 柳澤政生, 戸川望 “HDR-mcd を対象としたマルチクロックドメイン指向の低電力化高位合成手法,” 第 26 回 回路とシステムワークショップ, pp. 185-190, 淡路市, 2013 年 7 月 29 日. **阿部晋矢,** 宇佐美公良, 柳澤政生, 戸川望, “動的複数電源電圧およびフロアプラン統合化アーキテクチャを対象とした低電力化高位合成手法,” 情報処理学会 DA シンポジウム 2012, pp.163-168, 下呂市, 2012 年 8 月 30 日. **阿部晋矢,** 柳澤政生, 戸川望, “高集積かつ高周波な回路に対応した複数電源電圧指向の高位合成手法,” 第 25 回 回路とシステムワークショップ, pp. 160-165, 淡路市, 2012 年 5 月 30 日. **阿部晋矢,** 柳澤政生, 戸川望, "複数電源電圧および複数サイクルレジスタ間通信指向の低電力化高位合成手法," 情報処理学会 DA シンポジウム 2011, pp. 21-26, 下呂市, 2011 年 8 月 31 日.
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早稲田大学　博士（工学）　学位申請　研究業績書

(List of research achievements for application of doctorate (Dr. of Engineering), Waseda University)

種 類 別 By Type	題名、　発表・発行掲載誌名、　発表・発行年月、　連名者（申請者含む）(theme, journal name, date & year of publication, name of authors inc. yourself)
e.その他 (業績賞等)	2014 年 11 月 情報処理学会デザインガイアポスター賞. 2014 年 8 月 情報処理学会優秀発表学生賞. 2014 年 3 月 情報処理学会山下記念研究賞. 2013 年 8 月 情報処理学会優秀発表学生賞. 2012 年 8 月 情報処理学会優秀発表学生賞. 2012 年 5 月 電子情報通信学会集積回路研究専門委員会優秀若手講演賞.
(日本学術振興会 科学研究費補助金)	日本学術振興会特別研究員奨励費, “低消費電力 LSI 実現へ向けた高位・物理統合設計技術の開発,” 2013-2014 年度, 総額 220 万円(2013 年度:110 万円, 2014 年度:110 万円).