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博 士 論 文 概 要

論 文 題 目

Research on Low Power Technology by AC Power Supply Circuits

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In recent years, mobile devices are widely used in the consuming electronics field, and the battery life becomes a very important criterion for a device. Therefore, the power dissipation of a circuit is concerned more than ever before; in many applications, it is even more important than the high speed performance. Many directions, including novel system structures such as clock gating, novel algorithms such as parallel calculation, and novel circuit technology such as sub-threshold logic, are researched to lower circuits' power dissipation. Because the performance of portable devices increases dramatically, if there is no great development in the battery technology, the battery life of portable device will become very poor or a large size of battery will be necessary. Several technologies such as sub-threshold logic, power gating and clock gating are proposed to prevent the power dissipation from increasing so dramatically. With these technologies, circuits can work with very low power dissipation, but as the power is reduced, the operation frequency is also lowered. In this dissertation, charge recovery logic technology is researched; the research area includes novel structure of charge recovery logic and application area is also discussed.

Charge recovery logic is also a technology to lower the power dissipation of circuits. The basic concept of charge recovery logic uses clock as power supply. As clock rises and falls, energy is charged into and discharged from circuits, and during this procedure, energy can be recycled and only dissipates on parasitic resistance. The principle of charge recovery logic was researched firstly in 1961, and with the principle, charge recovery logic was applied in circuits design in 1990s. Until today, researches on charge recovery logic are processing, and many novel structures of charge recovery logic, such as ECRL, ADCVSL, CPAL, CAMOS, ADCL, 2PDADCL, and QSERL, have been proposed. These published charge recovery logics achieve low power dissipation in low operation frequency range, but when the operation frequency is higher than 100MHz, these types cannot work correctly any more. To apply the charge recovery logic in a higher frequency range, other types of charge recovery logic such as boost logic, enhanced boost logic, and sub-threshold boost logic are proposed. These types of charge recovery can work at Giga-hertz level with low power dissipation. But still they have shortcomings: low value of DC voltage power supply is required. This shortcoming would cause high complexity of circuits and extra requirements of peripheral circuits (e.g. multiple DC-DC converters). This dissertation proposed two novel types of charge recovery logic which can work in a high operation frequency with even lower power dissipation comparing with previous works. Moreover, several application fields of charge recovery are also discussed. This dissertation contains 5 chapters which are listed as follows:

Chapter 1 [Introduction] discusses the background of low power technologies and introduces several types of low power technologies. The principle of charge recovery logic is explained and several published charge recovery logics are introduced. To generate the power clock to drive charge recovery logic, the structure of *LC* oscillator is introduced and the power dissipation of the oscillator is analyzed in Chapter 1.

Chapter 2 [Pulse Boost Logic and Application on Multiplier] presents a novel structure of charge recovery logic named Pulse Boost Logic (PBL). The PBL uses two-phase non-overlapped power clock as power supply. PBL gate is divided into logic evaluation part and boost part. The logic parts consist of two-rail complementary evaluation blocks and for each rail, pull up network (PUN) and pull down network (PDN) are constructed by NMOS to promote the circuit performance in high frequency range. The boost part is a latch structure which is used to boost up the evaluated value from evaluation part. Energy firstly is charged into the evaluation part and logic value is evaluated, then the boost part is charged to amplify the evaluated value while the energy is discharged from the evaluation part. In Chapter 2, the power dissipation of PBL is analyzed theoretically, and comparing with previous types of charge recovery logic, PBL has lower power dissipation according to the analytic result. To demonstrate the low power of PBL, a 4-bit multiplier is designed and fabricated with 0.18μm CMOS technology. To detect the operation frequency, a 5-bit counter is designed for frequency dividing, and to convert AC format output of PBL to normal DC logic signal, data A/D converter is also designed. In simulation, PBL can work at as high as 1.8GHz, and dissipates less energy comparing with Enhanced Boost Logic, which has similar structure with PBL. The measurement of test chip is at an operation frequency up to 161MHz, and the power dissipation of the design is 772μW including 4-bit pipeline multiplier, frequency divider and data A/D converter.

Chapter 3 [Pseudo NMOS Boost Logic and Application on Large Scale Logic Circuits] presents another novel type of charge recovery logic called Pseudo NMOS Boost Logic (pNBL). The structure of PBL has four complementary blocks in its logic evaluation parts, which requires a large number of transistors, and pNBL is proposed to solve this problem. PNBL utilizes pseudo-NMOS structure in its evaluation part, and by this method, almost half number of transistors are reduced. When pNBL evaluates the logic value, the large sized PMOS transistors are on, and PDN in one side of the two-rail evaluation network pulls the evaluated logic down. The boost part amplifies the evaluated voltage value and output to other gates. During this procedure, energy is charge and discharged the same with that in PBL. The power dissipation of pNBL is also analyzed, and the analytic

result shows that the pNBL has lower power dissipation comparing with PBL and EBL. To demonstrate the low power dissipation of pNBL, a Processing Engine which is used in LDPC decode system is designed and fabricated with pNBL in standard 0.18μm CMOS process technology. The simulation results show when operation frequency is lower than 1.1GHz PE with pNBL gates achieves lower power dissipation than PE with conventional static CMOS gates. At the frequency range of several hundred megahertz which LDPC application is usually applied, energy dissipation of PE with pNBL gates is reduced much. The proposed PE dissipates 3.5pJ per cycle at 1.1GHz, and 1pJ at 403MHz in simulation. The latter one is only 36% of PE with static CMOS gates. Comparing with other charge recovery logic, pNBL also has a better performance over energy dissipation. The test chip was fabricated and measured, the result showed that the test chip can work at frequency up to 609MHZ with the energy dissipation of 2.1pJ/cycle including PE module and blip power clock generator.

Chapter 4 [Other Applications of Charge Recovery Logic] discusses two specified applications which is suitable to the charge recovery logic. Because charge recovery logic is driven by sinusoidal format power clock, it can be applied in the AC power environment such as wireless power transmission. In this chapter, an on-chip inductive coupling system is built, and the load circuits are designed with pulse boost logic (PBL). Due to the characteristics of PBL, no voltage rectifier is required and the power can be saved. The test chip was fabricated and measured; the result indicates that power transmitted by the system is 22mW while the value in previous work is 2.5mW. Other than wireless power transmission system, crystal oscillator also generates sinusoidal format clock. In sensor network systems, sensor nodes are using the crystal oscillator as clock generator. While in the sleep mode, only real time counter works in sensor node. But to drive the real time counter and other digital circuits, a converter is required to convert sinusoidal clock to square wave clock and the converter consumes relative large power. By substituting the conventional static CMOS with charge recovery logic to construct the real time counter, the power dissipation in sleep mode can be reduced dramatically. To demonstrate this proposal, 16-bit counters with both pseudo-NMOS Boost Logic (pNBL) and static CMOS are designed. The simulation results show that real time counter with charge recovery logic dissipates only 16% power of that dissipated by counter with static CMOS. Adding the power dissipated by the clock signal converter, sensor node structure with charge recovery logic counter reduced 92% power dissipation comparing with conventional structure.

Chapter 5 [Conclusion] summaries the proposals and draws conclusion of this dissertation.