Study on Low Power RF ICs with Adaptive Bias Circuits for Wireless Communications

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Waseda University Doctoral Dissertation

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Contents

Chapter 1Introduction

1.1 Backgroundof this research

Nowadays, wireless communications have impacted our daily life. Mobile phones can be used anytime and anywhere to make a call, to send short messages and to surf the Internet, etc. Transceiver ICsare the key components for wireless communications and the power consumption of transceiver decides the battery-time of the mobile terminals.For instance, with the development of IoT, there isa huge demand of the wireless communication systems connecting the IoT sensors and wearable devices to the Internet.The IoT devices are generally supplied with small batteries with critically limitedcapacity, such as button battery, solar-cell battery and energy harvesting system. Thus,decreasing the power consumption of transceiver ICs in the IoT device plays a crucial role.

In this dissertation, several adaptivebias circuits are proposed to decrease the power consumption of the RF building blocks in transceiver.Since bias circuits are flexible and have negligibleinfluence on the operational frequency, the proposed adaptive circuits are expected to be widely utilized in various wireless communication systems.

The frequency band interest in this dissertation is GHz-band including 2.4-GHz band (IEEE S-band), 5-GHz band (IEEE C-band) and 80-GHz band(IEEE W-band) [1]. The 2.4-GHz band could be applied for the wireless communications of Bluetooth [2]-[3], WLAN 802.11b/g [4]and Zigbee[5], etc. Since the 2.4-GHz band is crowdedand heavily used to the point,frequent dropped connections and degradation of service limits the data rate of the 2.4-GHz band wireless communications.

The 5-GHz bandcould be applied for the 802.11a Wireless Local Area Network (WLAN) communicationswithmore usable channels,higherreliability and higher data ratethan 2.4-GHz band communications. WLANhas become very popular not only in home and office but also at large public areas (airports, large shopping centers and sports stadiums, for instance). The WLAN 802.11a standarduses a 52-subcarrier Orthogonal Frequency-Division Multiplexing (OFDM) with a maximum raw data rate of 54 Mbit/s[6].

With the development of device process, the cut-off frequency and maximum

oscillation frequency of transistor increases, which make the RF ICs could operate at higher frequency. Recently,research on RF ICs in W-bandhas become popular for several applications, such as automotive radar [7]-[8], high-speed networks [9], imaging and gesture recognition [10]. In 2009, European Telecommunication Commission Institute (ETSI) has assigned a Short Range Radar (SRR) band from 77 to 81 GHz [7]. In 2012, the International Telecommunication Union (ITU) has recommended vehicular collision avoidance radars in the frequency band from 77 to 81 GHz [8]and fixed wireless systems (FWS) operating in the 71-76 and 81-86 GHz range [9]. A 94 GHz pulsed-radar transceiver was reported for the applications of imaging and gesture recognition [10].

1.2 Motivationsof this research

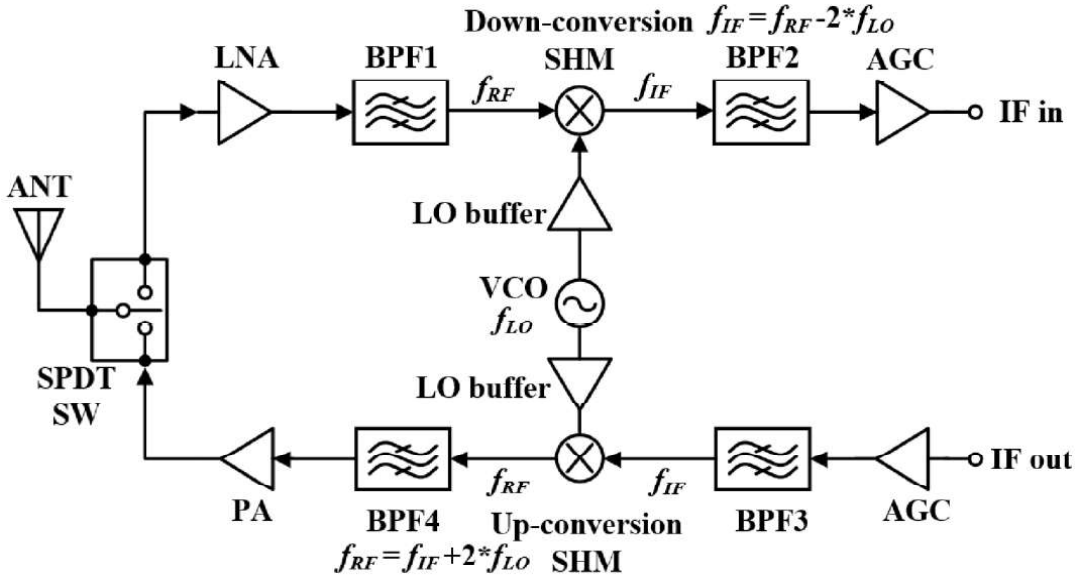

Figure 1-1 A typical block diagram of sub-harmonic transceiver IC in [11].

Figure 1-1shows atypical block diagram of sub-harmonic transceiver IC in [11]. In the receivermode, the RF input signalis received by the antenna (ANT) and switched the Single-Pole-Double-Throw Switch (SPDT SW) to Low Noise Amplifier (LNA). The LNAamplifies the RF signal. The Band Pass Filter (BPF1) works as an "image-reject" filter with a relatively small loss in the RF band and a large attenuation in the image band. The Voltage-Controlled Oscillator (VCO)generates the LO signal for mixing with the RF signal. The down-conversion Sub-harmonic Mixer (SHM)mixes the RF signal with the second harmonic of LO signal and down-converts the RF signal

to the IF signal ($f_{IF}=f_{RF}-2*f_{LO}$). The BPF2selects the IF channel of interest and removes the DC offset caused by theLO leakage of the mixer. Then Automatic Gain Control (AGC) amplifier amplifies the IF signal.

The transmitter architecture is similar to the receiver, but with the operations performed in "reverse" order. In the transmitter mode, the IF signal is firstly strengthened by the Automatic Gain Control (AGC) circuit and thenselected by the BPF3between AGC and Up-conversion SHM. Then the IF signal is mixed with the LO signal and up-converted to RF signal by the up-conversion SHM. The BPF4works as image-reject filter and attenuates the image signal generated by the up-conversion SHM. Then the RF signal is amplified by the power amplifier (PA), switchedby the SPDT SW andtransmittedthrough the ANT.

Table 1-1 Power consumption of each block in a 2.4/5-GHz band transceiver IC [12]

		Receiver		**Transmitter**			
Block		LNA & mixer	LO buffer	PA & mixer	LO buffer	VCO & PLL	Total
DC power	(mW)	36	36	72	14.4	39.6	198
	(%)	18.2	18.2	36.4	7.3	20.0	100

Table 1-2 Power consumption of each block in a 60-GHz band transceiver IC [13]

		Receiver		**Transmitter**			
Block		LNA	Mixer & LO buffer	Mixer & LO buffer	PA (On-chip & external)	VCO & PLL	Total
DC power	(mW)	30	44	53	154+732	80	1093
	(%)	2.7	4.0	4.8	81.1	7.3	100

Table 1-1and Table 1-2show the power consumption of each block in a 2.4/5-GHz band transceiver IC [12]and a 60-GHz band transceiver IC [13], respectively. In both transceivers, the PA is the most power-consuming block.VCO and LO buffer also significantly influence thepower consumption of transceiver IC.Thus, decreasing the power consumption of PA, VCO and LO buffer is effective to decreases the power consumption of transceiver. It is noted that the power consumption of LO buffer is decreased by decreasing the output power of LO buffer, which is decided by the LO

power requirement of SHM.

Hence, the research objective in this dissertation is to decrease the power consumption of transceiver by decreasing the power consumption of PA (Chapter 2), VCO (Chapter 3) and decreasing the LO power requirement of SHM (Chapter 4).

1.2.1 Power AmplifierIC

InChapter 2, a high linearityand high efficiencySiGe Heterojunction Bipolar Transistor(HBT)PAIC is designed for WLAN 802.11a applications. In transceiver, PA is the most power-consuming block.PA with higher efficiency has low power consumption with the same out power. Thus, PA should be designed with high Power Added Efficiency (PAE).

Sincethe PA IC is designed for WLAN 802.11a applications, OFDM signal is inserted as input signal. In OFDM transmissions, a large number of subcarriers are transmitted in parallel, which allows subcarriers to either add or subtract from one another at each point in time. As a result, the power statistics of an OFDM transmission are almost Gaussian in nature, leading to high Peak-to-Average-Power Ratio (PAPR) up to 10 dB in 64 Quadrature Amplitude Modulation (QAM) OFDM transmission [14]. In addition to the amplitude, the phase of the signal is also modulated in OFDM transmission. Hence, the PA should be designed with low gain compression (low AM-AM) and low phase distortion (low AM-PM) at large signal to meet the Error Vector Magnitude(EVM) specification for WLAN 802.11a communication.

In summary, the PA IC should be designed with high PAE while meeting the EVM specification.Thus, an adaptivebias circuit is proposedfor the PA IC design. Under the lowRF input power, the bias supplies the PA with small bias current, which decreases the power consumption and improves the efficiency. Under the highinput RF power, the bias circuit adaptively increases the bias currentof PA, which provides the PA with a largeswing range of output current and improves the linearity of PA. Hence, the proposed bias circuit the decreases the power consumption of PAIC without degrading thelinearityperformanceat large signal.

1.2.2 Voltage-ControlledOscillator IC

InChapter 3, alow voltage and low power CMOS VCO ICis designed for 2.4-

GHz band applications. Since the low power communication protocolsuch as Bluetooth Low Energy (LE) and Zigbee utilize 2.4-GHz band. This frequency band is quite suitable for the application of IoT devices. It is popular to use thelow voltage power supplysuch as solar-cell battery andenergy harvesting systemfor IoT devices.Thus, it is important to decrease the power supply of VCO.In addition, decreasing the power supply is also an effective method to decrease the power consumption.Thus, the VCO is designed for ultra-low-voltage operation.

The oscillation start-up is a critical issue for low voltage VCO design. It is well known that when gate-to-source bias voltage (Vgs) of transistor is lower than the threshold voltage (V_{TH}),transistor has NO gain at small signaland has gain at large signal.Thus, VCO requires high bias voltage for oscillation start-upand a low bias voltage to maintain the low power oscillation.

In summary, the VCO IC should be designed for low voltage and low power operation with robust oscillation start-up.Thus, an adaptivebias circuit is proposed for the VCO IC design. Initially, the bias circuit provides the VCO with high Vgs biasfor robust oscillation start-up. After oscillationis detected, the bias circuit adaptively decreases thebias voltage and shifts the VCO into low powersteady state. Hence, the proposedbias circuitdecreases the power consumption of VCO IC without influencing the robustness of oscillation start-up.

1.2.3 Down-conversionSub-harmonic M ixer IC

InChapter 4, alow power SiGe Sub-harmonic Mixer (SHM)ICis designed for 80-GHz band applications. It is noted that employing a SHM instead of mixer is an attractive solution in the millimeter-wave superheterodyne receiver.When the operation frequency increases, the transconductance of transistor and Q-factor of varactor significantly decrease.Thus, high frequencyVCO consumes high power for oscillation start-up, displays relatively poor spectral purity and haslimited tuning range. A frequency doubler is reported to double the frequency ofLOsignalfor mixingand to halve the oscillation frequency of VCO [16]. However, frequency doubler has high power consumption and requires a buffer amplifier operating at the frequency of $2*f_{LO}$ to drive the mixer, which brings severe power consumption. Alower power-consuming solution is reported to removethe frequency doubler and to utilizeaSHM instead of

mixer[17].SHM can mix the RF signal with 2* f_{LO} signal. The IF frequency (f_{IF}), RF frequency (f_{RF}) and LO frequency (f_{LO}) of SHM satisfy: $f_{IF} = f_{RF} - 2 * f_{LO}$. With relatively low oscillation frequency, the VCO has better phase noise performance, and the LO buffer couldprovide higher LO power with lower power consumption.

Sinceone of theresearch objects is to decrease the power consumption of LO bufferby improving the SHM design. Twoaspectsare considered for the SHM IC design. The first one is that decreasing the LO power requirement of SHM is effective to decrease the output power and power consumption of LO buffer.

The second one is that making conversion gain of SHM insensitive to LO power could remove the power control circuit of LO bufferand accordinglydecrease the power consumption of LO buffer.When injected LO power changes, the transistor requires different bias voltage to flattenthe generation of LO second-harmonic (2* f_{LO}) and to flatten the conversion gain.

In summary,SHM should be designed with low LO power requirement and with conversion gain insensitive to LO power.The proposal of SHM include two parts. The first is to propose a novel topology to decrease the LO power requirement of SHM. The second is to propose an adaptive bias circuit to flatten the conversion gain of SHM. When the LO power changes, the proposed bias circuit adaptively changes the bias voltage of LO doubling stage to flatten 2f_{LO} generation and the conversion gain.Hence, the proposal in Chapter 4 decreases the LO power requirement of SHM and makes the conversion gain of SHM insensitive to LO power, which is expected to decrease the power consumption of LObuffer.

1.3 Organization of this dissertation

The main focusofthis dissertation is to decrease the dc power consumptionof transceiver by decreasing power consumption of the RF building blocks including PA, VCO and LO buffer ICs.The methodto decrease the power consumption of the RF building blocks is proposingadaptive bias circuitsto decrease the power consumption of PA and VCO, and to decrease the LO power requirement of SHM.

Considering this focus, this dissertation is structured in five chapters. InChapter 1, the research background, motivations, and the organization of this dissertation have been briefly introduced.

In the following,adaptivebias circuits are presented to improve thepower consumption of RF ICs, including PA IC in Chapter 2, VCOIC in Chapter 3, and SHM IC in Chapter 4, respectively.From Chapter2 to Chapter 4, the proposals are presented with the review of previous works, process introduction. Inthe following, the operation principles and circuit design are described in details. Then measured performance and comparison with previous works are shown to confirm the effectiveness of the proposed bias circuits on decreasing power consumption.

At last, conclusions of this dissertation and main areas for future research on the adaptive bias techniques will be given in Chapter 5.

1.4 Conclusion

In this dissertation, adaptivebias techniquesare researched to decreasethe dc power consumption of RF ICs.Three RF ICsare proposed withadaptivebias circuits to improvethe power consumption as:

1.5-GHz band SiGe HBT PA IC with an adaptive bias circuit.

2.2.4-GHz band CMOS VCO IC with an amplitude feedback bias circuit.

3.W-band SiGe HBT SHM IC with a bottom-LO-configurationand a tail current bias circuit.

In this chapter, the research background, motivationsand organization of this dissertation are presented.The background of this research is firstly introduced in Session 1.1, including the applications of 2.4-GHz 5-GHz 80-GHz bands. Then the motivations s of this research are given in Session 1.2, including the roles of PA, VCO, and SHM in the transceiver andthemotivationsof adaptivebias circuits.Finally, organization of this dissertation is shown in Session 1.3.

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Chapter 2 High Linearityand High Efficiency SiGe HBT PA IC with an AdaptiveBias Circuit

2.1 Introduction

PAplays a particularly important role in transceiver anddecides the output power level of the whole transmitter.As mentioned in Chapter 1, PA is the highest power consuming block in the transceiver.Increasing the efficiency of PA candecrease the power consumption of PA with the same output power, which is effective to decrease the power consumption of transceiver.Consideringthat the supply voltage of PA is limited by the breakdown voltage of the transistor, it is popular to biasthe PA with large current for high output power. Thus, the adaptive control of bias current in PA becomes the critical issue.

In this chapter, an adaptive bias circuit is proposed to improve the linearity and efficiency of SiGe HBT power amplifier (PA) IC[1]-[2]. Since the PA is applied for the WLAN 802.11awireless communications, 64 QAM OFDM modulation with high PAPR (9-10 dB)is utilizedin transmissions.Thus, PA should be designed with low gain compression and low phase distortion under high input power to meet EVM specification. The proposed bias circuit provides the PA with low bias current under the low input power to improve the efficiency, and provides the PA with high bias current under the high input power to improve the linearity. Hence, the proposed bias circuit improves the efficiency of PA without degrading the linearity performance.The utilization of adaptive bias circuits has additional features, such as: 1) low additional DC power consumption, 2) little insertion loss, 3) almost no additional chip area.

A three-stage 5-GHz band PA IC with the proposed adaptivebias circuit for WLAN 802.11ac applications is designed,fabricated and fully tested in IBM 350-nm SiGe BiCMOS process.

In this chapter, introduction is firstly given in Section 2.1, including the performance parameters of PA, review of previous PA ICs and brief descriptions of 350-nm SiGe BiCMOS process. The proposedregulator bias circuit is described in detail in Section 2.2, including working principle analysis andlinearity improvement to PA. Then in Section2.3, athree-stage linear PA IC with the proposedbias circuit for 5-GHz band WLAN applications is presented with the circuit schematic and simulated

performance.In Section 2.4,measured performance is demonstrated with the comparison of previous works to confirm the effectiveness of the proposal.Finally, conclusions are given in Section 2.5.

2.1.1 Performance parametersofPA

2.1.1-a) Frequency band

The wireless communication standards 802.11a, 802.11n, and 802.11ac amendments all utilize the 5 GHz band ranging from 5.15 GHz to5.875 GHz,which is a mix of ISM and Unlicensed National InformationInfrastructure (U-NII) bands[3]. Since the supply voltage of PA is limited by the breakdown voltage of transistor, high output power of PA is realized by providing PA with highbias current and large output current swing. Thus, the power transistor in PA usually have an exceedinglylarge size, which results in very low input and output impedance of the power transistor.

The matching network should transform the low impedance to the characteristic impedance (typically 50 Ω).Constant Q lines in Smith Chart could be applied to evaluate the frequency bandwidth of the matching network. The Q of the impedance transformation network is defined as $Q = f_r/\Delta f$ [4], where f_r is the operation frequency and Δf is the frequency bandwidth, respectively.

When Q increases, the matching network has narrower bandwidth and requires less passive devices for the impedance transformation. In addition, the increase of passive devices increases the area and loss of matching networkand might decrease the linearity and efficiency of PA. Hence, 3-stage LC broadband output matching network is utilized to satisfy the bandwidth requirement.

2.1.1-b)Linearity

The linearity performance of PA is critical for some vector modulation methods in the wireless communications. In the transmitter, the nonlinearity of PA causes amplitude compression and phase distortion. There are many parameters to evaluate the linearity performance.

The input and output 1 dB compression point (IP1dB and OP1dB)are defined as the input and outputsignal powerwhen the power gain decreases 1dB from the small signal gain.Since OP1dB only shows the gain compression of power amplifier, it is not suitable to evaluate the linearity of WLAN PA.

In addition to 1 dB compression point, WLANuses a primary metric called Error Vector Magnitude (EVM) as a measure of modulation quality and linearity of transmitter. Figure 2-1 illustrates the reference vector and error vector for EVM calculation. In the PA measurement, an error vector is a vector in the I-Q plane between the reference constellation pointat the input of PA and the point at the output of PA.

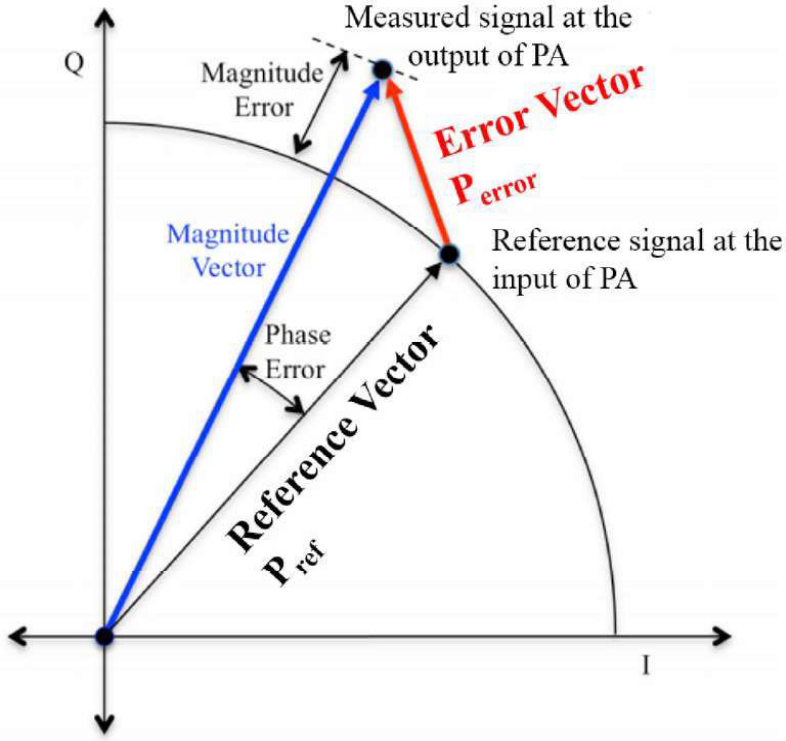


Figure 2-1.The Reference vector and error vector for EVM calculation.

The EVM is defined as the ratio of thepower of the error vector (P_{err}) to the power of the referencevector (P_{ref}) as:

$$\mathrm{EVM(dB)} = 10 \times \log\left(\frac{P_{err}}{P_{ref}}\right) \quad (2\text{-}1)$$

$$\mathrm{EVM(\%)} = \sqrt{\frac{P_{err}}{P_{ref}}} \times 100\% \quad (2\text{-}2)$$

Compared to OP1dB, EVM gives a more comprehensive evaluation of the PA linearity performanceincluding gain compressionand phasedistortion. Table 2-1 shows how the EVM specification varies with bit rate.In Table 2-1, there is a very clear relationship between the modulation quality and the complexity of the modulation scheme.

In this work, OP1dB and EVM performance of the proposed 3-stage PA IC with

the regulator bias circuit will be measured to evaluate the linearity and to confirm whether the PA IC meet the 802.11a WLAN standard.

Table 2-1 EVM limits for OFDM 802.11 a

Modulation Scheme	Code Rate	Data Rate (Mbit/sec)	EVM limit (dB)	EVM limit (%)
BPSK	1/2	6	-5	56.2
BPSK	3/4	9	-8	39.8
QPSK	1/2	12	-10	31.6
QPSK	3/4	18	-13	22.3
16-QAM	1/2	24	-16	15.8
16-QAM	3/4	36	-19	11.2
64-QAM	2/3	48	-22	7.9
64-QAM	3/4	54	-25	5.6

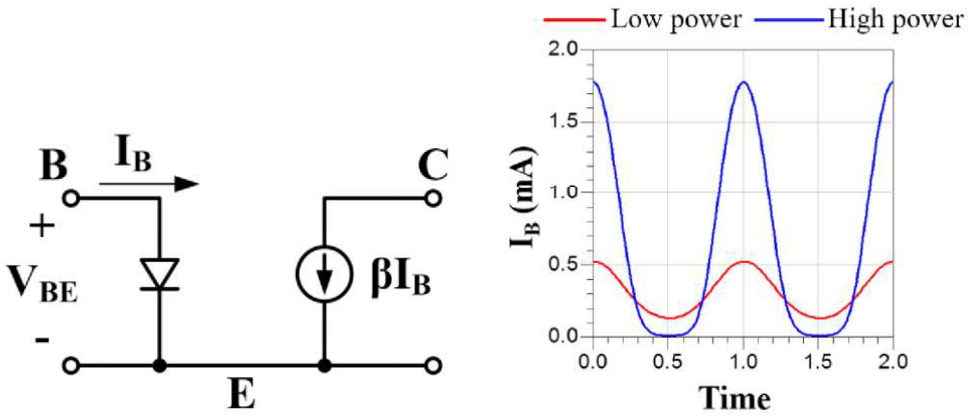
2.1.1-c) Efficiency

Although the standards in wireless communications do not specify the efficiency requirement, efficiency is also an important parameter in PA design. In a low efficiency PA, mostdc power consumption from power supply is transformed to the heat in chip instead of the output power.Since PAdominatesthe DC power consumption in theRF transceiver, the low efficiency PA significantly limitsthe battery lifeof mobile terminals. In addition, a decrease of PA efficiency increasesthe operation temperature of chip and decreases the reliability of the whole RF transceiver.Therefore, PAs shouldbe designed to have high linearity and high efficiency at the same time.Power-added efficiency (PAE) is a metric for rating the efficiency of a power amplifier that takes into account the effect of the gain of the amplifier. In this work, PAE is utilized to evaluate the efficiency performance of PA.

2.1.2 Review of reported PA ICs

Before the review of previously reported the PA ICs, an important distortion phenomenon of Heterojunction Bipolar Transistor(HBT) under high input power is introduced, which is employed to analyze the characteristics of difference bias circuits.

The Figure 2-2(a) shows a simple large signal model of HBT. When the input power increases, the base current (Ib) in the base-emitter diode of the RF HBT is rectified, as shown in Figure 2-2(b). Hence, the dc component of Ib increases and the input resistance of HBT base decreases with input RF power increassing.



(a) (b)

Figure 2-2. (a) Simple large signal model of HBT and (b)time domain waveforms of HBT base current with input power increasing.

The conventional current mirror bias circuit for the HBT PA was widely used ([5]-[9]) and is shown in Figure 2-3. A single-stage PA with current mirror bias circuit is designed and simulated in 350-nm SiGe BiCMOS to show its drawbacksand to compare with other topologies.The HBT is composed ofunits with emitter finger length of 20 μm, finger width of 0.8 μm and emitter stripes of 3. The RF amplifying HBT Q1 contains 48 units and the bias current mirror HBT Q2 contains 1 unit, respectively. R_{bias} is designed to 625 Ω for an appropriatebias current. For an accurate current copy, the base input resistance of Q1 and Q2 should be inversely proportional to the emitter size. Thus, the base bias resistor of Q1 and Q2 are designed to be R_{b1}=100 Ω and R_{b2}=4800 Ω, respectively. The output impedance transformation network is designed by load-pull simulation. The input matching network transforms the impedance of RF HBT to the system characteristic impedance (50 Ω). For simplicity, the input and output matching circuit is not shown. The supply voltages for the bias circuit and RF HBT are 3.3 V.

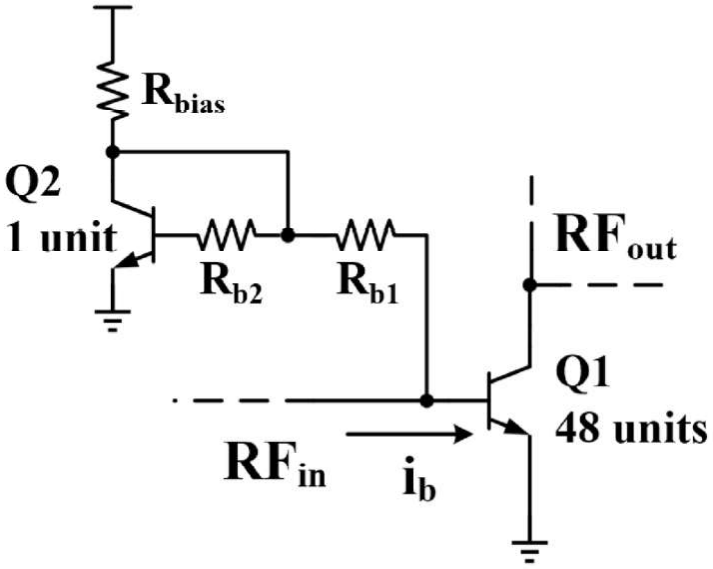
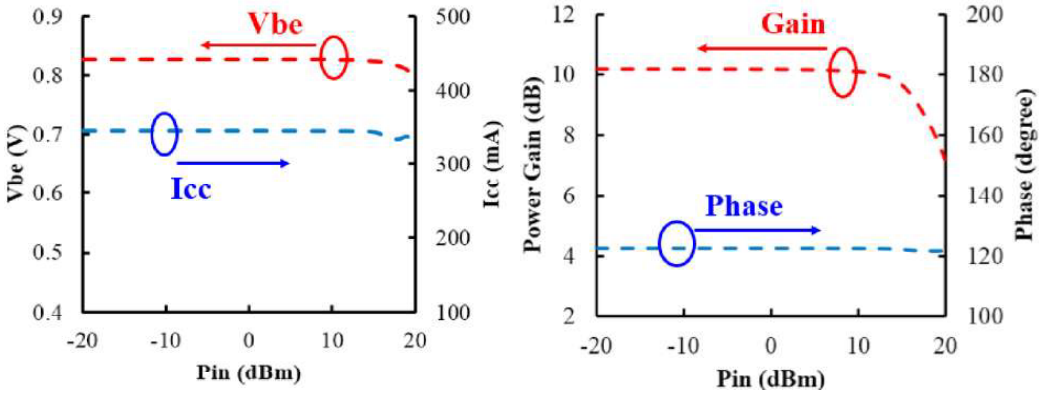


Figure 2-3. Schematic of the conventional current mirror circuitin [5]-[9].

In the PA with conventional current mirror bias circuit in Figure 2-3, when RF power increases, the input resistance of Q1 base and the base-to-emitter voltage (Vbe) of Q1 decreases. Figure 2-4(a) shows the simulated V_{be} and collector current (I_c) varication with RF powerincreasing from -20 to 20 dBm. Since the Vbe decreases with input power increasing, Vbe is high under the low input power, which causes a high quiescent bias current and low efficiency of PA at small signal. In addition, When Pin increases, gain compression is large as a result of Vbe decreasingas shown in Figure 2-4(b),which may cause the degradation of EVM.



(a) (b)

Figure 2-4.Simulatedperformance of PA with current mirror bias circuit: (a) V_{be} and I_b variation and (b) LSSPresponse with RF power increasing.

A great deal of works were devoted to improve the linearity and efficiency of PAs,

adaptive bias circuits were reported to increase the base current (Ib) of the RF HBT to maintain enough output current swing and to improve linearity as the input power increases.

The adaptive bias circuits using HBT base-collector junction diode as alinearizer was reported in [10]as shown in Figure 2-7(a). The RF amplifying HBT Q1, input and output matching circuits are the same as thosein Figure 2-3. The Rbias provides a suitable quiescentIb bias for Q1. The supply voltages for the bias circuit and RF HBT are 1.6 and 3.3 V, respectively.

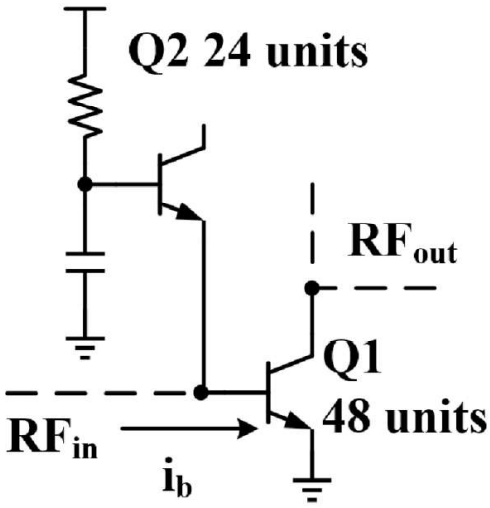
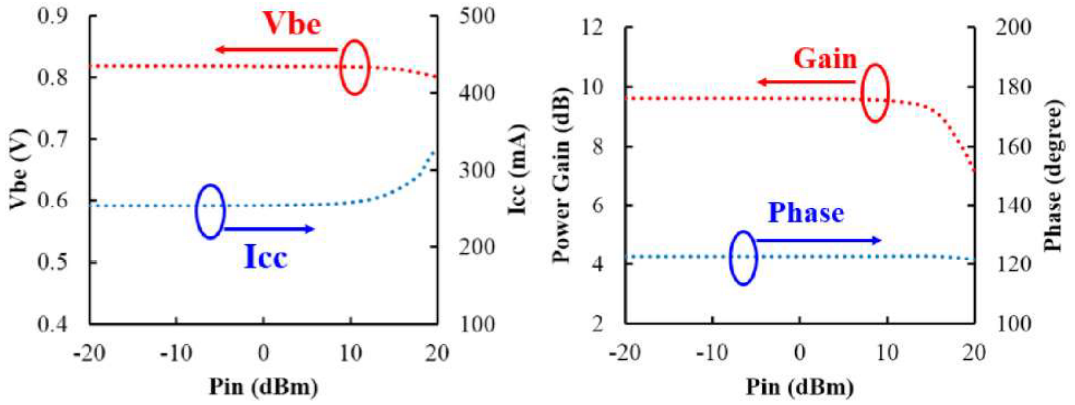


Figure 2-5. Schematic of linearized HBT PA with diode bias circuit as adaptive bias circuit reported in paper[10].

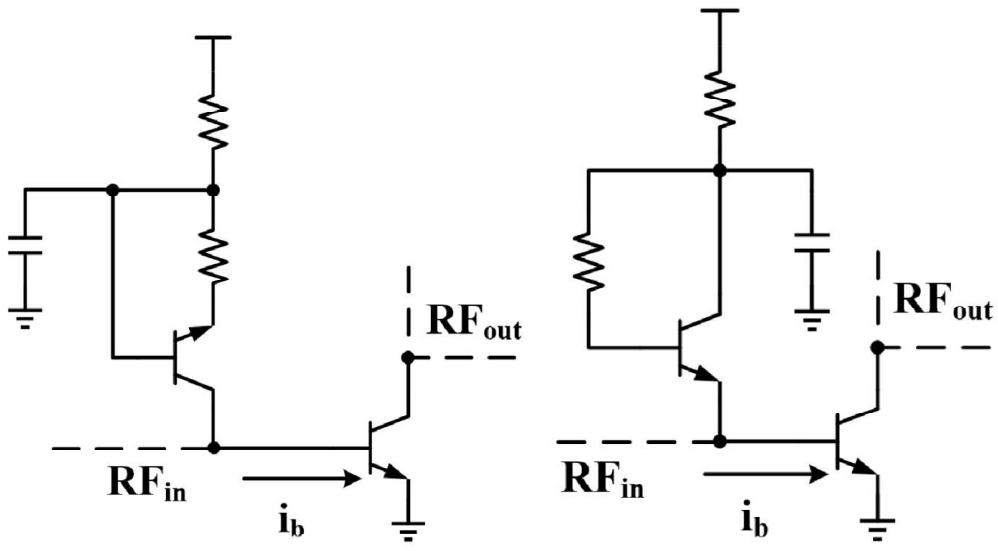
As the input power increases, the current of diode is rectified and the dc voltage across the diode decreases, whichincreases the Ib bias of Q1. Figure 2-6shows the simulated (a) RF HBT V_{be} and I_c varication, and (b) LSSP response of PA with RF power increasing from -20 to 20 dBm.Compared to the simulated performance of the current mirror biased PA in Figure 2-4, the diode linearizer providedhigher Ic bias and suppressedthe gain compression and phase distortion at high RF input power. However, since the driving ability of diode is limited, the diode size was large and the linearizer bias circuit did not provide sufficient bias current and Vbe of RF amplifying HBT still slightly decreasedathigh input RF power.In addition, the Rbias suppressed the increase of Ic in the RF HBT. Thus,Rbias in the bias circuits should not be too high, which limited the flexibility of Vbias and resulted indifferent voltages for bias circuit and power supply.



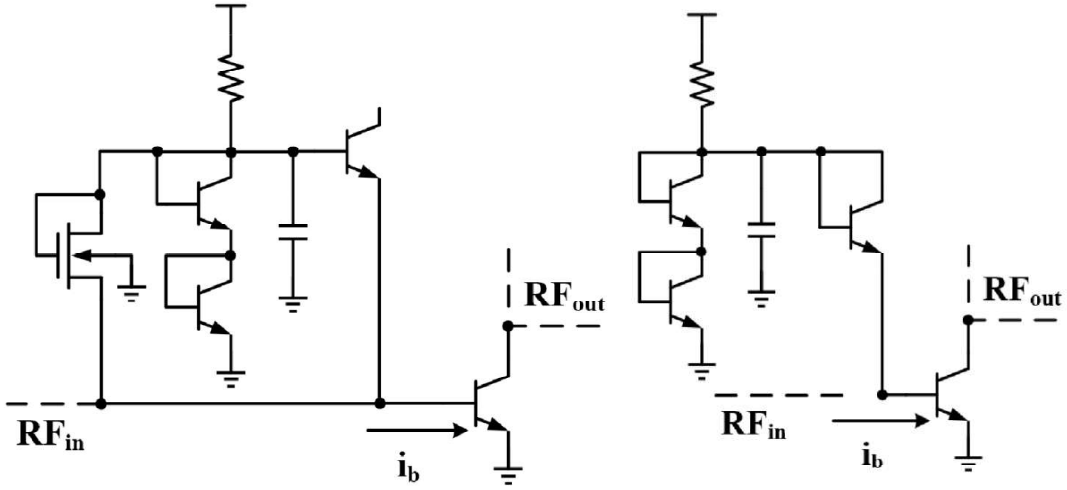
(a) (b)

Figure 2-6. Simulated performance of PA with diodelinearizerbias circuit: (a) Vbe and Ib variation and (b) LSSPresponse with RF power increasing.

Other adaptive bias circuits using HBT base-collector junction diode as linearizers were reported in [11]-[14]as shown in Figure 2-7(a)-(d). Paper [11]reported base-collector junction diode in the bias circuit to realize linearizer, as shown in Figure 2-7 (a).Paper [12]reported base-emitter junction diode in the bias circuit to realize linearizer, as shown in Figure 2-7(b). Paper [13]reported a linearizer including a base-emitter junction diode of an open collector HBT and a feedback MOS in diode connection, as shown in Figure 2-7(c). Paper [14]reported a linearizerapplying a base-emitter junction diode, as shown in Figure 2-7(d).The bias circuitsin [13]and [14] utilized two series NPN HBT in diode connectionto determine the Vbe bias of the RF amplifying HBT and to decrease the fluctuation of quiescent currentover PVT variation.



(a) (b)



(c) (d)

Figure 2-7. Schematic of linearized HBT PA with diode linearizer bias circuit reported in paper (a)[11], (b)[12],(c) [13], and (d)[14].

This paper presents a novel CMOS active bias circuit topology ([1],[2]) with strong DSC and excellent linearity improvement. Acommon source feedback amplifier is used to control the output voltage of the bias circuit. The novel bias circuit can effectively keepVbe of RF HBT constant, increase Ib, and flatten the gain of the PA as the input power increases.

2.1.3 350-nm SiGe BiCMOS process

Several types of semiconductor technologies such as Si CMOS, GaAs HBT/HEMT and SiGe HBT have been used to design RF PAs. AlthoughSi CMOS is the most cost-effective process, it has low linearity characteristics. GaAs has high power density and excellent linearity. However, the high cost limits its commercial applications. SiGe BiCMOS process can balance this trade-off with higher performance than Si CMOS and lower cost than GaAs, and SiGe BiCMOS process is fully compatible with the Si CMOS process. Hence, SiGe BiCMOS process is a good candidate to design PAs for WLAN applications. In this work, IBM 350-nm SiGe BiCMOS processis utilized to realize the linear PA IC.

Figure 2-8shows the cross section of the high-speed NPN HBT (Heterojunction Bipolar Transistor) based on thenon-self-aligned emitter-base integrationin this 350-nm SiGe BiCMOS process,where LTE epi is the Low-Temperature Epitaxy[15].

This process provides the high-performance and high-breakdown NPN HBTs by optional selectively implanted collector (SIC) mask [16]. Thetypical specifications of high-performance and high-breakdown HBTs are shown in Table 2-2, where BVceo is the collector-emitter breakdown voltage of HBTwith base open, f_T and f_{MAX} are the cut-off frequencyand maximum osculation frequency of the NPN HBT, respectively.

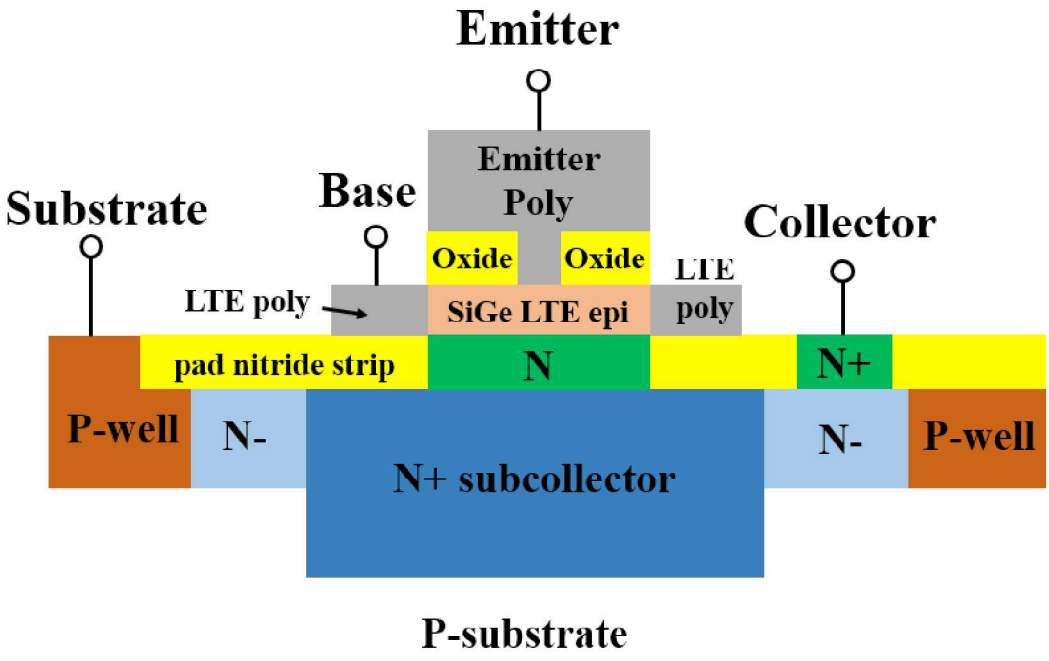


Figure 2-8. The cross section of the IBM NPN HBT in the 350-nmSiGe BiCMOS process.

Table 2-2 Typical specifications of the SiGe NPN HBT (25 °C)

	BV_{CEO} (V)	*ft* (GHz)	*fmax* (GHz)	β_F	Emitter size (μm^2)
High-breakdown HBT	8.5	27	≈ 90	100	0.8×20

The forward current gain of the common-emitter HBT (β_F) is defined as: β_F=Ic/Ib. For Indcsimulation, the Forward Gummel Curves with collector short base (Vbc = 0 V) could beapplied to evaluate the quality of the emitter-base junction of HBTand estimate β_F. β_F reaches the highest value and is almost constant in the mid-current region. In the low-current region, the increase of Ib and the drop in β_F are caused by the recombination of carriers at the surface and in the emitter-base space-charge layer, and

the formation of emitter-base surface channels [17]. In the high-current region, the decrease of Ic and the drop in β_F are caused by the saturation, the effect of high-level injection andKirk effect [5].

With a peakf_T and f_{MAX} of 27GHzand around 90 GHz, the high-breakdown NPN HBT can well cover full frequency band of IEEE 802.11a standard. Therefore, the high-breakdown HBT with higher BVceois applied to implement the PA IC with higher supply voltage and output power.

This process includes 4 metal layers and the thickness of the top layer is around 4 μm to realize high Q-factor inductors. In addition, through silicon via (TSV) technology is employed, which can effectively reduce parasitic resistance and inductance. Especially, the decrease of HBT emitter inductance by employing TSV is expected to improve the power gain of SiGe HBT PA IC. Moredetails of this process are described in [16].

2.2 Operation principle

2.2.1 Adaptivebias circuitwith voltage regulation

Figure 2-9illustrates the simplified schematic diagram of the novel linearizing CMOS bias circuit proposed in this paper.This novel bias circuit works like a regulator. When the input power increases,the novel bias circuit keeps V_{be} constant and sufficiently increases I_b to improve the linearity. For DC analysis of the novel bias circuit, input resistance of RF amplifying HBT is simplified to resistor R_{be}.

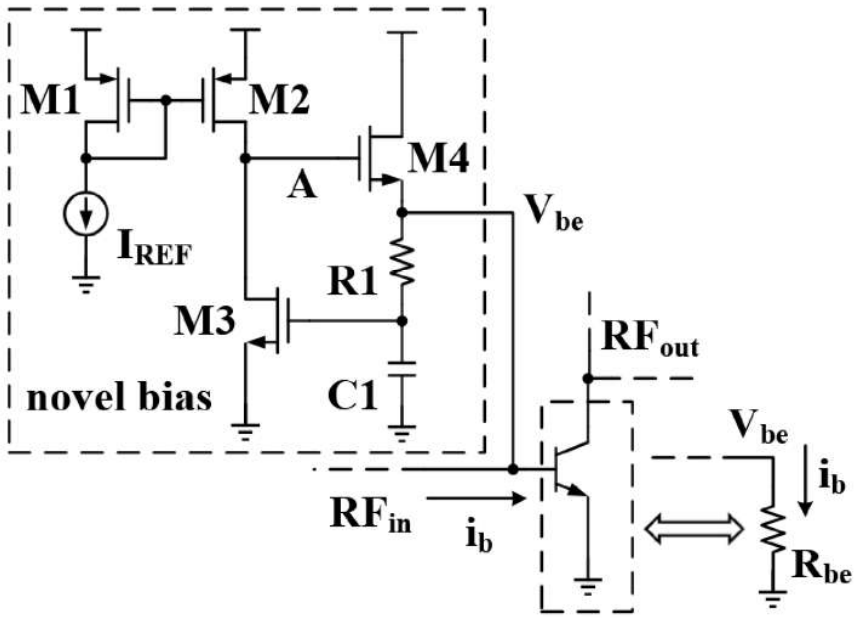


Figure 2-9. Schematic of PA with novel linearizing bias circuit.

Resistor R1 and capacitor C1 form a low pass filter to isolate MOS transistor M3 from the RF input. MOS transistors M1 and M2 and current source I_{REF} form a current mirror to supply the drain current of M3 (I_{D3}).

At first, channel length modulation effect is neglectedto estimate output voltage (V_{be}) of the novel bias circuit.The potential of node A (V_A) is floating and has no influence on I_{D3}. I_{D3} is only decided by the gate-to-source voltage of M3 (V_{GS3}), which equals to V_{be}. Therefore, the output voltage of the bias circuit can be expressed as:

$$V_{be} = V_{TH3} + \sqrt{\frac{2I_{REF}W_2L_1L_3}{\mu C_{OX}W_1W_3L_2}} \tag{2-3}$$

where W1, W2, W3 and L1, L2, L3 are the total gate widths and gate lengths of M1, M2 and M3, respectively. V_{TH3} is the threshold voltage of M3, μ is the carrier mobility, and C_{OX} is the gate oxide capacitance per unit area.

It is noticed that V_{be} is independent on R_{be}, which is the most important feature of the novel bias circuit. To provide a more intuitive explanation, when R_{be} decrease, V_A will increase to increase I_b and to keep V_{be} constant. The gate widths and gate lengths of the transistorsand I_{REF} are optimized to supply a sufficient V_{be} bias for the RF HBT. In the equation (2-3), V_{be} is influenced by V_{TH3}. Since the concentration in this paper is the improvement of linearity, an additional compensated circuit might be necessary in the bias circuit to suppress the influence of V_{TH} on V_{be}.

The next step is considering the channel length modulation effect to analyze the DSC of the novel bias circuit and to optimize the device parameters. If V_{GS3} slightly decreases, V_A will significantly increase to decrease I_{D2} and to get a new balance of $I_{D2} = I_{D3}$. Hence, M1, M2, M3 and I_{REF} form an open-loop common source feedback amplifier, and the novel bias circuit can be simplified to the equivalent circuit as shown in Figure 2-10.

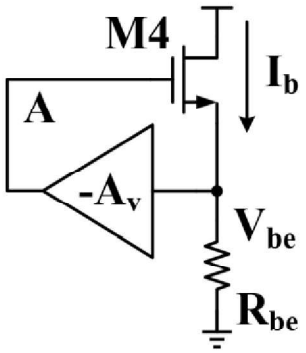


Figure 2-10. Equivalent circuit of the novel bias circuit.

Small signal analysis is applied to calculate how the variation of R_{be} affects V_{be}. It is assumed that R_{be} changes to $R_{be}+\Delta R_{be}$ and V_{be} changes to $V_{be}+\Delta V_{be}$. Since the feedback amplifier has an input voltage variation of ΔV_{be}, the output voltage variation of amplifier at node A is $-A_V \cdot \Delta V_{be}$, where A_v is open-loop gain of the amplifier. The V_{GS} variation of M4 (ΔV_{GS4}) is $-A_V \cdot \Delta V_{be} - \Delta V_{be}$. Thus, the variation of I_b can be expressed by:

$$\Delta I_b = \frac{V_{be}+\Delta V_{be}}{R_{be}+\Delta R_{be}} - \frac{V_{be}}{R_{be}} = g_{m4}(-A_V \cdot \Delta V_{be} - \Delta V_{be}) \quad (2\text{-}4)$$

where g_{m4} is the transconductance of M4. Therefore, the derivative of V_{be} with respect to R_{be} is:

$$\frac{\Delta V_{be}}{\Delta R_{be}} = \frac{V_{be}}{R_{be}[1+g_{m4}R_{be}(A_V+1)]} \quad (2\text{-}5)$$

Considering a typical value of $g_m \approx 10$ mS, $A_V \approx 40$ dB, and $V_{be} \approx 0.8$ V, when $R_{be} > 100\ \Omega$, $\Delta V_{be}/\Delta R_{be} << 1$. It means that ΔV_{be} keeps almost constant when R_{be} changes. From Eq. (4) it is inferred that $\Delta V_{be}/\Delta R_{be} > 0$ and $\Delta V_{be}/\Delta R_{be}$ increases as R_{be} decreases. Thus, V_{be} slightly decreases with the increase of R_{be}.

DSC of the novel bias circuit can be derived from equation(2-4)as:

$$\frac{\Delta I_b}{\Delta V_{be}} = -g_{m4}(A_V + 1) \quad (2\text{-}6)$$

Therefore, g_{m4} and A_v should be designed to a large value to increase the DSC of the bias circuit and to improve the linearity of PA. L_2 and L_3 areincreased to suppress the channellength modulation effect. Meanwhile, W_2 and W_3 should be proportionally increased to keep W_2/L_2 and W_3/L_3 constant. Therefore, V_{be} is constant and A_v is increased. Since V_{be} is independent on M4 parameters, gate width of M4 is increased to enhance g_{m4} without influencing V_{be}.Consequently, the device parameter is optimized to: L1 = L2 = L3 = L4 = 0.5 μm, W1 = 100 μm, W2 = 10 μm, W3 = 40 μm, W4 = 400 μm, R1 = 5 kΩ, and C1 = 10 pF. Although W4 is large for the DSC improvement,the area of the transistor with finger structure is insignificant compared with the inductors and capacitors.

Figure 2-11shows the variations of V_{be} and I_b with R_{be} from the dc simulation. When R_{be} is swept from 20 to 1000 Ω, I_b largely decreases from 39 to 0.8 mA, while V_{be} slightly increases from 0.78 to 0.8 V. The simulation results show good consistency with the theoretical analysis.

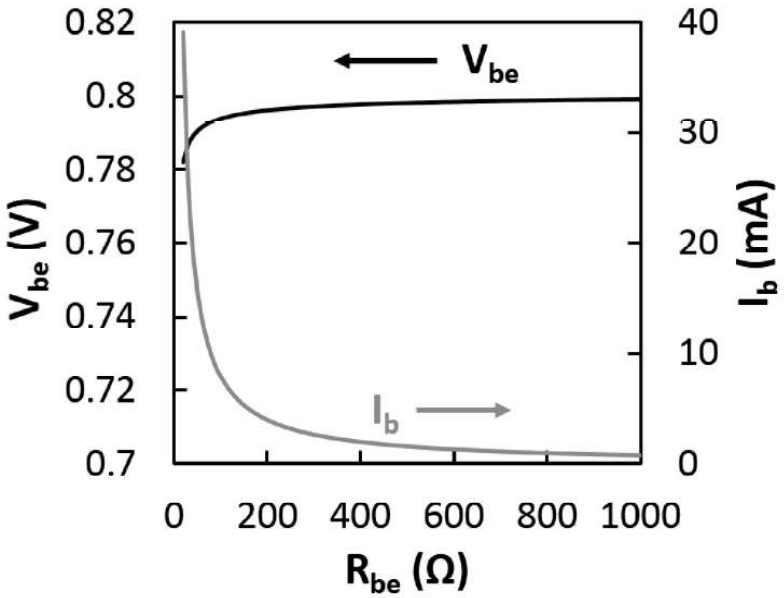


Figure 2-11. Simulated dependence of V_{be} and I_b on input power of the linearized PA (solid lines)and the conventional PA (dashed lines).

The stability of the regulator bias circuit is confirmed from the open-loop gain of the feedback loop.Figure 2-12shows the schematic to simulate theopen-loop gain by ac simulation. An infinitely large ideal inductor asRF choke and an infinitely large ideal capacitorfor dc cut are inserted to make to feedback loop open for ac signal

without influencing the dc operations point of the bias circuit and RF HBT.

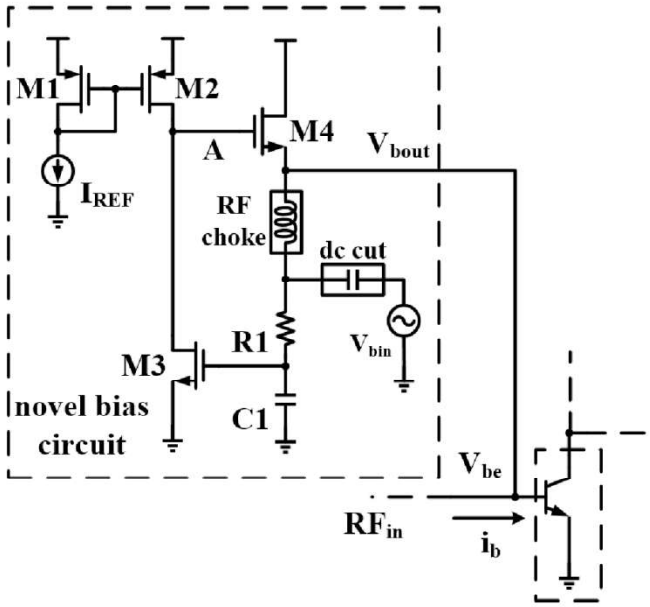


Figure 2-12. Schematic to simulate the open-loop gain of the regulator.

As shown in Figure 2-12, Vbin with 1mV amplitude is inserted as the input voltage, Vbout is open-loop output voltage of the bias circuit. The open-loop gain of the bias circuit is defined as:

$$Gain = 20 * \log(\frac{V_{bout}}{V_{bin}}) \tag{2-7}$$

and the open-loop phase shift of the bias circuit is defined as:

$$Phase = Phase\ (V_{bout}) - Phase\ (V_{in}) \tag{2-8}$$

Figure 2-13shows the Bode magnitude plot and Bode phase plotof the regulator bias circuit with Vbin frequency swept from 1 kHz to 1 GHz. When the frequency is low, the gain is around 20 dB and the phase shift is 180 degree, which confirms the negative feedback of the loop and voltage regulation of the bias circuit. When frequency increases and the gain decreases to 0 dB, the phase shift is larger than 0 degree, which confirms the stability of the feedback loop.

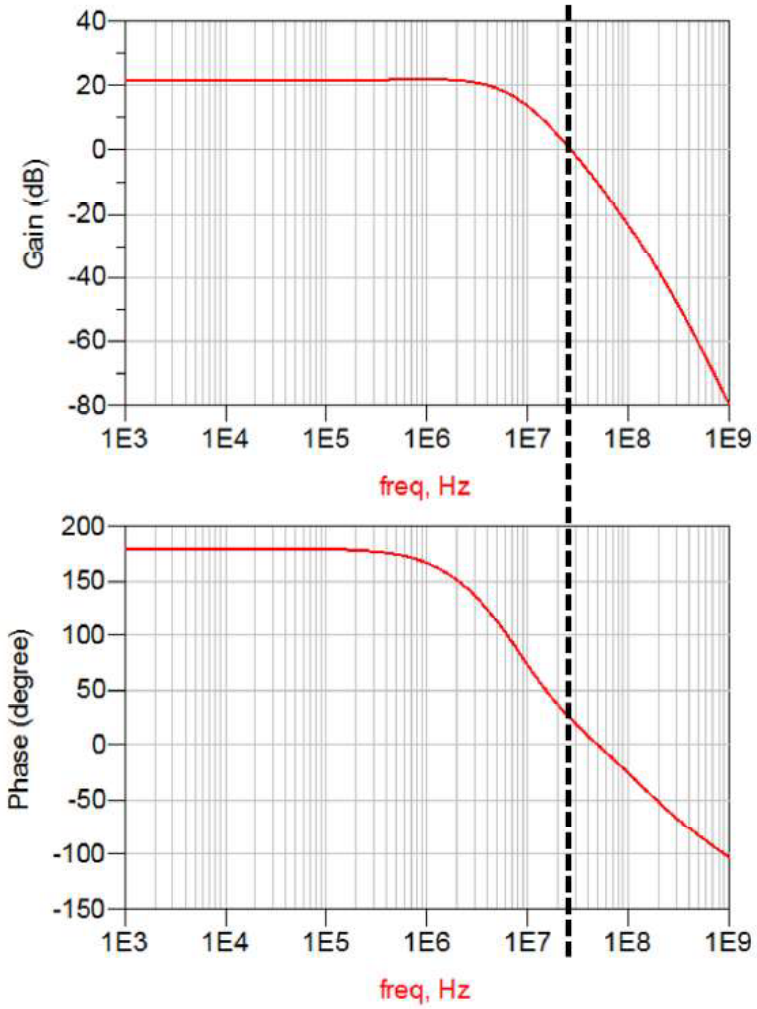


Figure 2-13. Bode plot of the open-loop gain of the regulator.

Harmonic balance simulation is performed to confirm the DC analysis and to compare the linearized PA in Figure 2-9with the conventional PAin Figure 2-3. Figure 2-14shows the simulated dependence of V_{be} and I_b on the input power swept from -20 to 20 dBm. In the conventional PA, I_b slightly increases from 1.2 to 1.4 mA and V_{be} significantly decreases from 0.798 to 0.541 V. In the linearized PA, I_b largely increases from 1.2 to 4.1 mA and V_{be} keeps almost constant (V_{be} changes from 0.798 to 0.796 V). Therefore, it is expected that the novel bias circuit is effective in improving the linearity of PA.

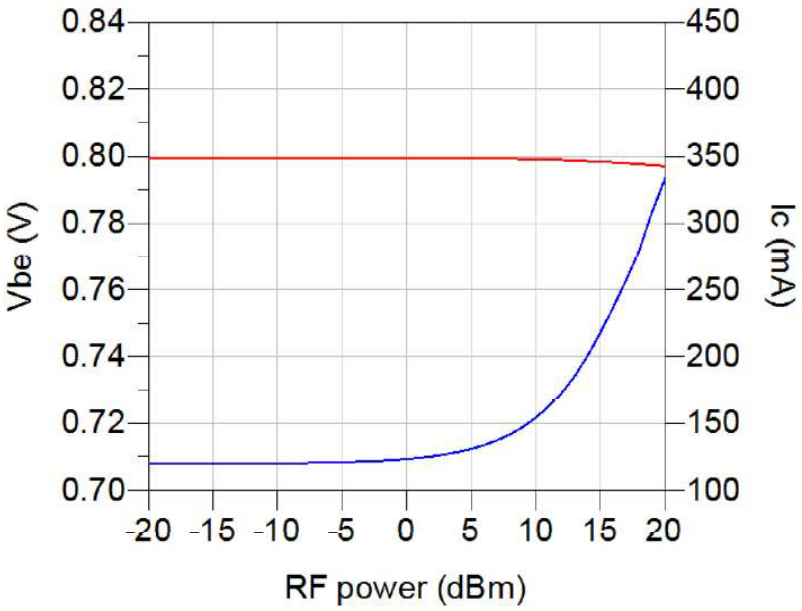


Figure 2-14. Simulated dependence of V_{be} and I_b on input power of the linearized PA (solid lines)and the conventional PA (dashed lines).

2.2.2 Decreaseof quiescent currentby the adaptivebias circuit

To furtherexplain the principle of the linearity improvement, the novel bias circuit is modeled as an RC shunt circuit as illustrated inFigure 2-15. R_{var} and C_p are the output resistance and capacitance of the bias circuit, respectively.

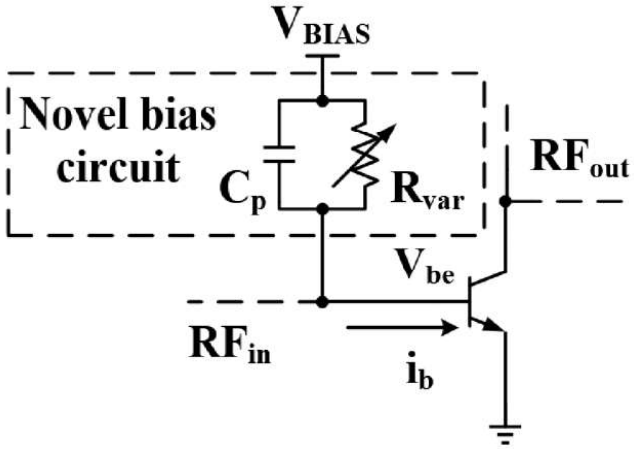


Figure 2-15. Schematic of PA with simplified model of the novel bias.

C_p can be derived from Figure 2-15as:

$$C_p = C_{DS4} + \frac{C_{GS4}(C_{DS2}+C_{DS3})}{C_{GS4}+C_{DS2}+C_{DS3}} \quad (2\text{-}9)$$

where C_{DS2}, C_{DS3} and C_{DS4} are the drain-to-source capacitances of M2, M3 and M4,

respectively, and C_{GS4} is the gate-to-source capacitance of M4. When the input power increases, C_{GS4} is slightly increased while C_{DS2}, C_{DS3} and C_{DS4} are almost constant. Since $C_{DS2}+C_{DS3}$ is smaller than C_{GS4}, the influence of C_{GS4} on C_p is insignificant. As the input power decreases, C_p can be regarded as constant, while R_{var} increases to keep R_{be}/R_{var} constant,ensure a constant V_{be} bias and decreases HBT bias current.

Figure 2-16shows the simulated input power response of Vbe and Icc in one-stage PA with current mirror bias circuit in Figure 2-3, with diode bias circuit in Figure 2-5 and with the proposed adaptive bias circuit in Figure 2-9. When RF input power increases from -20 to 20 dBm, novel bias circuitkeeps Vbe bias of HBT constantand sufficiently increases the collect bias current. The quiescent current consumption (Icq) of PA with novel biascircuit is ONLY 35% Icq of CM biased PA and 47 % Icq of diode biased PA.

Figure 2-17shows the simulated LSSP performance of one-stage PA with current mirror bias circuit in Figure 2-3, with diode bias circuit in Figure 2-5and with the proposed adaptive bias circuit in Figure 2-9.The OP1dB of PA with current mirror, diode and the proposed adaptive bias circuits are 25.4 dBm, 25.6 dBm and 26.3 dBm, respectively. The phase distortion at OP1dBof PA with current mirror, diode and the proposed adaptive bias circuits are 0.7°, 0.4°and 1.2°, respectively. Hence, PA with the proposed bias circuit has similar linearity with much lower quiescent current.

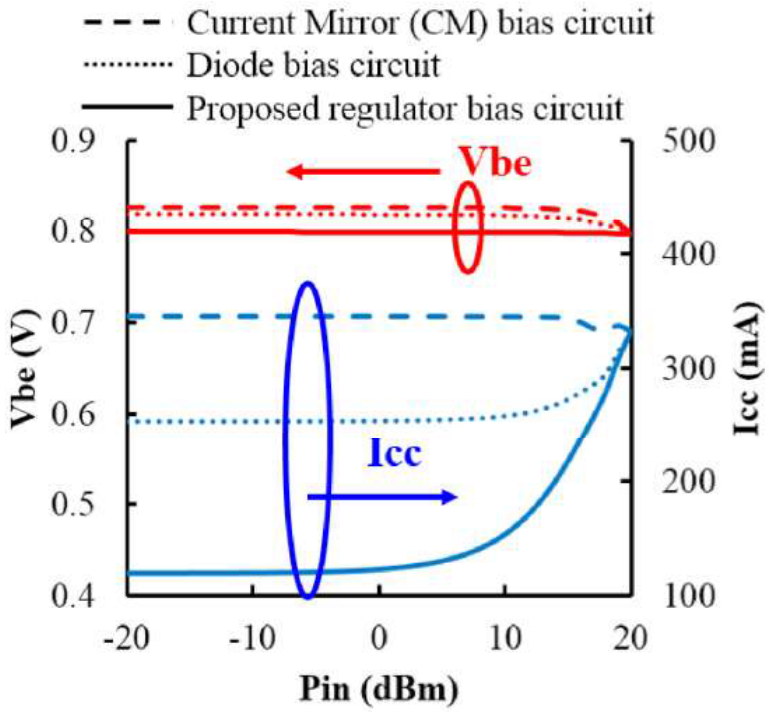


Figure 2-16. Simulated LSSP (S_{21} magnitude and phase response) of the linearized PA (solid

lines)and the conventional PA (dashed lines).

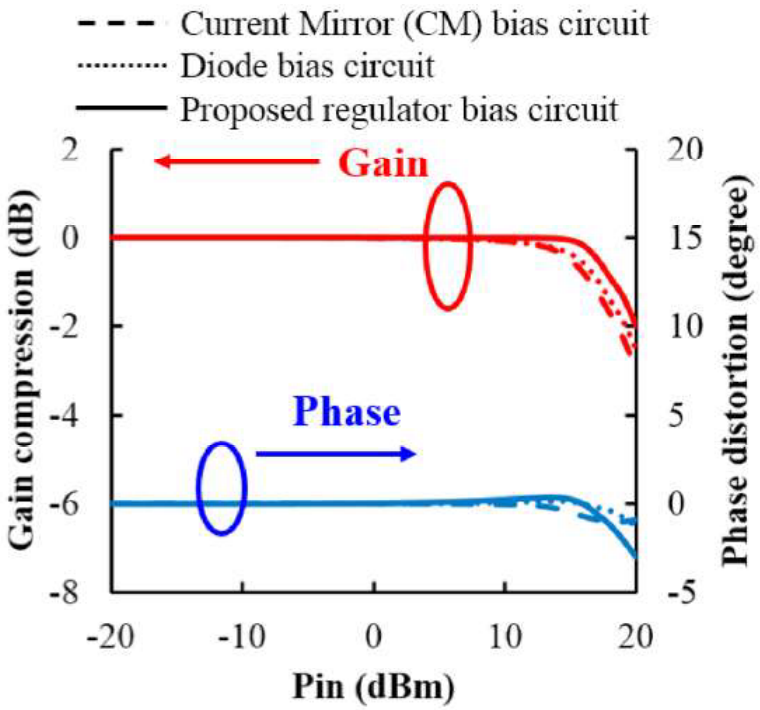


Figure 2-17. Simulated LSSP (S_{21} magnitude and phase response) of the linearized PA (solid lines)and the conventional PA (dashed lines).

2.3 Circuit design

2.3.1 Schematicof 3-stage PA IC

Figure 2-18illustrates the simplified schematic of a 3-stage PA IC for WLAN applications with the novel bias circuit. Since the breakdown voltage of the HBT is 8.6 V, the supply voltageof RF HBT (V_{cc}) is set to 4.2 V, and the supply voltageof novel bias circuit (V_{ref}) is set to 3 V for the suitable operation of MOS transistors. The PA IC is mounted on the PCB for measurement. The bonding wires (BW1, BW2 and BW3 in Figure 2-18) are inevitable in packaging and are incorporated in the design of matching network.

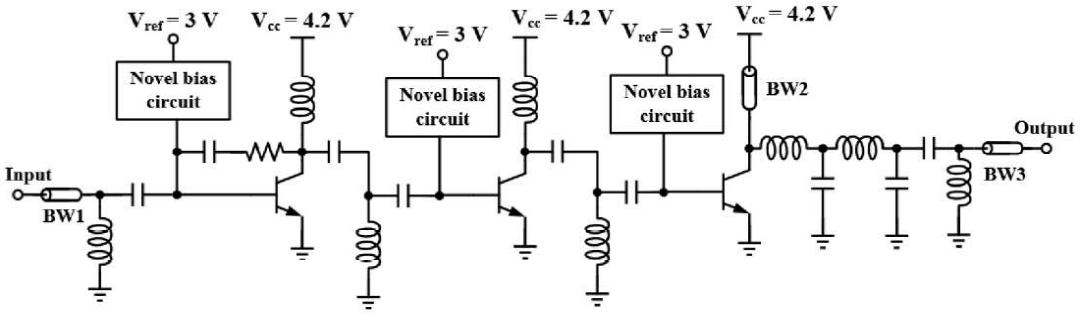


Figure 2-18. Simplified schematic of the 5 GHz-band 3-stage SiGe HBT PA IC with the novel biascircuit.

The RF HBT is composed of units with emitter finger length of 20 μm, finger width of 0.8 μm and emitter stripes of 3. Since the first stage and second stage work as the gain-stage amplifiers, a 2-unit HBT is applied for the first stage, and an 8-unit HBT is applied forthe second stage. To improve the stability of the PA, a resistive feedback is utilized at the first stage. Since the third stage plays the role of power-stage, a 96-unit HBT is applied.Gain compression may still occur in the gainstages with high input power due to the small emitter size of the RF HBTs. Hence, all the three stages employ the novel bias circuit to improve the linearity.

2.3.2 Simulated performance

Figure 2-19shows the simulated S-parameters of the 3-stage PA IC. In a frequency band from 4.5to 5.8GHz, the input and output return losses are better than 10 dB. The maximum small-signal gain is 30.5dB at 5.1GHz with 3 dB bandwidth from 4.6to 5.9 GHz.

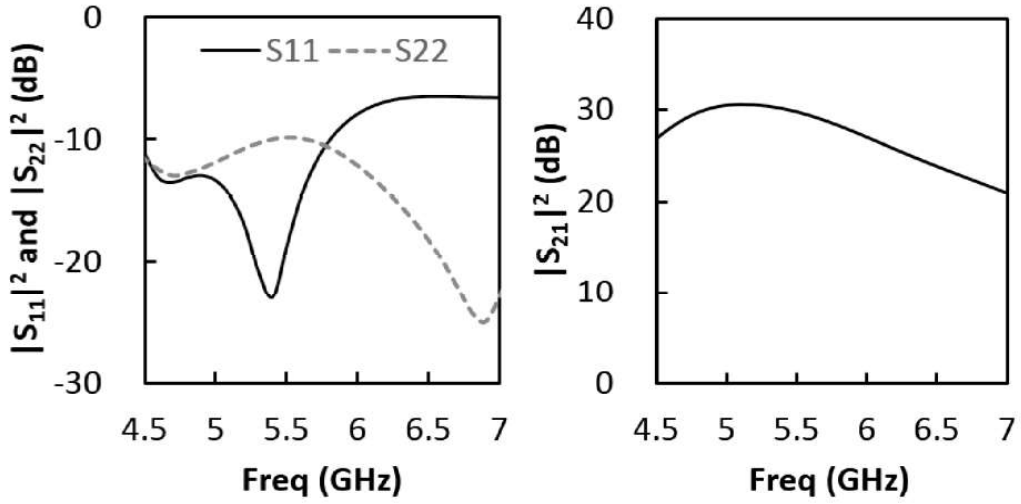


Figure 2-19.Simulated S-parameters of the 3-stage PA IC.

Figure 2-20shows the simulated dependence of LSSP performance (S_{21} magnitude and phase) on the input power at 5.4 GHz. The simulated input P1dB is -3.2 dBm and the output P1dB is 26.4 dBm with a phase distortion of 4.1 degrees.

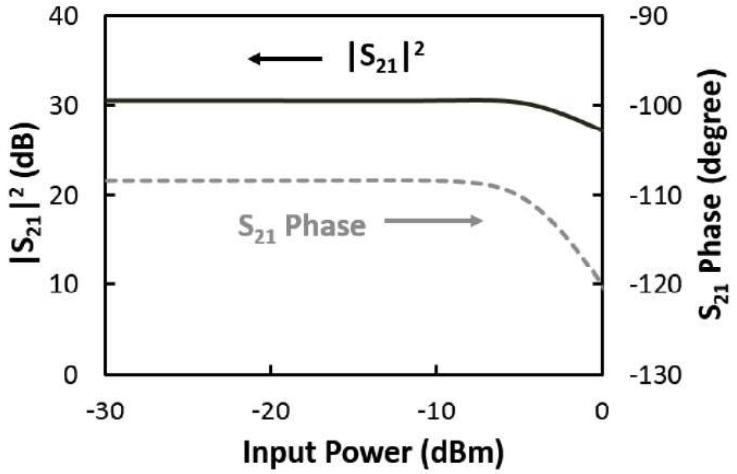


Figure 2-20. SimulatedLSSP (S_{21} magnitude and phase) response with the input power.

Figure 2-21shows the simulateddependence of the output power and Power Added Efficiency (PAE) on the input power under the continuous wave (CW) at 5.4 GHz. As the input power increases from -25 to 0 dBm, the output power increases from 5.1 to27.5 dBm and the peak PAEis 25.1%.

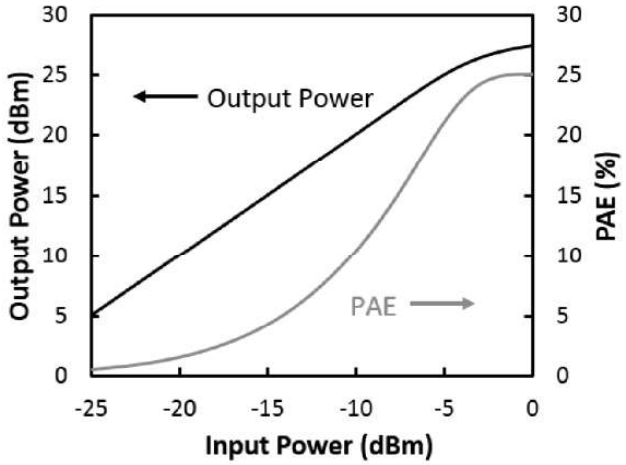


Figure 2-21. Simulated output power and PAE under the continuous wave at 5.4 GHz.

Figure 2-22shows the simulateddependence of the output power and PAE on the input power under the 54 Mbps OFDM signal at 5.4 GHz with a 20 MHz channel bandwidth. Small signal gain is 30.3 dB and the output P1dB is 24.3 dBm with the peak PAE of 22.9 %.

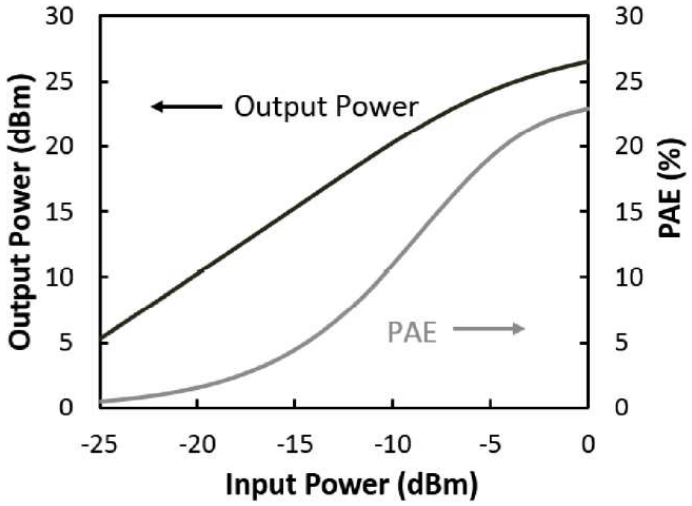


Figure 2-22. Simulated output power and PAE under the 54 Mbps OFDM signal at 5.4 GHz.

Figure 2-23shows the simulated Error Vector Magnitude (EVM) under the 54 Mbps OFDM signal at 5.4GHzwith a 20 MHz channel bandwidth. When the output power is lower than 21.2 dBm, the simulated EVM is better than 5%.

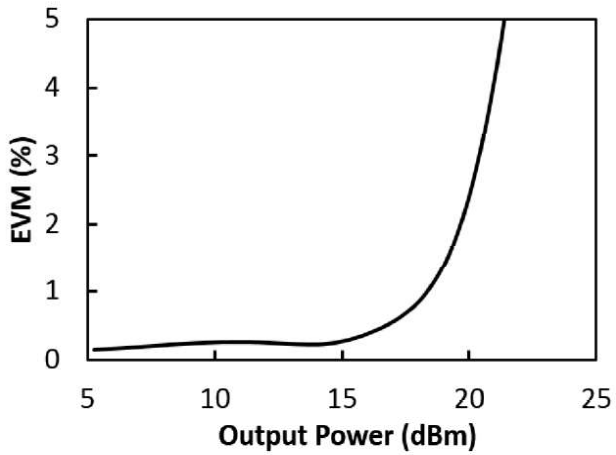


Figure 2-23. Simulated EVM vs. the output power under the 5.4 GHz 54 Mbps OFDM signal.

2.4 Measured performance

Figure 2-24illustrates the chip photograph of the 3-stage linearized PA IC with the novel bias circuit. The chip is fabricated inIBM 350-nm SiGe BiCMOS processand mounted on a PCB for testing. The chip size is 1.9 mm by 0.95 mm with a thickness of 100 μm.

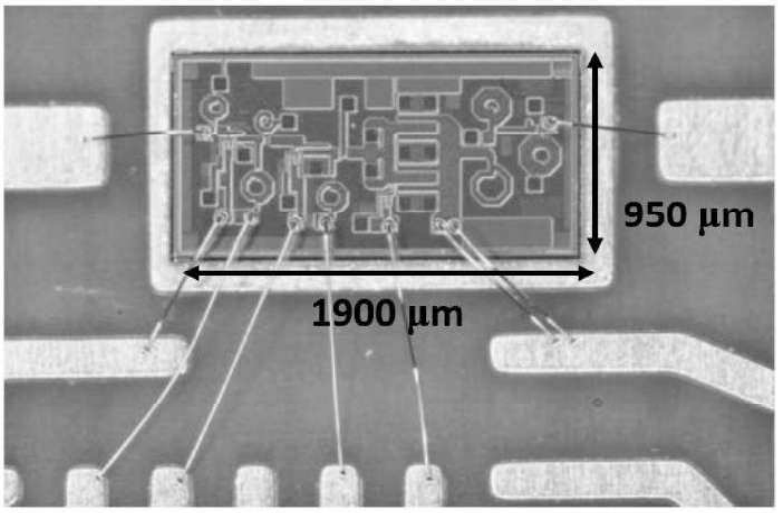


Figure 2-24. Photograph of the fabricated PA IC chip with an evaluation board.

Figure 2-25 depicts themeasured S-parameters of the 3-stage PA IC. In a frequency band from 4.9 to 5.9 GHz, the input and output return losses are better than 10 dB. The maximum small-signal gain is 29.2 dB at 5.2GHz with a 3 dB bandwidth from 4.9to 6.1 GHz. The measured frequency response of S_{21} is slightly shifted to

higher frequency than the simulated onein Figure 2-19. It is considered that the inductance deviation of the bonding wires affect the impedance matching condition.

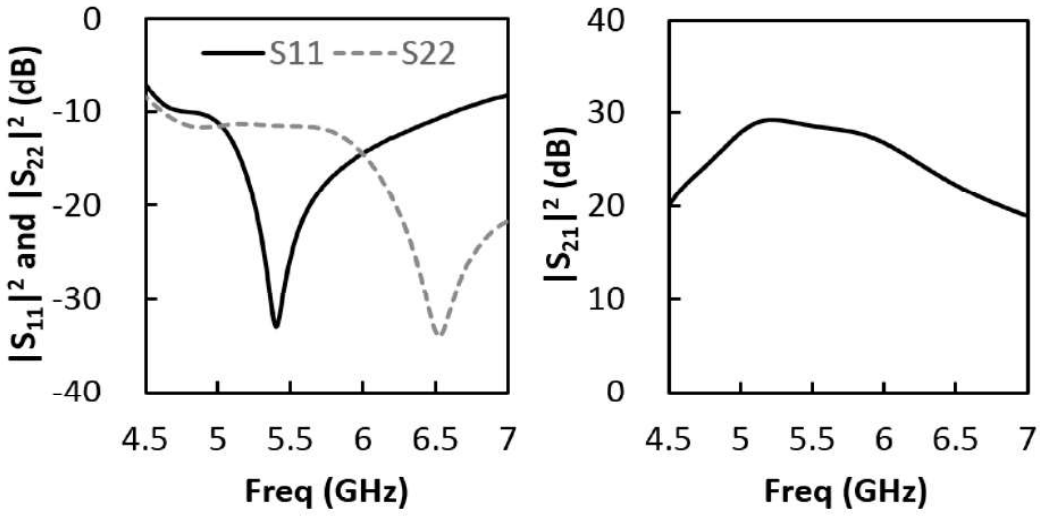


Figure 2-25.Measured S-parameters of the 3-stage PA IC.

Figure 2-26shows the measureddependence of output power and PAE on the input power under the continuous wave at 5.4GHz. The supply voltage is 4.2 V and the total quiescent current is 145 mA (9 mA for the first stage, 30 mA for the second stage and 106 mA for the third stage).The 3-stage PA IC exhibits an input P1dB of -0.5 dBm, an output P1dB of 26.7 dBm and a peak PAE of 20.7%. The measured linearitywell agrees with the simulated one in Figure 2-21. The measured PAE is slightly lower than the simulated one in Figure 2-21.

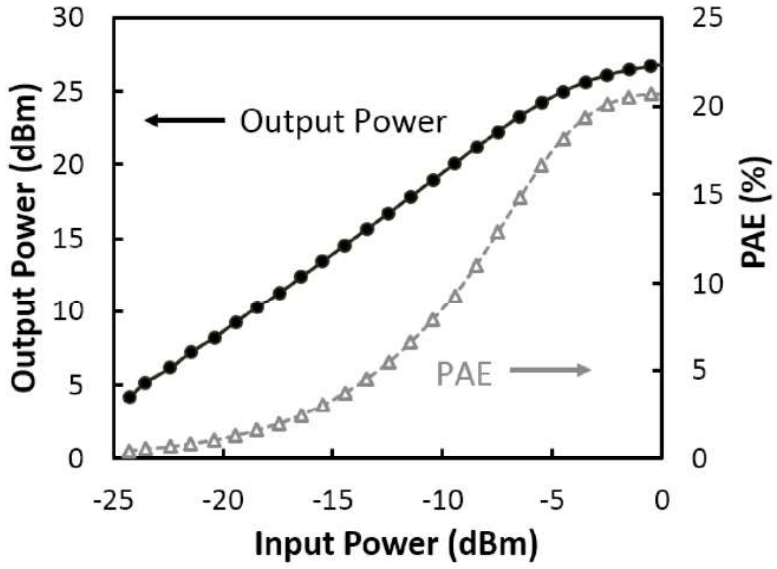


Figure 2-26. Measured output power and PAE under the continuous wave at 5.4 GHz.

Figure 2-27depicts the measureddependence of the output power and PAE on the input power under the 54 Mbps OFDM signalsat 5.4 GHz. Since the dynamic range of the OFDM signal generator for measurement was limited, the maximum input power to the PA IC was -5 dBm, which was lower than the input P1dBof the PA IC.

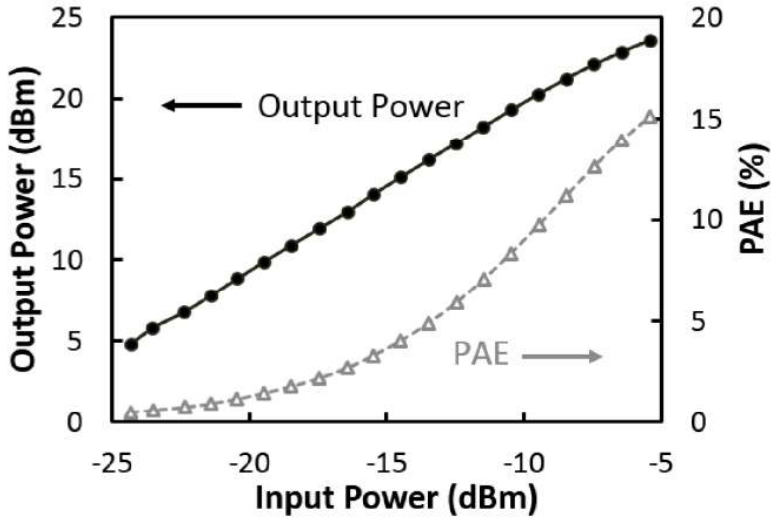


Figure 2-27. Measured output power and PAE under the 54 Mbps OFDM signal at 5.4 GHz.

Figure 2-28shows the measured EVM performance, which gives a comprehensive evaluation of the PA linearity performanceincluding gain compressionand phase distortion.The EVM measurement is performed under 54 Mbps OFDM signals at carrier frequencies of 4.9 GHz, 5.4GHz and 5.9 GHz. The measured EVMs are similar in the frequency range from 4.9 to 5.9 GHz. At 5.4 GHz, the PAIC exhibits a measured EVM of 0.9% (-40.9 dB) at an output power of 17 dBm, and that of 4.2% (-27.5 dB) at 20.3 dBm. Themeasuredperformancesunder54 Mbps OFDM signalswell agree with the simulatedresults as shown in Figure 2-22and Figure 2-23,and well meet the 802.11a WLAN standard.

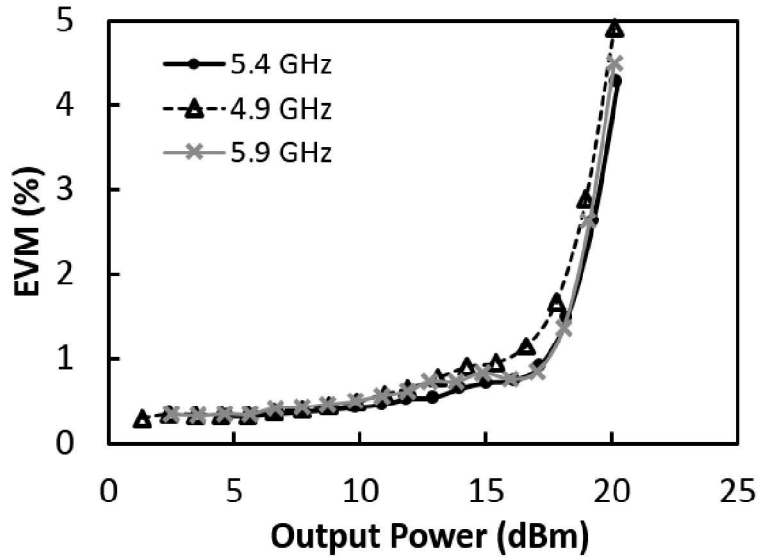


Figure 2-28. Measured EVM vs. the input power under the 5.4 GHz 54 Mbps OFDM signal.

Table I summarizes the measured performance of the linearized PA IC with previous works. Compared with the previous works [9]and [10]with similar frequency band and the same SiGe process, this work achieves higher output power and better PAE with similarEVM.

Table 2-3Summary of the Measured Performance of the PA IC with Previous Work

	Process	Freq (GHz)	Gain (dB)	CW OP1dB (dBm)	Modulation	Pout (dBm)	PAE (%)	EVM (%)
[9]	350-nmSiGe BiCMOS	5.3	31	N. A.	64-QAM 54 Mbps	16	7.8	3
[10]	350-nm SiGe BiCMOS	5	21.9	27.0	64-QAM 54 Mbps	16	6.0	2.7*
[18]	180-nmSiGe BiCMOS	5.9	27	N.A.	64-QAM 54 Mbps	11 18.3	3.5 15	3.2 5.6
This work	350-nmSiGe BiCMOS	5.4	29	26.7	64-QAM 54 Mbps	19.3 20.3	8.3 9.7	2.6 4.2

* The measured EVM without feedforward error amplifier is used for comparison

2.5 Conclusion

A 5-GHz band SiGe PA IC has been demonstrated with a novel linearizing CMOS bias circuit for WLAN application. With the utilization of an open loop common source feedback amplifier, the novel bias circuit works like a regulator with excellent DC sourcing capability. As the input power increases, the novel bias circuit well keeps the

V_{be} of RF HBT constant and largely increases the I_b for sufficient output current swing. The novel bias circuit can effectively improve linearity performance of the PA IC.

Under 54 Mbps OFDM signal at 5.4 GHz, the PA IC has achieved a measured EVM of 0.9% with 284 mA DC current consumption at 17 dBm output power, andan EVM of 4.2% with 330mA DC current consumption at 20.3 dBm output power. The measured linearity performance well satisfies the requirements of IEEE 802.11a WLAN standards.

The measured performance confirms the effectiveness of the proposed adaptive bias on improving the efficiency and linearity of PA. With higher efficiency, PA has lower power consumption with the same output power. Since PA is the most power consuming block in transceiver, it is expected that the proposed topology could decrease the total power consumption of transceiver IC.

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Chapter 3Low Voltage and Low Power CMOS VCO IC with an Amplitude Feedback Bias Circuit

3.1 Introduction

In Chapter 2, a high efficiency and high linearity PA IC with adaptive bias circuit for WLAN 802.11a applications has been demonstrated in 350-nm SiGeBiCMOS process.

In this chapter, alow voltage and low powerVCO IC is designed for 2.4-GHz applications[1]-[2]. As mentioned in Chapter 1, the 2.4-GHz band VCO IC is quite suitable for the application of IoT devices. Thus, decreasing the power supply of VCO could make it supplied with solar-cell battery orenergy harvesting system, which is an attractive solution for large distribution of IoT devices.Decreasing the power supply could also decrease the power consumption of VCO.

In addition to low voltage operation, low power operation is also important for the VCO design to increase the battery-life of IoT devices. Since the LC-VCO requires high bias voltage for oscillation start-upand a low bias voltage to maintain the low power oscillation,an amplitude feedback bias circuit is proposed for the VCO IC design. The amplitude feedback bias circuitis formed by a detector,a comparator, dc level shifters and buffer amplifiers. At the initial state, the proposed bias circuits provides the LC-VCO with high bias voltage for robust oscillation start-up. After the detector detects the oscillation, the proposed bias circuit adaptively decreases the bias voltage of LC-VCO to shift the oscillation into steady low power state. The circuit topologies of LC-VCO and amplitude feedback bias circuits are improved for ultra-low-voltage operation.

Alow voltage and low power VCOIC with the proposed adaptivebias circuit for 2-GHz band applications is designed,fabricated and fully tested in 65-nm CMOS process.

In this chapter, introduction is firstly given in Section 3.1, including the performance parameters of VCO, review of previous VCO ICs and brief descriptions of 65-nm CMOS process. The proposedregulator bias circuit is described in detail in Section 2.2, including working principle analysis andlinearity improvement to PA. Then in Section 2.3, athree-stage linear PA IC with the proposedbias circuit for 5-GHz band WLAN applications is presented with the circuit schematic and simulated

performance.In Section 2.4, measured performance is demonstrated with the comparison of previous works to confirm the effectiveness of the proposal.Finally, conclusions are given in Section 2.5.

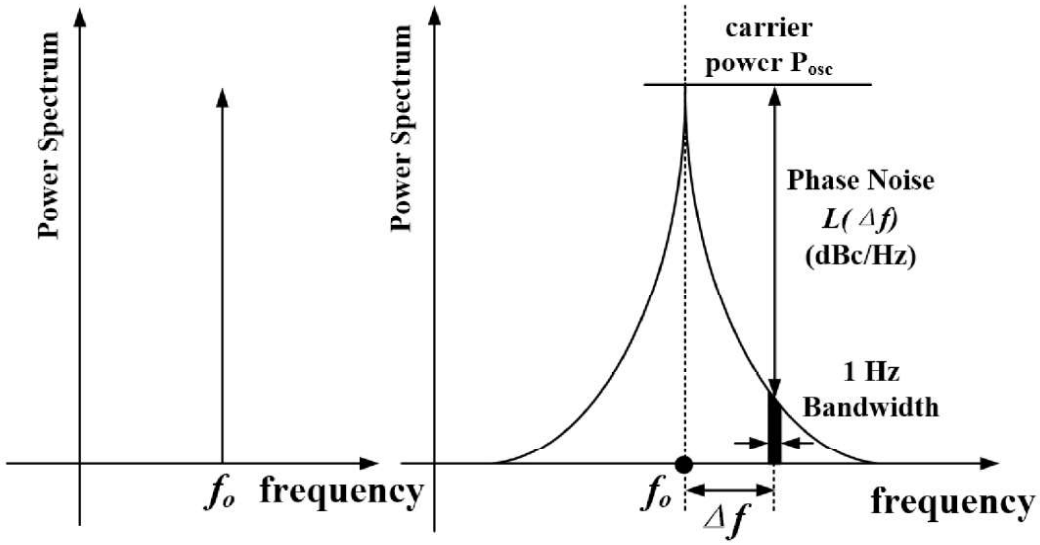
3.1.1 Performance parameters ofVCO

3.1.1-a) Phase noise

In an ideal oscillator,the oscillation frequency is constant with time variation and the carrier power in the frequency spectrum is a single impulse, as shown in Figure 3-1 (a), where the f_o refers to the oscillation frequency. In the actual case, the oscillation frequency is modulated by the noise in the elements and varies randomly. Thus the carrier power in the frequency spectrum is broadened, as shown in Figure 3-1(b). Phase noise is utilized to evaluate the "purity" of the output signal of the oscillator. Phase noise is characterized [3], as:

$$L(\Delta f) = \frac{P_n(\Delta f)}{P_{osc}} \tag{3-1}$$

where$Pn(\Delta f)$ is the spectral power in a 1Hz bandwidth atthe offset frequency (Δf) from the center frequency (fo), and Posc is the carrier power, which could be viewed as the peak of the spectrum, as shown in Figure 3-1(b).



(a) (b)

Figure 3-1. Carrier power spectrum of the (a) ideal and (b) noisy oscillator.

For simplicity, the noise in the resistor and the transconductance stage are linearly modeled as whitethermal noise currentsin the parallel connection,as shown in the

Figure 3-2.

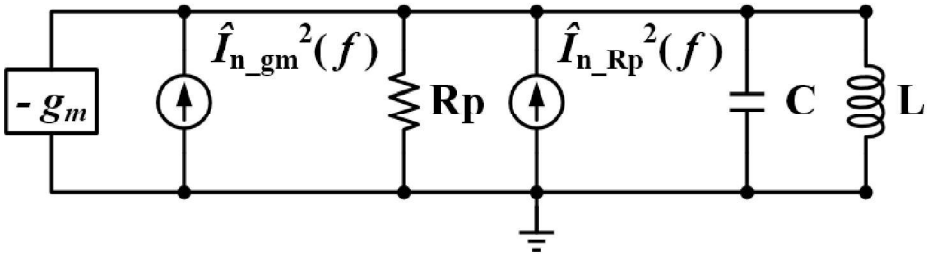


Figure 3-2. Linearnoise model of an oscillator.

The noise density is given by:

$$\hat{I}_{n\_gm}{}^2(\omega) = \frac{4kT}{R_p} \tag{3-2}$$

$$\hat{I}_{n\_Rp}{}^2(\omega) = 4kTg_m\gamma \tag{3-3}$$

where $\hat{I}_{n\_gm}$ and $\hat{I}_{n\_Rp}$ are the noise currentsin the resistor and the transconductance stage, respectively. γ is the noise figure of the transconductance stage. k is the Boltzmann constant with the values of 8.62×10^{-5} eV/K.T is the thermodynamic temperaturewith the unit of Kelvin.

The noise voltage of the oscillator at the frequency of $\omega+\Delta\omega$ iscalculatedas:

$$\hat{V}_n{}^2(\omega) = \left[\hat{I}_{n\_gm}{}^2(\omega) + \hat{I}_{n\_Rp}{}^2(\omega)\right] \times |Z(\omega_o + \Delta\omega)|^2 = kTR_p(1+\gamma)\left(\frac{\omega_o}{Q\Delta\omega}\right)^2 \tag{3-4}$$

where $Z(\omega_o+\Delta\omega)$ is the impedance at the offset frequency ($\Delta\omega=2\pi\Delta f$) from the center oscillation frequency ($\omega_o=2\pi f_o$).

The phase noise in (3-1)can be expressed as:

$$L(\Delta f) = \frac{\hat{V}_n{}^2(\omega)}{V_{osc}{}^2(\omega)} = \frac{\hat{V}_n{}^2(\omega)}{2R_pP_{osc}} = \frac{2kT(1+\gamma)}{P_{osc}}\left(\frac{\omega_o}{2Q\Delta\omega}\right)^2 \tag{3-5}$$

This is the famous Leeson's equation [4]. Figure 3-3 shows the typical independence of phase noise on the offset frequency with three region. In the ω^{-3} region from ω_{osc} to ω_1, phase noise is proportionalto the ω^{-3}, which shows a slope of 9 dB per octave. The flicker noise of the transistor (1/f noise) at low frequency is mixed with the oscillation signal and up-converted to the frequency near ω_{osc}, and caused the phase noise in this region.In the ω^{-2} region from ω_1 to ω_2, phase noise is proportionalto the ω^{-2}, which shows a slope of 6 dB per octave and is explained by Equation (3-5).As $\Delta\omega > \omega_2$, phase noise is flat and has norelationship with Δf, which is caused by the noise of buffer amplifier and noise floorof the measurement equipment. .

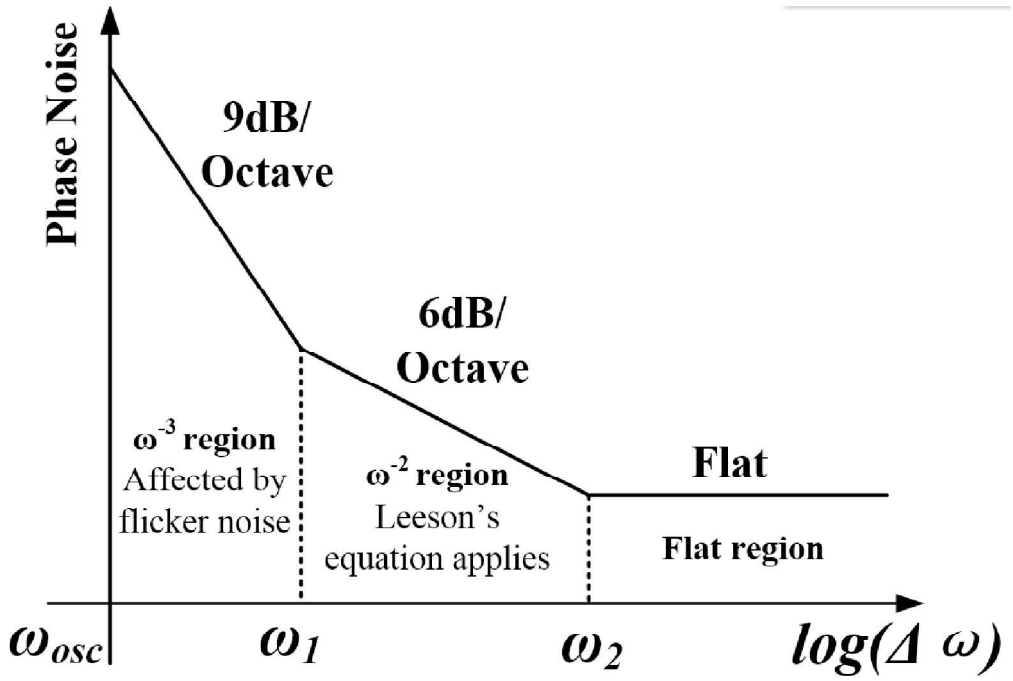


Figure 3-3. Typical phase noise in an oscillator vs. offset frequency.

Considering all these influence factors, Leeson improved the equation (3-5)to:

$$L(\Delta f) = 10 * \log\left(\frac{2FkT}{P_{osc}}\right) + 10 * \log\left[1 + \left(\frac{\omega_o}{2Q\Delta\omega}\right)^2\right] + 10 * \log\left(1 + \frac{\omega_1}{\Delta\omega}\right) \quad (3\text{-}6)$$

where F represents the noise from the transconductancestage in the ω^{-2} region, which is obtained by measurement. The number "1" in the polynomial $1 + \left(\frac{\omega_o}{2Q\Delta\omega}\right)^2$ refers to the floor noise in the buffer amplifier or measurement equipment. The polynomial $1 + \frac{\omega_1}{\Delta\omega}$ refers to the phase noise in the ω^{-3} region.

In Leeson's theory, ω_1 is the corner frequency of the flicker noise of transistor, and $\omega_2=\omega_{osc}/2Q$, respectively. Actually, ω_1 and ω_2 are not always satisfy this relationship. However, Leeson's model gives us plenty of guidelines to minimize the phase noise [5] such as: filtering the noise from the DC power and bias voltage, increasing the Q-factor of varactor and inductor, decreasing the flicker noise in the active elements (applying dc-offset cancelling technique, for instance), decreasing the noise figure of buffer amplifier and increase the carrier power at the output of the resonant tank.

3.1.1-b) Frequency tuning

The gain or of VCO (Kvco) are frequency tuning range (FTR) applied to describe the frequency tuning performance of VCO. Kvcois defined as:

$$K_{VCO} = \frac{\partial \omega_o}{\partial V_{ctrl}} \tag{3-7}$$

where V_{ctrl} is the control voltage of the varactor. FTR is defined as:

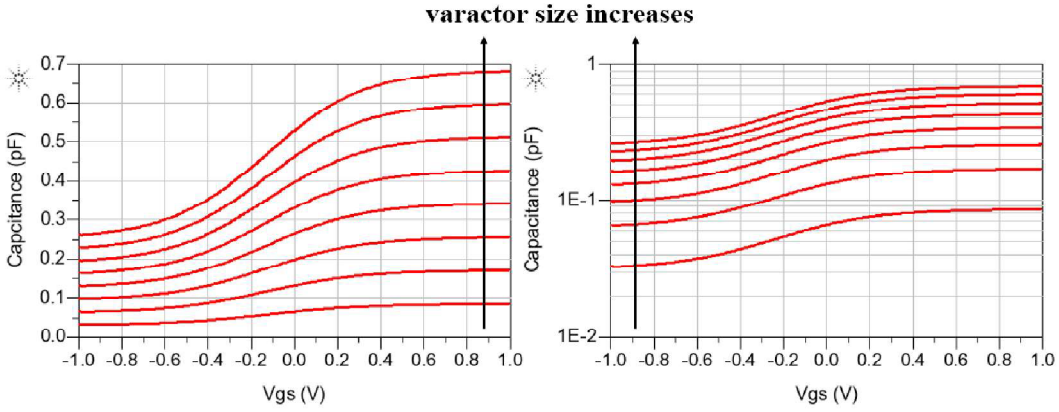
$$FTR = \frac{\omega_{o\_max} - \omega_{o\_min}}{V_{dd}} = \int_0^{V_{dd}} K_{VCO} \times \partial V_{ctrl} \tag{3-8}$$

where ω_{o_max} and ω_{o_min} are the maximum and minimum oscillation frequencies, respectively, when V_{ctrl} changes from 0 V to V_{dd}.

For simplicity, the parasitic capacitance of the transconductance stage is ignored and Kvcocan be calculated as:

$$K_{VCO} = \frac{\partial\left(\frac{1}{\sqrt{LC}}\right)}{\partial V_{ctrl}} = \frac{-1}{2C\sqrt{LC}} \times \frac{\partial C}{\partial V_{ctrl}} = -\frac{\omega_o}{2} \times \frac{\partial(\ln C)}{\partial V_{ctrl}} \tag{3-9}$$

When the oscillation frequencyis fixed, Kvco depends on the derivativeof lnC with respect to Vctrl. Figure 3-4shows a typical dependence of AMOS varactor capacitance in (a) linear scale and (b) log scale on the Vgs bias with different varactor size. The slope of capacitance in log scale at the same Vgs bias voltage is independent to the varactor size, as shown in Figure 3-4(b). Hence, when the oscillation frequency is determined, simply changing varactor size does not influence the Kvco and FTR.



(a) (b)

Figure 3-4. The AMOS varactor capacitance in (a) linear scale and (b) log scale vs. Vgs bias with different varactor size.

In this work, a 2.4-GHz band VCO IC is designed. Generally speaking, the Q-factor of the varactor is much higher than the inductor at this frequency band. When designing the LC resonant circuit, the size of inductor should be firstly optimized for the highest Q-factor, and then chose the appropriate varactor size for the specific oscillation frequency. According to Leeson's equation, optimizing the Q-factor of the LC resonant circuit improves the phase noise without influencing the Kvco and FRT of the VCO.

3.1.2 Review of reported VCO ICs

Several topologies were reported to decreasethe power consumption of VCOs such as Class-C VCOs [6]-[8]and low voltage VCOs [9]-[11].

3.1.2-a) thefirstly reported Class-C VCO IC

Class-C VCO ICswere introduced, theoretical analyzed and verified to have a phase noise than the conventional cross-coupled LC-VCO with the same power consumption in [6]. Figure 3-5shows the circuit schematic of the RC-biased Class-C VCO ICs reported in [6]. After oscillation, the phase noise of VCO could be improved by appropriately decreasing the bias voltage of cross-coupled transistors (Vbias). However, these reported VCO ICs have constant Vgbias and suffer from the problem of oscillation start-up .In the measurement, the circuits should be initially biased at Class-AB with high Vbias for oscillation start-up, and then Vbias was manually decreased for Class-C oscillation. Hence, automatic Vgbias control circuit is required for Class-C VCO IC implementation in the transceiver IC as a product.

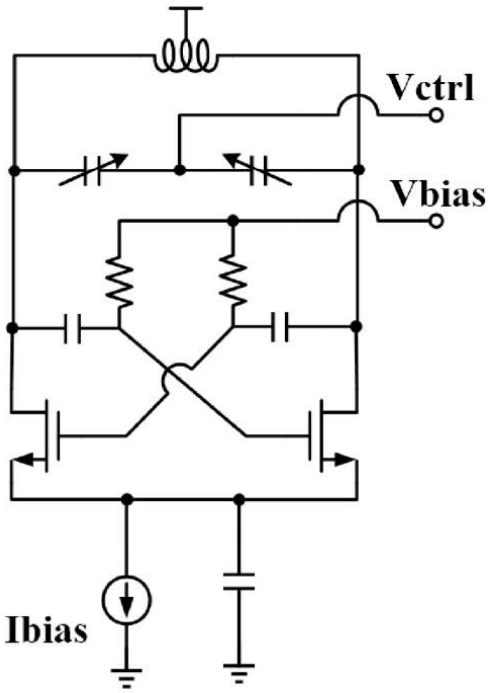


Figure 3-5. Schematic of theRC-biasedClass-C VCO IC reported in [6].

3.1.2-b) thereported Class-C VCO ICs with adaptive bias circuits

Hence, Class-C VCO ICs with adaptivebias circuits are reported in [7]-[8]. The paper [7]uses the feedback loop composed of an amplitude detector, a hysteresis comparator, a low pass filter and digital Finite State Machine (FSM) bias control circuit, which detects the output magnitude of the VCO and switches the bias voltage automatically from the voltage for star-up to the operating voltage for optimal performance, as shown in Figure 3-6. The advantages of digital control bias circuit are reconfigurationand a stable voltage control for all operation conditions. However, the digital control circuit has significant circuit complexity, which increases the designing time, chip size and power consumption of the VCO IC. The switching current bias (Ibias) serves as a Digital-to-Analog Convertor (DAC) and the Least Significant Bit (LSB) of Ibias should be high to ensure the tuning resolution, which furthermore increases the circuit complexity and power consumption. In addition, the digital control circuit has a long settling time from the initial oscillation start-up to the steady Class-C state and limits the application in the PLL or transceiver.

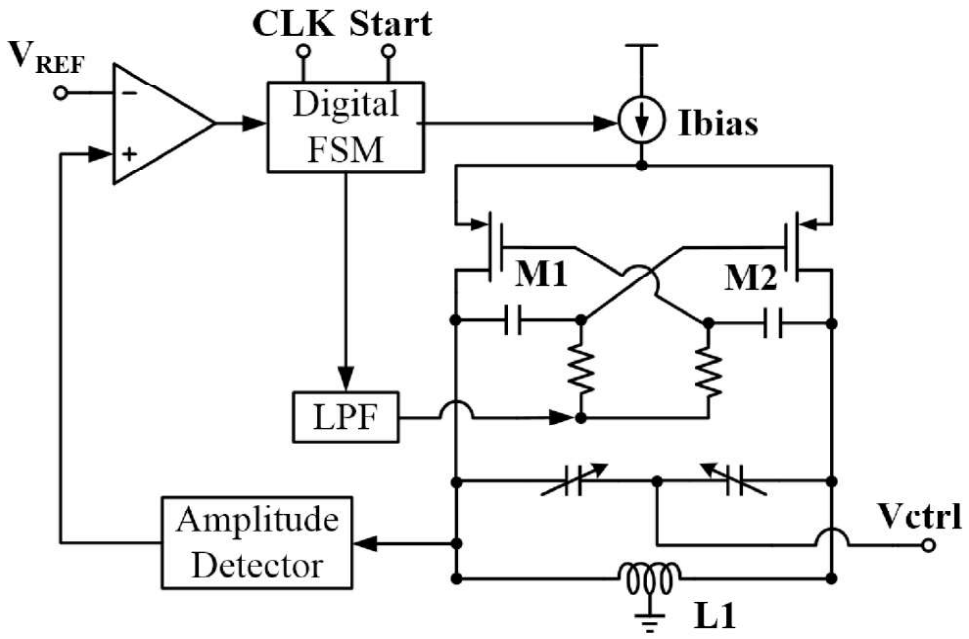


Figure 3-6. Schematic of the Class-C VCO IC applying digital dynamic bias circuit in [7].

The paper [8]uses an LC-VCO with a tail capacitorand with atail current source, as shown in Figure 3-7.The voltage at the common source of thecross-coupled transistors V_{CM} raisedas a result ofthe rectifying action of the tail capacitor.Thus, the

feedback loop in paper [8]sensedthe V_{CM} and decreases the gate to source bias of the cross-coupled transistors to realizeClass-C oscillation, whichpreventedthe amplitude detectorfromloading the LC resonant tank. Since the tail current source (or tail resistor) in the LC-VCO was required in the bias circuit, this reported VCO IC was not suitable for ultra-low voltage applications.

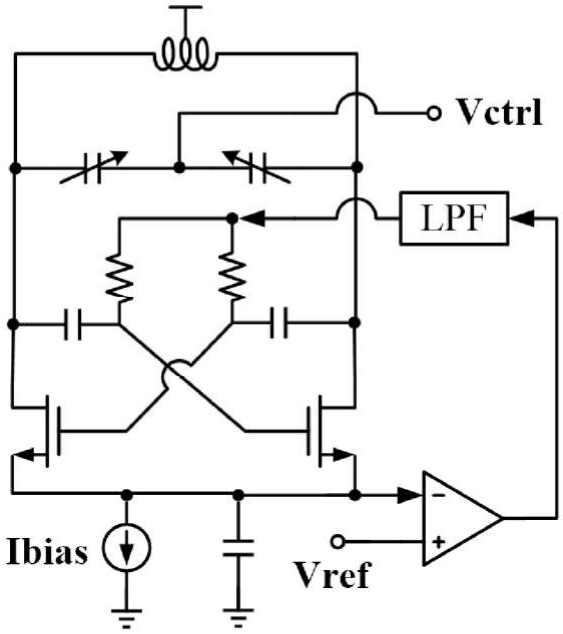


Figure 3-7. Schematic of the Class-C VCO IC applying analog amplitude feedback dynamic bias circuit in [8].

3.1.2-c) thereported low voltage VCO ICs

The papers[9]-[11]reported low voltage VCO ICs. However, these topologies are lack of bias voltage control circuits. In these topologies, is the supply voltage is near (or lower than) the V_{TH} of transistor, the VCO ICs may suffer from the critical issue of oscillation start-up. However, if the supply voltage is much higher than V_{TH} of transistor for robust oscillator start-up, the bias voltage is high for steady state and cause a high power consumption of VCO.

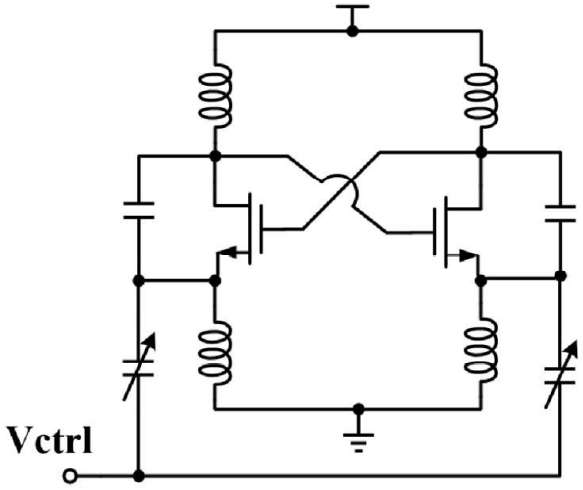


Figure 3-8. Schematic of the Class-C VCO IC applying analog amplitude feedback dynamic bias circuit in[9].

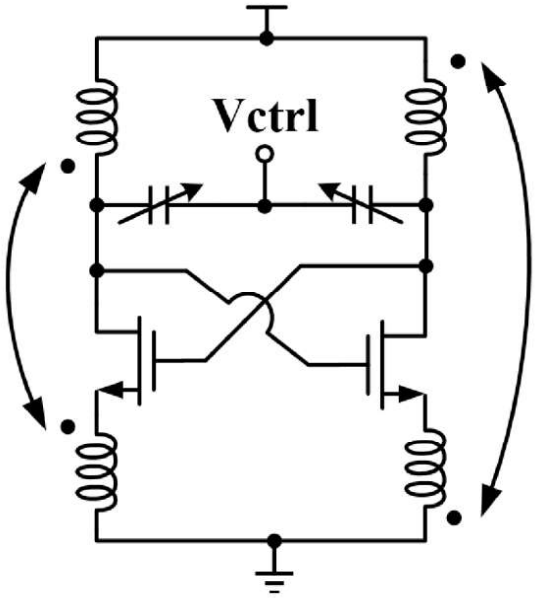


Figure 3-9. Schematic of the Class-C VCO IC applying analog amplitude feedback dynamic bias circuit in [10], [11].

3.1.3 65-nm CMOS process

In the modern RF IC design, the CMOS process is renowned for cost effectiveness in mass production and the capability of high System-On-Chip integration with digital parts.The 65nm CMOS processfor fabrication includes 12 metal layers, in which 1.2um thickaluminum is used as top layer for high Q-factor inductor design.

The cut-off frequency(f_T)and maximum oscillation frequency(f_{MAX}) of transistor are employed to evaluate the high frequency characteristic of transistor. f_T is defined as

the frequency when the current gain (H21) decreases to 0 dB. The maximum oscillation frequency (f_{MAX})is defined as the frequency when Mason's Unilateral Power Gain (Gmax) decreases to 0 dB. Gmaxrefers to the maximized power gain with respect to the reflection coefficients of source and load (Γ_S and Γ_L), after device has been unilateralized by lossless reciprocal embedding [12].

Figure 3-10shows the cross section of the Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs)in the 65-nm CMOS process. With a peak f_T and f_{MAX} over 200 GHz and a threshold voltage below 0.5 V, the nMOSFET is well qualified for 2-GHz-band VCO IC implementation.It is noted that triple-well process is available, in which the deep-n-well layer is inserted between p-well channel layer and p-substrate. Since this structure forms the p-n-p junction, the p-well channel layer is isolated to the p-substrate. Thus, according to the back-gate effect,the p-well channel layer (body) can be positively biased to decrease V_{TH} for the low voltage applications.

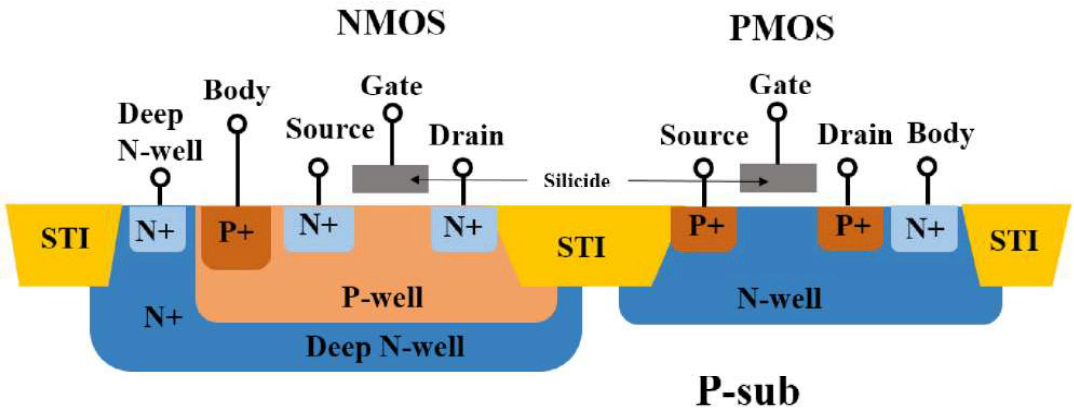


Figure 3-10. Cross section of the triple-well MOS transistors.

3.2 Operation principle

3.2.1 Block diagram ofVCO IC

Figure 3-11illustrates the simplified block diagram of proposedVCO IC, which consists of an LC-VCO, a power detector and a comparator. The detector and the comparator form an amplitude feedback loop circuit.

In the initial state, the LC-VCO starts to oscillate in class-AB operation. The DC output voltage of the detector increases as the amplitude of the LC-VCO output signal increases. The comparator compares the output voltage of the detector with the

reference voltage. The reference voltage V_{ref} of comparator is set to half of the maximum output voltage of the detector. When the detector output is larger than V_{ref}, the comparator feeds back a lower DC voltage to the LC-VCO to realize low power operation.

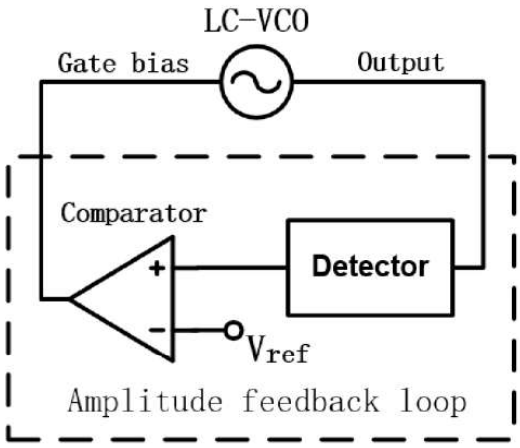


Figure 3-11. Block diagram of the VCO IC.

3.2.2 LC-VCO design

The cross-coupled LC-VCO topology is adapted due to its robust start-up and simple circuit implementation, as shown inFigure 3-12. Main interest in this paper is challenging to realize an ultra-low-voltage VCO IC. For oscillation to occur, the negative resistance generated by the cross-coupled transistors must cancel the loss of the LC resonant tank.

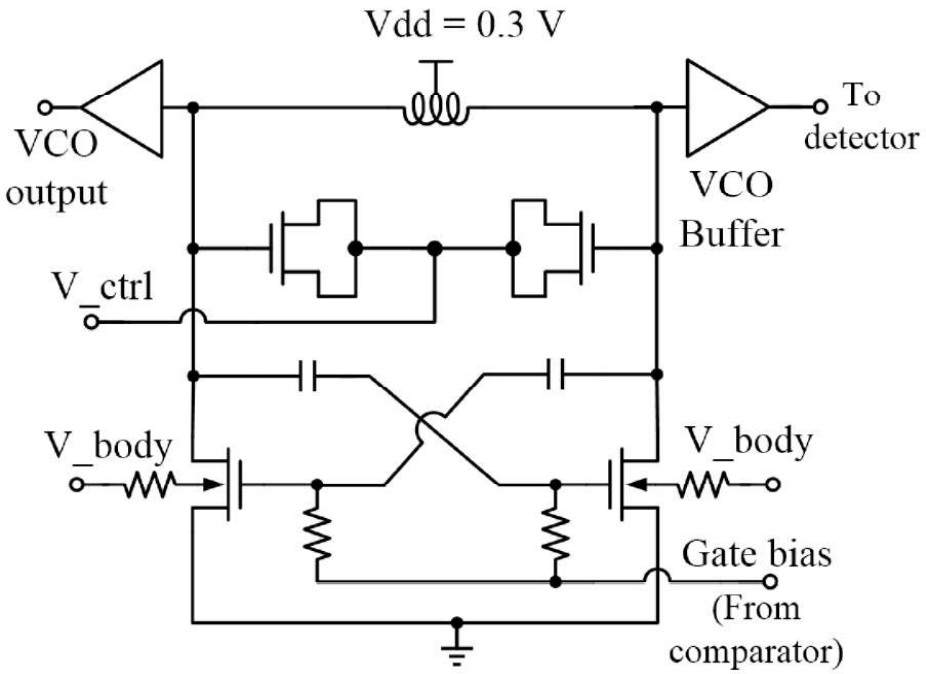


Figure 3-12. Circuit schematic of the LC-VCO core.

It is known that body-biasing technique can decrease the threshold voltage (V_{TH}) of a MOSFET and increase the small-signal transconductance (g_m),which helps the VCO to oscillate in low-voltage condition. Thus, triple-well process is applied for back-gate effect, in which the deep-n-well layer is inserted between p-well channel layer and p-substrate. Since this structure forms the p-n-p junction, the p-well channel layer is isolated to the p-substrate. Thus, the p-well channel layer (body) can be positively biased to decrease V_{TH}.

In the LC-VCO core circuit design, a gate bias circuit is inserted with resistors which are connected to the output of the comparator, as shown in Figure 3-12. Supply voltage (Vdd) of LC-VCO is from 0.3 V to 0.5 V, and comparator output voltage (V_bias) is 0.5 V in the initial state. Considering the low supply voltage, the conventional tail current source is eliminated to enlarge g_m and the voltage swing of the cross-coupled transistor pairs. To generate an appropriate DC bias current and g_m large enough with V_bias = 0.5 V, the total gate width of the cross-coupled transistor is chosen to 80 μm, and the gate length is 65 nm. After oscillation start-up, comparator output voltage decreases and the cross-coupled transistors bias is shifted fromhigh Vgs to low Vgswith lower DC bias current. Since the breakdown voltage of 65-nm CMOS process is 1.2 V, full voltage swing operation is affordable to long time reliability. In addition, decreasing the loss of the LC resonant circuit is very important to satisfy the

oscillation start-up condition in low voltage operation. For LC resonant circuit design, a single symmetric inductor is optimized to 4 nH with a Q-factor of 11.7 at 2.4 GHz.

Figure 3-13shows the simulated performance of oscillation frequencies under class-AB operation in steady state. It is expected that the LC-VCO starts to oscillate with an ultra-low supply voltage of only 0.3 V.Frequency tuning range is 9.8 % (from 2.23 to 2.46 GHz) with 0.5 V voltage supply and 8.7 % (from 2.3 to 2.51 GHz) with 0.3 V voltage supply.

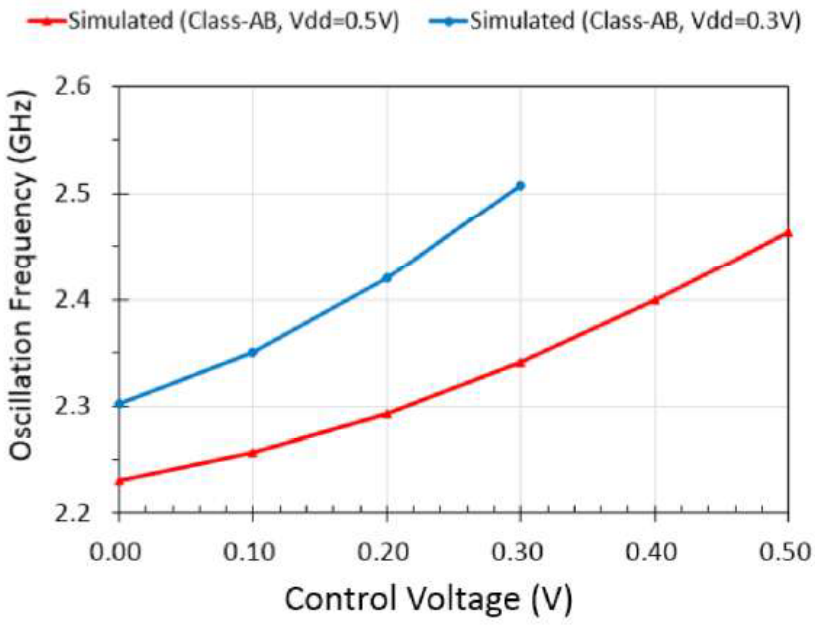


Figure 3-13. Simulated oscillation frequency vs. control voltage (V_ctrl).

Figure 3-14shows the load lines of the cross-coupled transistor at Vdd = 0.3 V, which confirms the operational region of the cross-coupled transistors. With $V_{TH} < Vgs \leq Vdd + V_{TH}$ bias, cross-coupled transistors work in saturation region and ensure an oscillation start-up.

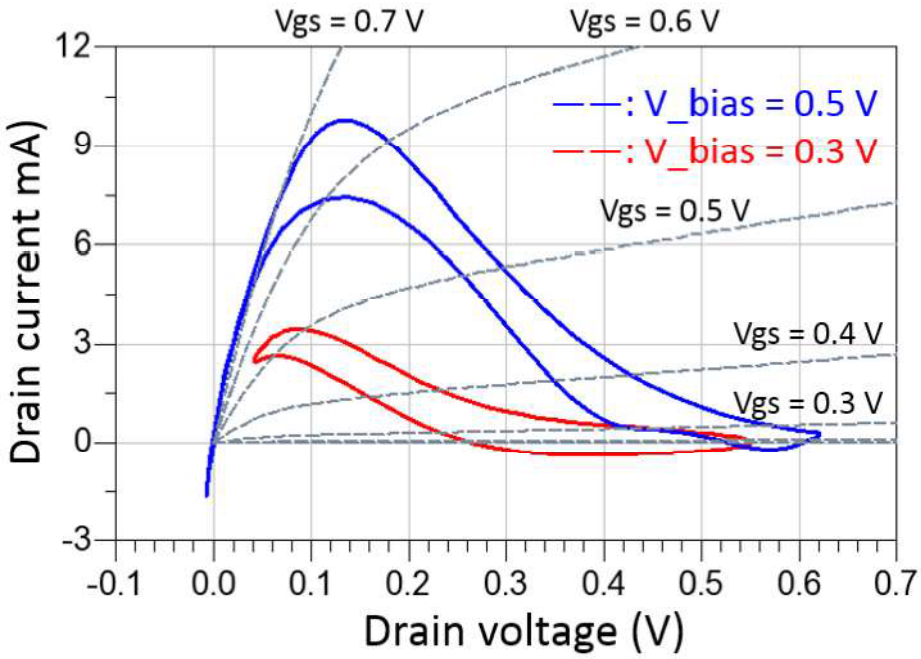


Figure 3-14. Simulated NMOS load lines at Vdd = 0.3 V with (V_{bias}) = 0.3 and 0.5 V.

3.2.3 Amplitude feedbackbiascircuit design

Figure 3-15 illustrates circuit schematic of the detector[13]. This topology employs the nonlinear behavior of both NMOSFET M1 and PMOSFET M2 to detect the input signal and transfer the ac input signal amplitude to DC output voltage. The core of the detector is formed by transistors M1 and M2, resistor R1, and MIM capacitors C1 and C2. Capacitor C1 serves as dcblock and is set to large value (5 pF) to decrease the power loss from the detector input to the gate of M1. Large resistor R1 (5 KΩ) supplies the dc component ofgate-to-source voltage (Vgs_dc)of M1 the same as dccomponent ofdrain-to-source voltage (Vds_dc) of M1. Capacitor C2 serves like a low-pass filter and keeps the M1 Vds_dcconstant. PMOSFET M2 serves as acurrent source and providesM1with small dcbias current (I_{bias}).

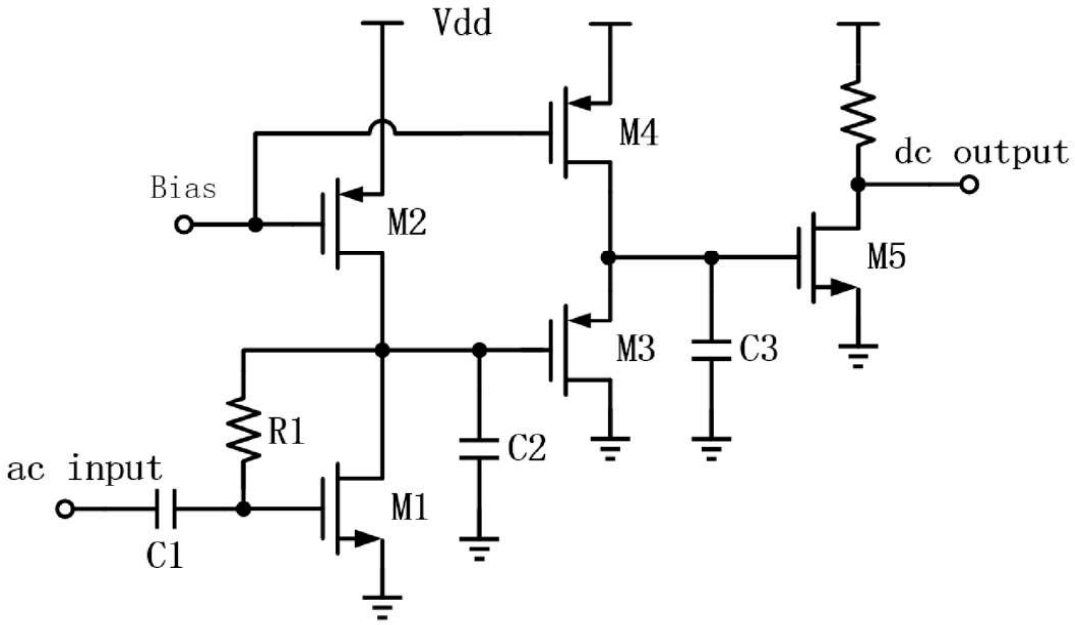


Figure 3-15. Circuit schematic of the power detector.

When the detector has no input signal, M1 Vgs_dcis near to V_{TH}. Since Vdd is 0.5 V, M2 Vds_dcis only about 0.1 V and M2 works in triode region. When the detector has a small ac input signal, the output voltage of M1 ($V_{M1.out}$) is:

$$V_{M1.out} = V_{TH} + \sqrt{\frac{2L_{M1}}{\mu_n C_{OX} W_{M1}} I_{bias} - \frac{A^2}{2}} \quad (3\text{-}10)$$

where A is the peak amplitude of the input signal assuming a sinusoidal waveform. W_{M1} and L_{M1} are the total gate width and gate length of M1. μ_n andC_{OX} are NMOS mobility and gate capacitance per unit area, respectively.

Whenthe detector input power slightly increases, dccomponent of drain current (Id_dc)of M1 and M2 increase as shown inFigure 3-16. Since M2 works in the triode region, M2 Vds_dcincreases for larger M2 Id_dc, which means that M1 Vds_dc and M1 Vgs_dcdecrease. Then M1 Vgs_dcis lower than V_{TH} and M1 enters the weak-inversion region. As M2 Vds_dccontinues to increase, M2 enters the saturation region and then M2 Id_dckeeps constant. As M1 Vgs_acincreases with input power increasing, M1 Vgs_dccontinues to decrease to keep the M1 Id_dcconstant.

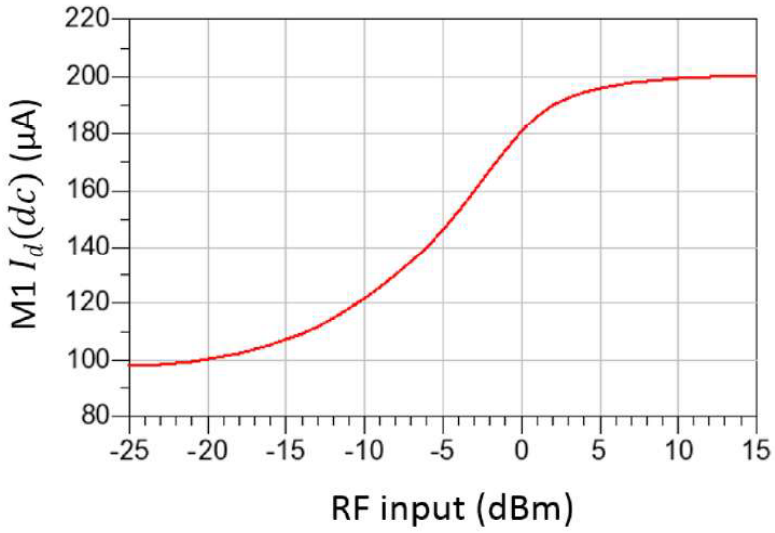


Figure 3-16. M1 Id_dcvs. input power.

Figure 3-17shows the time domain waveform of M1gate to source voltage (M1 Vgs_ac)and M1 drain current (M1 Id_ac) with increasing detector input signal power. As RF input power increases, dc bias of M1Vgs_dcdecreases and conduction angle of M1 Id_ac decreases.

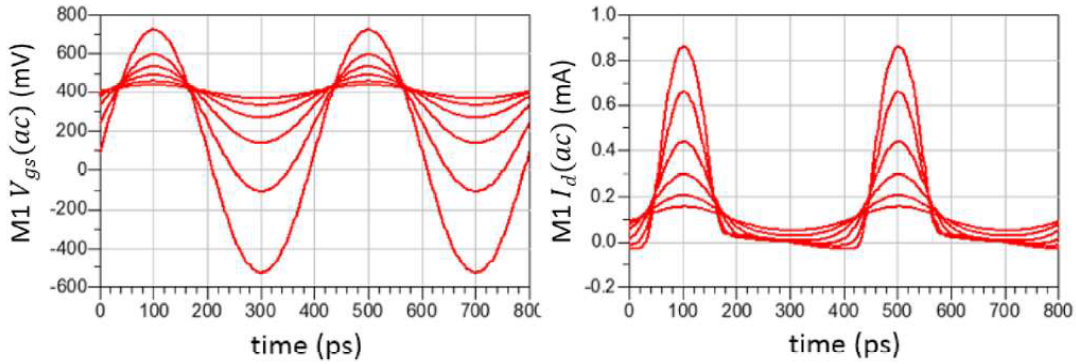


Figure 3-17. M1 Vgs_ac and M1 Id_acwaveform with different input power.

A two-stage amplifier is connected to the detector core circuit. The first stage is PMOS source follower for DC level conversion. A large capacitor (C3 = 5 pF) serves as a low pass filter. The second stage is the NMOS common source amplifier for DC voltage amplification.

Figure 3-18illustrates the simulated dependence of the DC output voltage on the input power. The frequency of the input signal is 2.4 GHz, and the operation voltage is 0.5 V. The output DC voltage gradually increases with increasing the input power, and the threshold power is around -10 dBm.

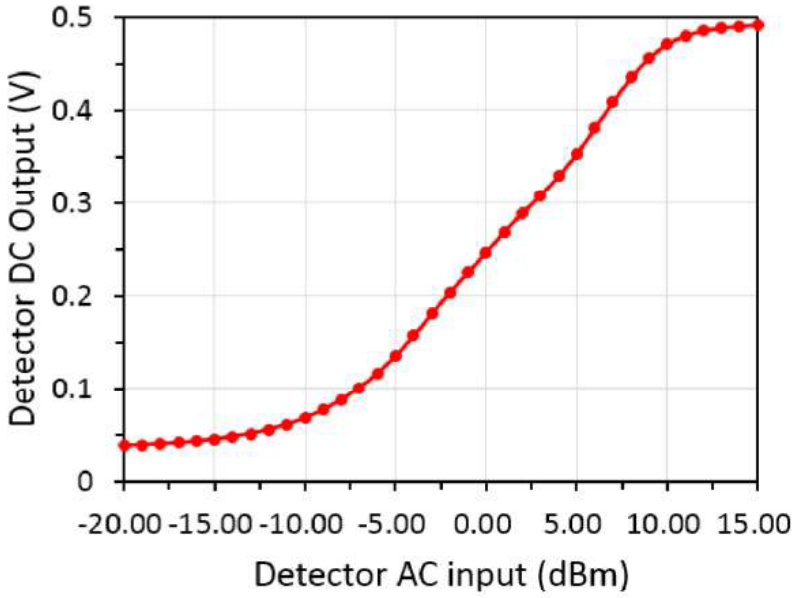


Figure 3-18. Simulated DC output voltage vs. ac input power of the power detector.

Figure 3-19illustrates circuit schematic of the comparator. Transistors M6, M7, M8, M9 and M10 form an open-loop operational amplifier. In the initial state, the detector output is close to 0 V,and the comparator output is close to Vdd of the feedback loop (0.5 V). After oscillation starts up, the DC output voltage of the detector increases. The reference voltage V_{REF} is set to one-half of the maximum output voltage of the detector. When the comparator input voltage is larger than V_{REF}, the gate to source voltage of M11 increases. Transistor M11 forms a buffer amplifier with a source degeneration resistor(R_S), which limits the minimum output voltage of the comparator to provide an optimal bias voltage for low poweroscillation.

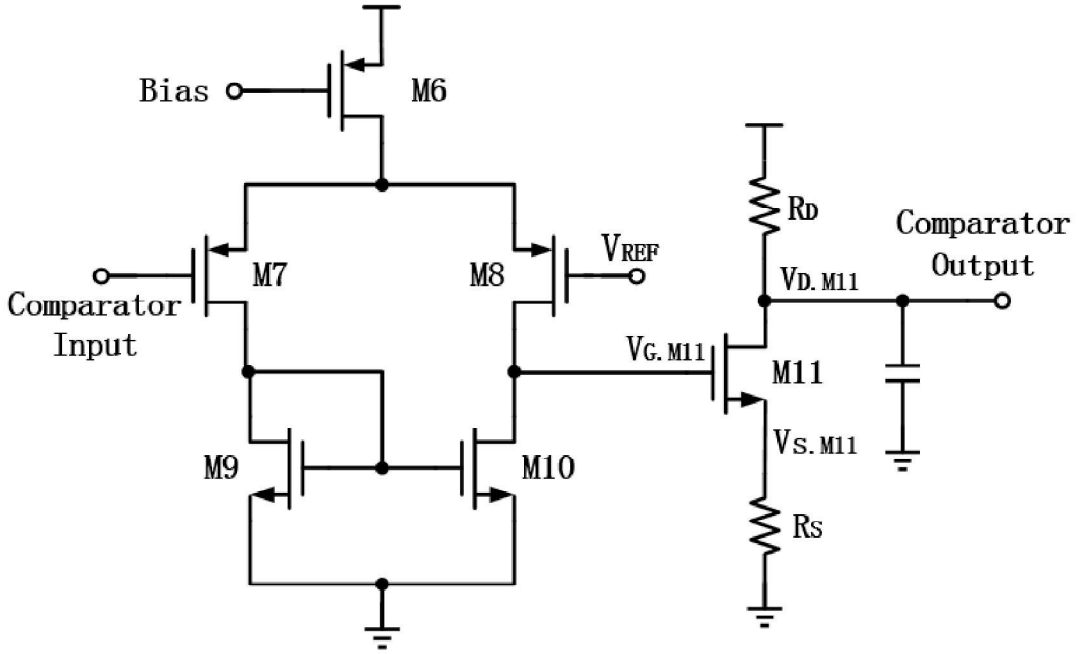


Figure 3-19. Circuit schematic of the comparator.

For transistor M11, drain current:

$$I_{M11.D} = \frac{1}{2}\mu_n C_{OX}\frac{W_{M11}}{L_{M11}}(V_{M11.G} - I_{M11.D}R_S - V_{TH})^2 \quad (3\text{-}11)$$

where W_{M11} and L_{M11} are the total gate width and gate length of M11, μ_n and C_{OX} are NMOS mobility and gate capacitance per unit area, respectively.

And the output voltage of comparator:

$$V_{COMP.out} = V_{M11.D} = V_{dd} - I_{M11.D}R_D \quad (3\text{-}12)$$

For low poweroscillation, the target of comparator output voltage is around V_{TH}, Thus, Rs can be calculated:

$$R_S = \left(\frac{V_{M11.G}-V_{TH}}{V_{dd}-V_{TH}} - \sqrt{\frac{2L_{M11}}{\mu_n C_{OX} W_{M11}(V_{dd}-V_{TH})}}\right) \times R_D \quad (3\text{-}13)$$

The comparator is designed to enhance the stability of the feedback loop. Since a fast transient of the LC-VCO gate to source bias potentially causes the oscillationto stop, a large capacitor (5 pF) is employed at the load of comparator as a low pass filter to make the bias voltage gradually decrease. In addition, to ensure the LC-VCO gate to source bias voltage high enough for continuous oscillation, the minimum output voltage of the comparator is controlled by a buffer amplifier with source degeneration.

3.3 Circuitdesign

3.3.1 Schematicof VCO IC

Figure 3-20showsthe detailedschematic of low powerVCO ICwith the proposed amplitude feedback bias circuit. Initially, the LC-VCO does not start oscillation and the detector dc output voltage is low.Thus, the comparator dc input voltage is lower than V_{REF} and the dc output voltage of comparator is high, which provides a high Vgs bias voltage for the LC-VCO. With a high Vgs and a high Id bias, the LC-VCO starts oscillation. After oscillation, the detector detects the oscillation and the dc output voltage of detector increases. When the dc input voltage of the comparator increases and is higher than V_{REF}, the dc output voltage of comparator decreases. Hence, the Vgs bias and current consumption of the LC-VCO decreases.TheLC-VCO is shifted from the initial robust oscillation start-up to the low power steadyoscillation state.

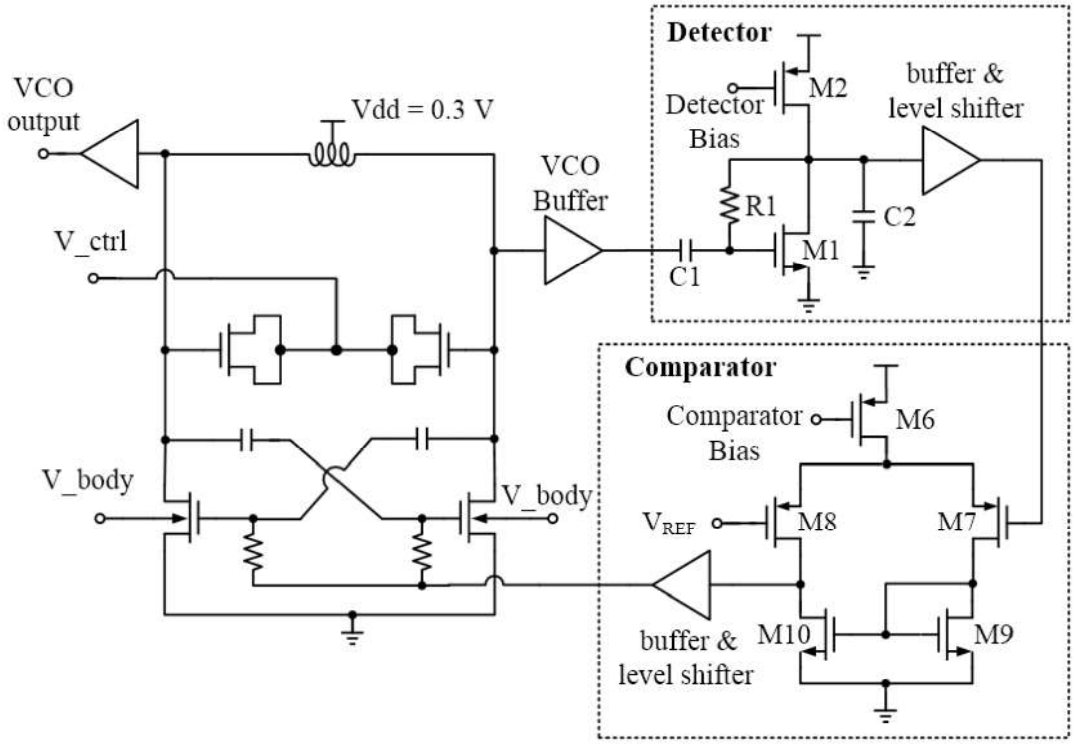


Figure 3-20. Detailed schematic of VCO IC with the proposed bias circuit.

3.3.2 Simulated performance

A transient simulation is performed to confirm the oscillation start-up and amplitude feedback performance of theVCO IC. Figure 3-21illustratesthe output waveform of the detector and comparator to confirm the feedback loop operation.

Initially, output voltage of the detector is close to 0 V, and output voltage of the comparator is about 0.5 V. The cross-coupled transistors are biased at Class-AB operation to ensure the oscillation start-up. When the oscillation starts, the detector output voltage increases and the comparator output decreases to about 0.3 V. Consequently, the operation of the LC-VCO changes from high powerto low power.

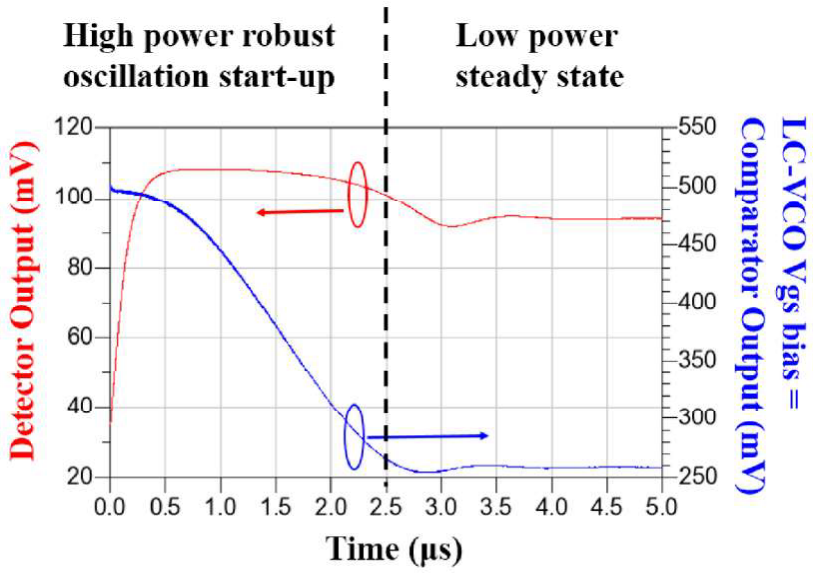


Figure 3-21. Simulated transient detector and comparator output voltage.

Figure 3-22shows the simulated waveform of the drain voltage of the LC-VCO cross-coupled transistors. From high powertolow poweroscillation, the voltage swing of the VCO slightly decreases. Figure 3-23shows the simulated waveform of the drain current of the LC-VCO cross-coupled transistors. From high powerto low power oscillation, the current swing significantly decreases from 10 mA to 4 mA. Therefore, it is expected that this amplitude feedback loop stably operates and effectively decreases the current consumption of the LC-VCO.

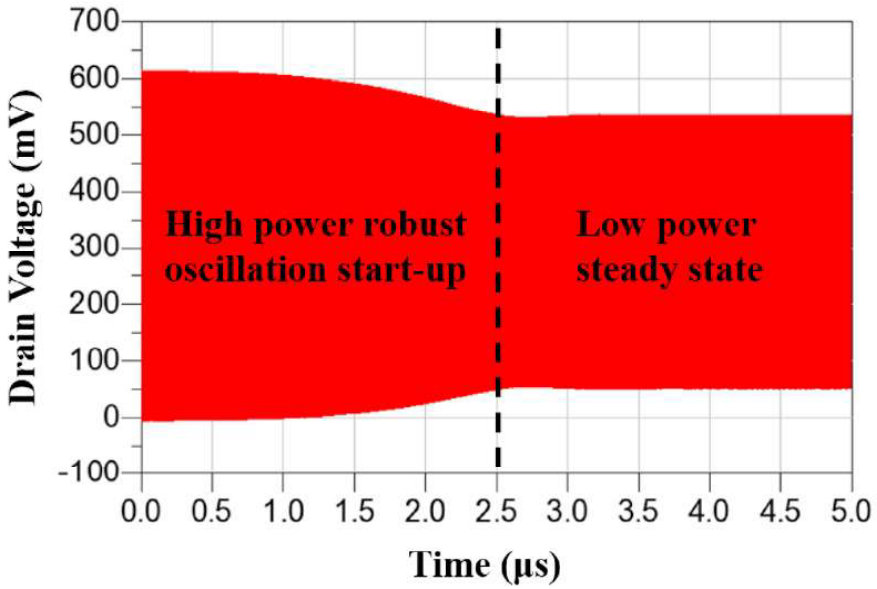


Figure 3-22. Simulated transient drain voltage of the LC-VCO cross-coupled transistors.

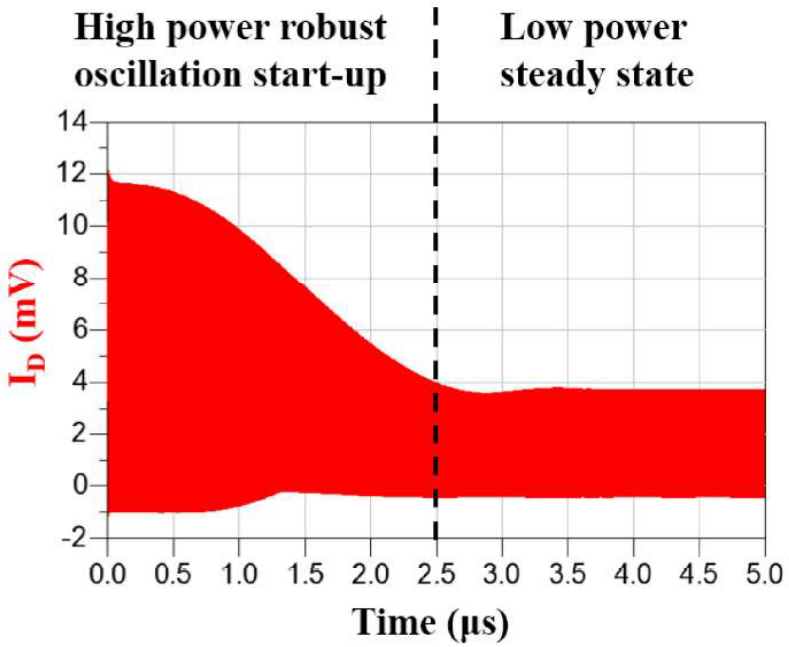


Figure 3-23. Simulated transient drain current of the LC-VCO cross-coupled transistors.

3.4 Measured performance

Figure 3-24illustrates the microphotograph of the VCO IC fabricated in 65-nm CMOS process. The core size of the VCO IC is 710 μm by 390 μm excluding pads.

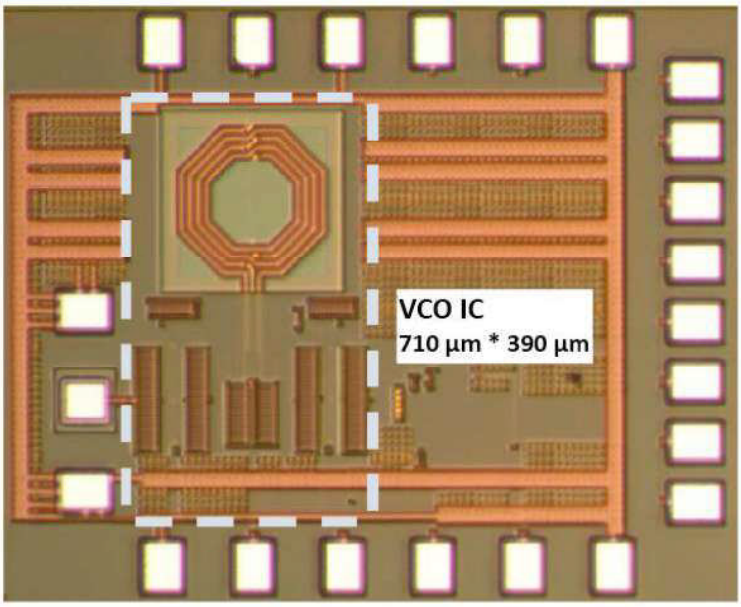


Figure 3-24. Die photograph of the VCOIC.

The measurements of the VCO IC was carried out using on-wafer probes. The DC current consumption of the LC-VCO core are 5.2 mA at a supply voltage of 0.5 V and 1.92 mA at 0.3 V, respectively. Power consumption of the proposed VCO is only 0.58 mW with a 0.3 V supply voltage.

Figure 3-25depicts measured dependence of oscillation frequencies in steady-state on the control voltage. The measured oscillation frequency bands are from 2.09 to 2.29 GHz (9.1 %) at a supply voltage of 0.5V, from 2.16 to 2.36 GHz (8.8 %) at a supply voltage of 0.4V, from 2.25 to 2.48 GHz (9.7 %) at a supply voltage of 0.3 V, respectively. Compared to the simulation results, measured oscillation frequency band at low power state changes only around 5 %, which shows a good agreement. This tiny change is probably caused by the parasitic effects of the layout,and the changeof junction capacitance of nMOSFETfrom initial high powerstart-up to low powersteady-state oscillation.

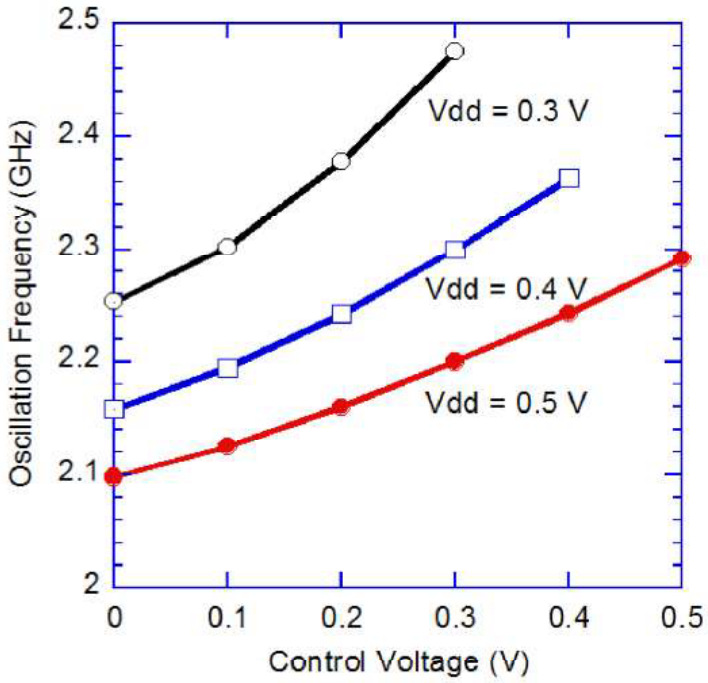


Figure 3-25. Measured oscillation frequency.

Figure 3-26 shows the measured oscillation frequency of the VCO IC with sweeping the supply voltage. When supply voltage decreases from 0.6 to 0.28 V, oscillation frequency increases from 2.10 to 2.27 GHz with control voltage fixed to 0 V. It is confirmed that the VCO IC can oscillate at a supply voltage over 0.28 V.

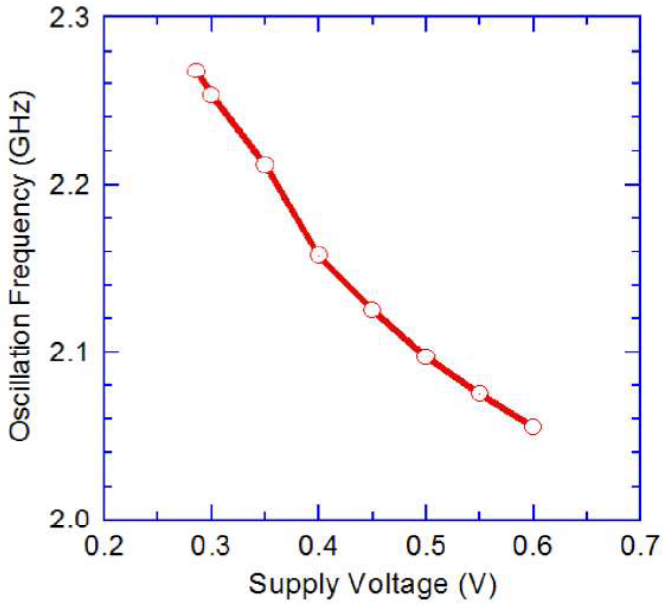


Figure 3-26. Measured oscillation frequency vs. supply voltage.

Figure 3-27depicts measured phase noise at an operation voltage of 0.3 V. The LC-VCO IC exhibits a measured phase noise of -111 dBc/Hz at 1 MHz offset from the 2.43 GHz carrier frequency. There are somephase noise spurs around 1 MHz offset frequency. Since the VCO IC chip is directly measured on wafer by probes, the phase noise measurement is sensitive to the noise of measurement environment.

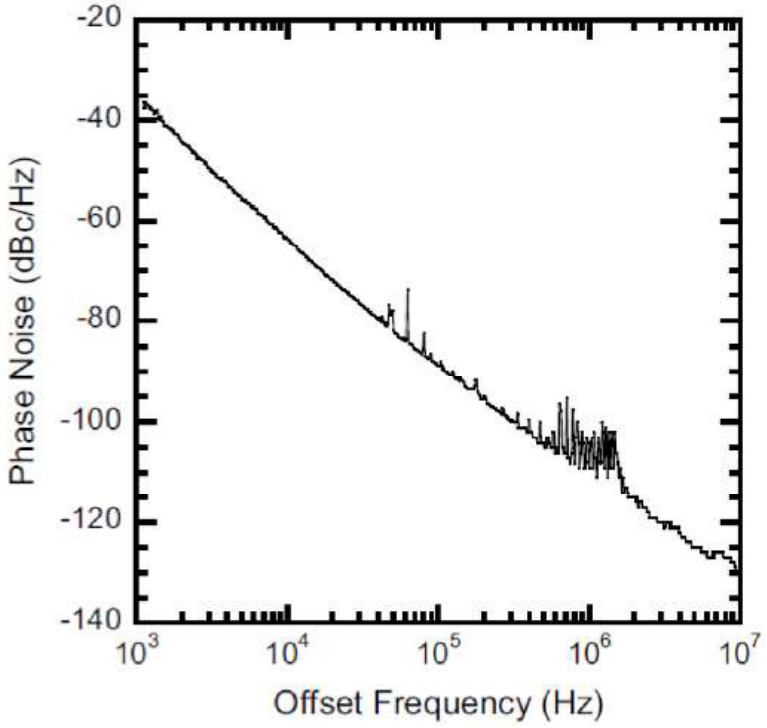


Figure 3-27. Measured phase noise at a power supplyof 0.3V.

At an operation voltage of only 0.3 V, Figure-Of-Merit (FOM), which is widely used for performance comparison of VCOs, is:

$$\text{FOM} = L(\Delta f_m) - 20\log\left(\frac{f_o}{f_m}\right) + 10\log\left(\frac{P_{diss}}{1\,mW}\right) \approx -181.1\ \text{dBc/Hz} \quad (3\text{-}14)$$

where $L(\Delta fm)$is the phase noise at the offset frequency (f_m), f_o is the oscillation frequency, and Pdiss is the dissipation power of the VCO.

Table 3-1summarizes the performance of the proposed VCO IC with other reported low-voltage VCOs. This work shows a competitivephase noise and FOM T with ultra-low-voltage operation and low power consumption.

Table 3-1. Comparisonwith previous VCO ICs

Ref.	Process	Freq. (GHz)	Vdd (V)	DC power (mW)	Phase Noise @ 1MHz (dBc/Hz)	FOM (dBc/Hz)
[8]	90-nm CMOS	3.97	1.2	6.6	-127	-190.8
[10]	65-nm CMOS	2.04	0.3	0.78	-102	-169.3
[14]	65-nm CMOS	5.54	0.5	0.92	-105	-180.2
This work	65-nm CMOS	2.43	0.3	0.57	-111.0	-181.1

3.5 Conclusion

A novel 2.4-GHz band ultra-low-voltage and low power VCO IC with an amplitude feedback bias circuithas been demonstrated in 65-nm CMOS process. The VCO IC consists of an LC-VCO circuit and an amplitude feedback biascircuit.

Forthe ultra-low-voltage operation, the tail current bias circuit of the LC-VCO is removed and black-gate effect is adopted to decrease the V_{TH} of transistor. For the low power oscillation without the oscillation start-upproblem, an amplitude feedback bias is proposed including the power detector, voltage comparator, dc level shifter and buffer amplifier. The proposed bias circuit adaptively changes the bias voltage of LC-VCO according the output power of VCO, and shiftsthe oscillation state of LC-VCO from initial high power oscillation start-upstate to steady low power state.

The VCO-IC has achieved alow power consumption of 0.58 mW, a phase noise of -111 dBc/Hz and an FOM of 181 dBc/Hz are at a power supplyof only 0.3 V.The measured performance confirms the effectiveness of the proposed amplitude feedback bias circuit of decreasing the power consumption of VCO without influencing the oscillation start-up. Since the VCO significantly influences the power consumption of transceiver, it is expected that the proposed topology could decrease the power consumption of transceiver IC.

References of Chapter 3

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Chapter 4Low Power SiGe HBT Down-conversion SHM IC with a Tail Current Bias Circuit

4.1 Introduction

In Chapter 3, a low voltageand low powerVCO IC withan amplitude feedback bias circuit for 2-GHz bandapplications has been demonstrated in 65-nm CMOS process.

In this chapter, a low power Sub-harmonic Mixer (SHM) IC is designed for 80-GHz applications[1]-[2]. Down-conversion mixer is a key component of the RF receivers. As introduced in Chapter 1, sub-harmonic mixer (SHM) can mix the RF signal with the second harmonic of the LO ($2f_{LO}$) signal.With relatively low oscillation frequency, the oscillator has better phase noise performance, and the buffer of the oscillator can provide higher LO power with lower power consumption. Hence, SHM is an attractive solution in the W-band receivers.

For SHM IC design, decreasing the LO power requirement is effective to decrease the output power and power consumption of LO buffer. In addition, making the conversion gain of SHM insensitive to LO power could remove the power control circuit of LO bufferand accordinglydecrease the power consumption of LO buffer. Thus,SHM should be designed with low LO power requirement and with conversion gain insensitive to LO power.In this work, a novel bottom-LO configuration is proposed to decrease the LO power requirement of SHM. A tail current bias circuit is proposed to make the conversion gain insensitive to LO power. The proposed bias circuit adaptively changes the bias voltage of LO stage to flattenthe 2* f_{LO} generation and to flatten the conversion gain with injected LO power changing.

A bottom-LO-configured SHM IC with the proposed bias circuitfor 80-GHz band applications is designed, fabricated and measured in 130-nm SiGe BiCMOS technology. From comparison, a conventional top-LO-configured SHM IC is also designed, fabricated and measured.

At the beginningof this chapter, introduction is givenin Section4.1, including the review of previously reported down-conversion SHMICs and brief descriptions of 130-nmSiGe BiCMOS for chip fabrication. Theworking principles of the proposed bottom-LO-configured SHM (with and without a tail current source) and the conventional top-

LO-configured one are described and comparedinSection4.2. Then in Section4.3, the circuit design including the schematic and simulated performance of both theproposed and conventional SHM ICs are presented.In Section 4.4, measured performanceof the SHM ICs isdemonstrated with the comparison of previous works. Finally, conclusions are given in Section4.5.

4.1.1 Review of reported down-conversion SHM ICs

Figure 4-1shows the schematic of aPassive Anti-Parallel Diode Pair (APDP) SHM ICreported in [3]. The diode passive mixer has the advantages of no dc power consumption, high operation frequency and high linearity. However, the passive mixer requires particularly high LO power (10 dBm)and significant conversion loss (-8 dB).

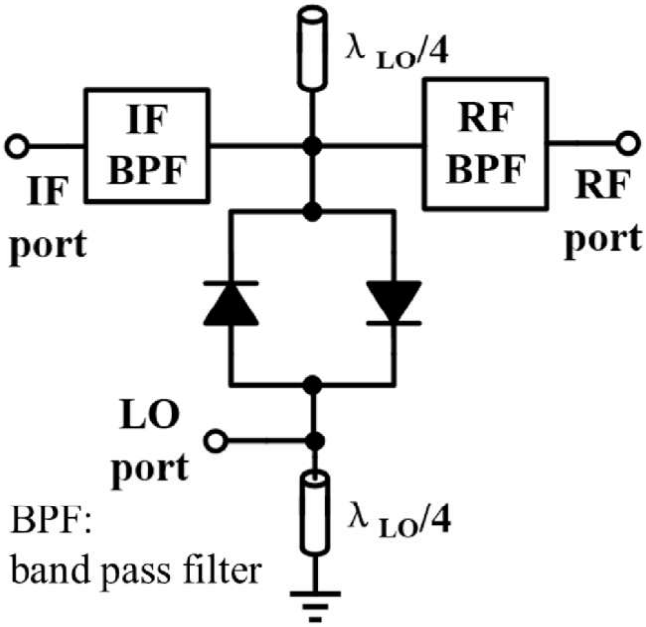


Figure 4-1. Passive Anti-Parallel Diode Pair (APDP) SHM ICreported in [3].

Figure 4-2shows the schematic of a Sub-harmonically pumped gate SHM IC reported in [4]. As an active mixer, the SHM could have conversion gain.This topology re-used the LO frequency doubling stage and RF amplifying stage, which decreased the supply voltage.However, the 90° phase shifter of LO signal for the LO isolation networkhad high lossand increased theLO power requirement (6 dBm).Another critical issue of this topology was the bias voltage.Class-C bias voltage is required for the 2* f_{LO} generation, while Class-AB biasregion is required for the RF signal amplification. Thus,conversion gain of the SHM IC was suppressed.

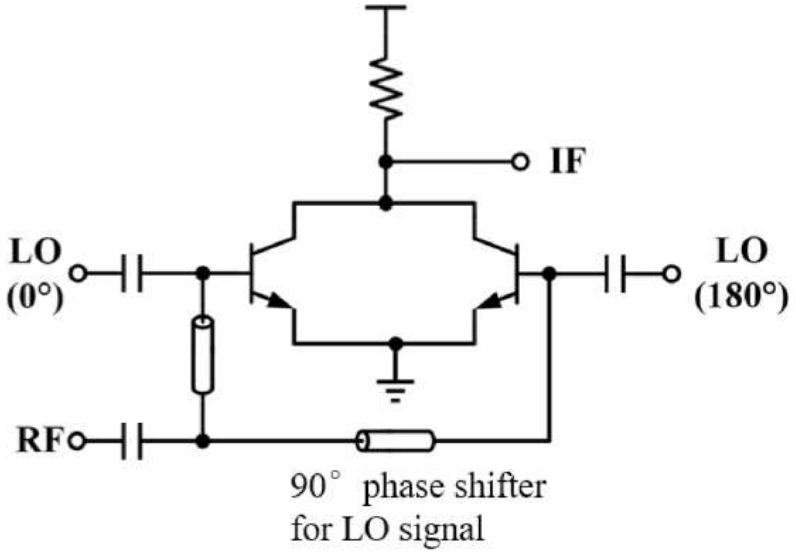


Figure 4-2.Sub-harmonically pumped gate SHM IC reported in [4].

Paper [5]reported an SHM topology with a compact input network, as shown in Figure 4-3. L1 and C1 resonant at f_{LO} to prevent LO-RF leakage, while L2 and C2 resonant at f_{RF} to preventRF-LO leakage. The LC πnetwork provides a 90 °phase shift at f_{RF} ($\approx 2f_{LO}$) and a corresponding 180 °phase shift at f_{LO}. From the base of HBT Q1 to the base of HBT Q2 with two LC -nπtworks,RF signalis transferred from single-ended to differential while LO signal is kept at the samephase. This topology has high LO-RF and 2LO-RF isolation between the LO and RF ports. However, it is challenging to realize the RF and LO input matching at the same time. Thus, this topology requires high LO pumping power.

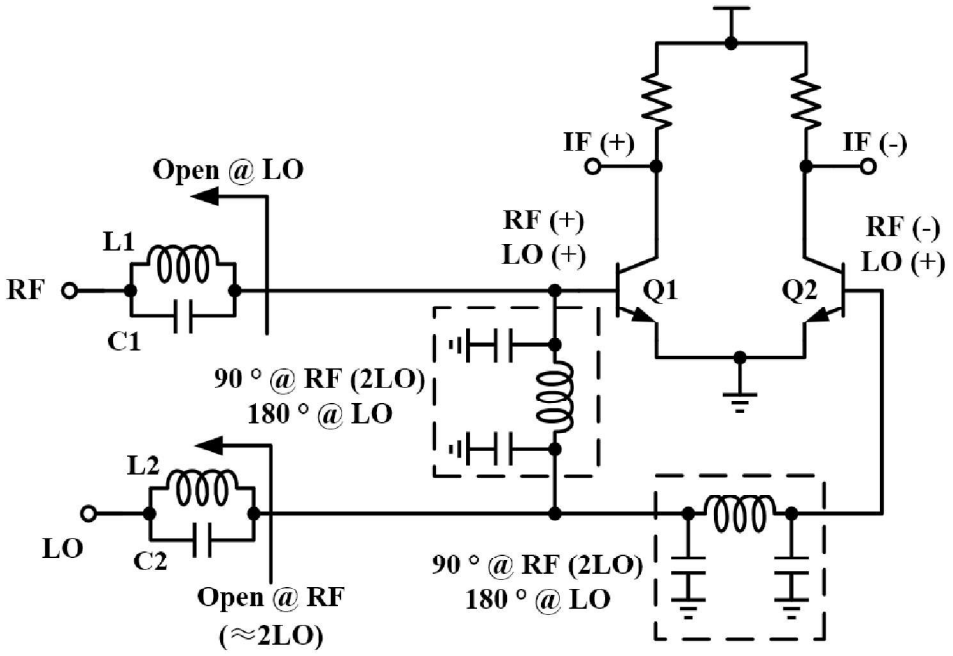


Figure 4-3. Reported balanced SHM with a compact networkin [5]

Gilbertcell topologiesare also widely used to implement SHMs.Threekinds of the Gilbert-cell based SHMs are reportedand extensivelyused: three-level stacked-LO SHMs [6]-[9], levelled-LO SHMs with bottom-LO configuration[10]-[12]and top-LO configuration [13]-[15].

Figure 4-4(a) shows the schematic of the three-level stacked-LO SHM, which use the current switching mechanism to mix the f_{RF} signal with the 2* f_{LO} harmonic to generate the f_{IF} signal.For simplification, the behaviors of LO stage HBTs are regarded as ideal switchesand the RF currents (I_{RFP} and I_{RFN}) are modulated by the LO stages. The switching functions of LO stages are square waveforms toggling between off (0) and on (1)and are expressed as S_1,S_2, S_3 and S_4, as shown in Figure 4-4(a). The phase differences of the switching functions are dependent on the phase differences of the LO signals injected at the base of HBTs. Thus, the time domain waveforms of S_1,S_2, S_3 and S_4 are drawn in Figure 4-4(b). The RF stage transfer the f_{RF} voltage input to f_{RF} current (I_{RFP} and I_{RFN}). The down LO stage switches the I_{RFP} and I_{RFN} and generatesthe current I_1 and I_2. The up LO stage switches the I_1 and I_2 and generates the IF output current I_{IFP} and I_{IFN}. Hence, I_{IFP} and I_{IFN} can be expressed as:

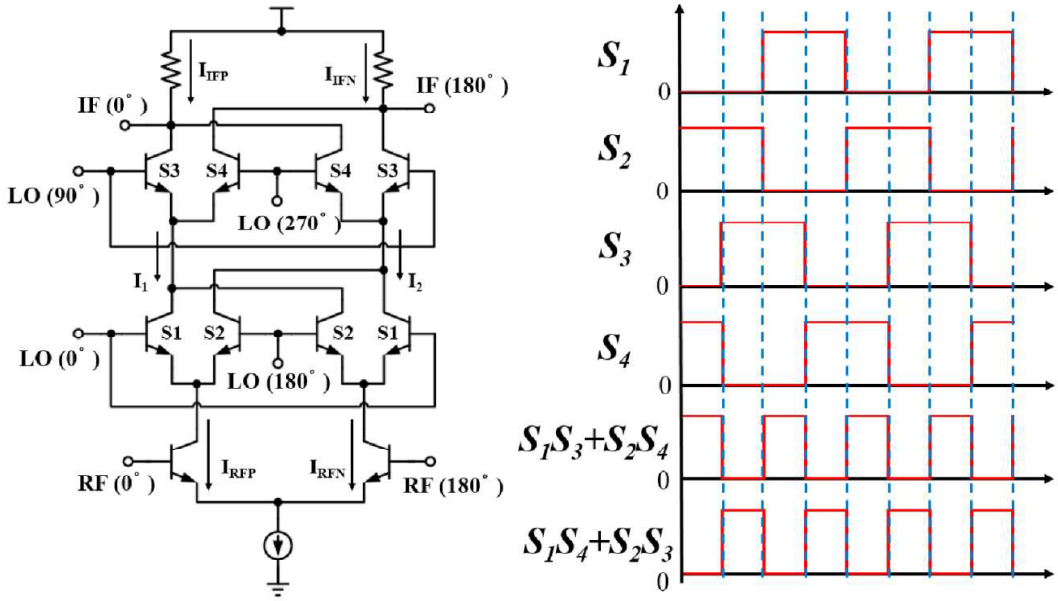
$$\begin{aligned} I_{IFP} &= S_3 I_1 + S_4 I_2 = S_3(S_1 I_{RFP} + S_2 I_{RFN}) + S_4(S_2 I_{RFP} + S_1 I_{RFN}) \\ &= (S_1 S_3 + S_2 S_4)\, I_{RFP} + (S_1 S_4 + S_2 S_3)\, I_{RFN} \qquad (4\text{-}1) \\ I_{IFN} &= S_4 I_1 + S_3 I_2 = S_4(S_1 I_{RFP} + S_2 I_{RFN}) + S_3(S_2 I_{RFP} + S_1 I_{RFN}) \end{aligned}$$

$$=(S_1S_3 + S_2S_4)\, I_{RFN} + (S_1S_4 + S_2S_3)\, I_{RFP} \quad (4\text{-}2)$$

Figure 4-4(b) illustrates the time domain waveforms of the switching functions $S_1S_3+S_2S_4$ and $S_1S_4+S_2S_3$. It is obvious that these two switching functions have a phase difference of 180°. Considering the phase difference between the I_{RFN} and I_{RFP} is also 180°, I_{IFP} and I_{IFN} can be calculated as:

$$I_{IFP} = 2(S_1S_3 + S_2S_4)\, I_{RFP} = -I_{IFN} \quad (4\text{-}3)$$

It is noted that the frequency of $S_1S_3+S_2S_4$ is twice of frequency of the S_1 (f_{LO}). Hence, I_{IFP} is modulated by the 2* f_{LO} and the IF frequency: $f_{IF} = f_{RF}$ -2* f_{LO}.



(a) (b)

Figure 4-4. (a) Reported Gilbert-cell three-level stacked-LO SHM in [6]-[9].(b) time domain waveform of the LO stage switching function.

Gilbert-cell levelled-LO SHM topologies were reported including both bottom-LO configuration [10]-[12]and top-LO configuration [13]-[15], which use the nonlinearities of transistors to generate 2* f_{LO} signal for mixing. Figure 4-5and Figure 4-6show the Gilbert-cell levelled-LO SHM with bottom-LOand top-LO configurations, respectively. The Gilbert-cell levelled-LO SHMs are essentiallyGilbert-cell mixers. The HBTs in LO stages are replaced by the Common Emitter Common Collector Transistor Pairs(CECCTP), which doublethe frequency of LO signal. Since the LO frequency is doubled, the phase difference of LO signal is doubled. In the bottom-LO-configured Gilbert-cell SHM as shown in Figure 4-5, the 2* f_{LO} output currents of

CECCTPs at the bottom are differential and are modulated by RF stages to generated the IF signal. However, the RF signals are small signals and the switching behaviors of RF HBTs are particularly weak, which significantly limits the conversion gain. Thus, top-LO-configured Gilbert-cell SHM withhigher conversion are reported as shown in Figure 4-6. Four top CECCTP stages are applied to generated the double-balanced differential 2*f_{LO} signals. Hence, the differential RF current at the bottom are modulated by the 2*f_{LO} switching stages to generate the IF signal. The SHM in Figure 4-6works like a traditional Gilbert-mixer with 2*f_{LO} injected at the top LO switching stages.

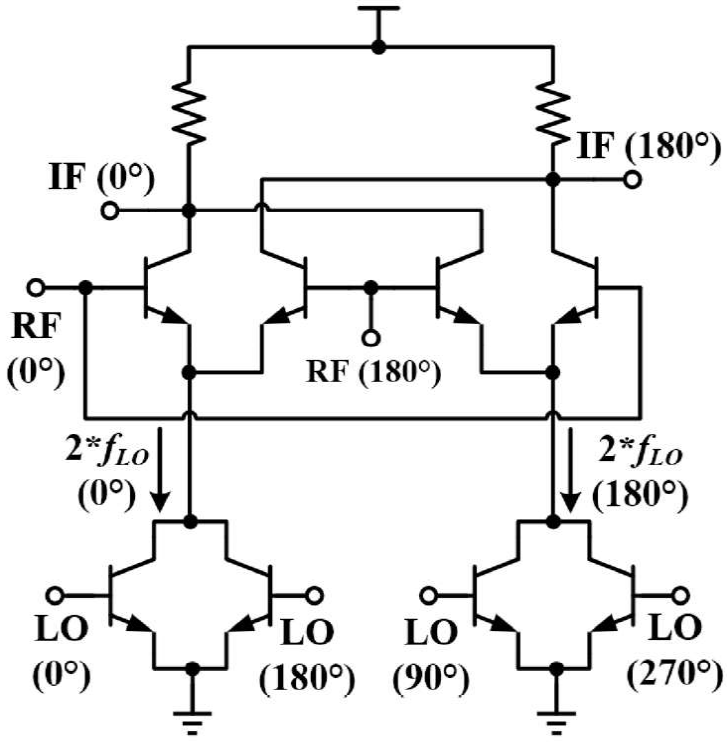


Figure 4-5. Reported Gilbert-cell levelled-LOSHM with bottom-LO configurationin [10]-[12].

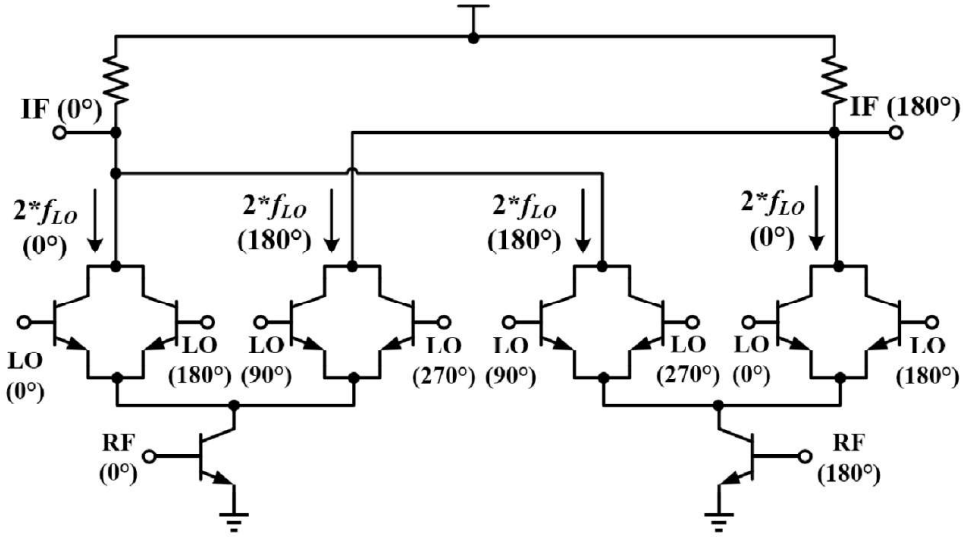
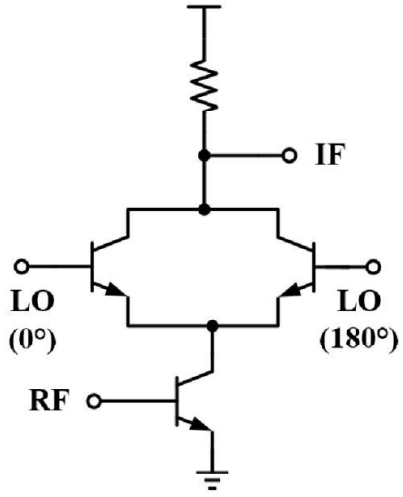


Figure 4-6. Reported Gilbert-cell levelled-LOSHM with top-LO configurationin [13]-[15].

The design trade-offs of the Gilbert-cell SHMs between stacked-LO and levelled-LO configurations were reported in [16]. It is reported that Gilbert-cell stacked-LO SHM has lower LO power requirement but lower operational frequency than the Gilbert-cell levelled-LO SHMs. This trade-off is mainly caused by the different operational principles. The transistor switching characteristic used by stacked-LO SHM is sensitive to signal frequency. The transistor nonlinearities used by levelled-LO SHMs is sensitive to signal power.In addition, paper [16]also reported trade-offs of the levelled-LO Gilbert-cell SHMsbetween the bottom-LO and top-LO configuration. Compared to the bottom-LO Gilbert-cell SHM, top-LO one has higher conversion gain and 2LO-to-RF isolation, but also has power consumption, lower linearity, and lower RF-to-IF isolation.

All these Gilbert-cell SHM topologies require a precise quadrature LO signal and have complicated circuit layouts, which makesthe implementation of Gilbert-cell SHMs for millimeter wave applications quite challenging.The CECCTPSHMs with top-LO-configuration were also reported in[17]-[19], as shown inFigure 4-7.Owing to differential LO signal input and simple circuit layout, CECCTP structure is considerable for millimetre-wave SHM IC.In the conventional top-LO-configured CECCTP SHM, however, the bottom RF stage suppresses the generation of $2f_{LO}$ signal and results in a high requirement of LO power.Hence, in this work, an improved bottom-LO-configured CECCTP SHM IC with a tail current source is proposed for W-band applications [1].The bottom-LO-configuration decreases the LO power

requirement and the tail current sourceflattensthe conversion gain.



(a) (b)

Figure 4-7. Conventional CCEETP mixer employing top-LO configurationreported in [17]-[19].

4.1.2 130-nm SiGe BiCMOS technology

130-nmSiGe BiCMOS processis applied to design and fabricate theSHM IC. The process has six layers of aluminum metal.The top metal (M6) has a thickness of 2.8 m, μ which has low resistivity and is suitable to design the implement the low loss passive devices, such as inductor, microstrip line and Marchand balun. TheMIM (Metal-Insulator-Metal) capacitor with low capacitance density on Metal 4andstacked MIM capacitor with high capacitance density on Metal 3 and Metal 4are availablein this process.

It is noted that the high-speed NPN HBT has a collector implant layer, which increases the cut-off frequency but decreases the breakdown voltage. Deep Trenches (orange region) form the sidewall isolation from the n-typecollector to the P-substrate. The deeptrenches minimizethe perimeter capacitance from collector to substrate.The details of this130-nm BiCMOSprocess are described in [20].

Table 4-1shows the typical measured specifications of the high-speedHBT with collector implant and the high-voltage HBT without collector implant. Since the high-speed HBT has a cut-off frequency (f_T) of 240 GHz and maximum oscillation frequency (f_{MAX}) of 260 GHz, high-speed HBT is utilized to implement the W-band SHM IC design.

Table 4-1 Typical specifications of the SiGe NPN HBT (25 °C)

NPN type	BV_{CEO} (V)	*ft* (GHz)	*fmax* (GHz)	Emitter size (μm^2)
Low voltage (with collector implant)	1.6	240	260	0.13×1

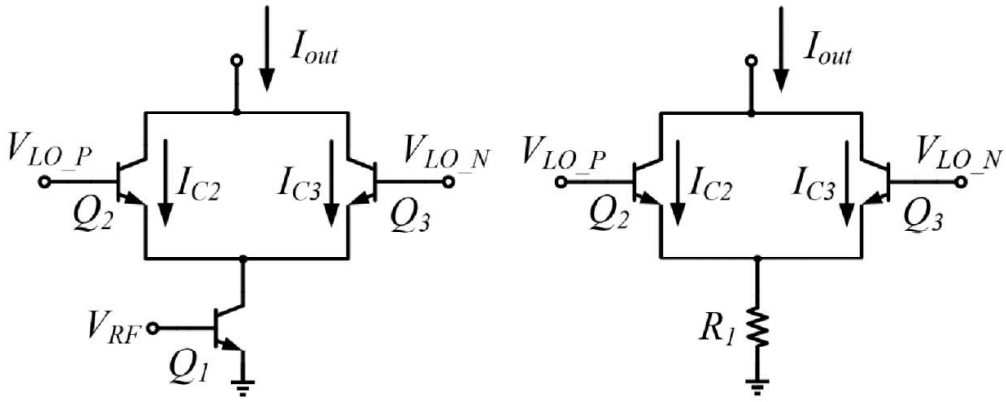
4.2 Operation principle

4.2.1 CECCTP SHMs with top-LO and bottom-LO configurations

3.3.1-a) Conventional top-LO-configured CECCTP SHM

Figure 4-8(a) illustrates thecore circuit of the conventional top-LO-configured CECCTP SHM. Load and bias circuits are not drawn for simplicity. HBT Q1 serves as a transconductance amplifier for RF input stage. HBTs Q2 and Q3 form a CECCTP stage to generate the second harmonic of the LO signal (2*f_{LO}). The frequency mixing principle of this SHM is very similar to the dual-gate mixer analyzed in paper [21]. The generated 2*f_{LO} signal modulates the collector voltage of Q1 and switches Q1 between the saturation and forward active region over 2* f_{LO} cycle. Since the bias current and transconductance of Q1 are modulated by 2*f_{LO} signal, the RF signal is mixed with the 2*f_{LO} signal and the IF signal ($f_{IF} = f_{RF}$ -2* f_{LO}) is generated. It is noted that the 2* f_{LO} power significantly influences the Q1 modulation and the conversion gain of SHM.

In order to maximize the generation of 2*f_{LO} signal, Q2 and Q3 are biased to work in switching mode [22], which means that when one transistor is turned on, theother one is turned off.Figure 4-8(b) shows the simplified model of the LO frequency doubling stage. For each half cycle, Q2 orQ3 works like a common emitter amplifier with a degeneration resistor R_1. Hence, the magnitude ofthe collector current is decreased and the generation of 2*f_{LO} in the output current (I_{out}) is suppressed.

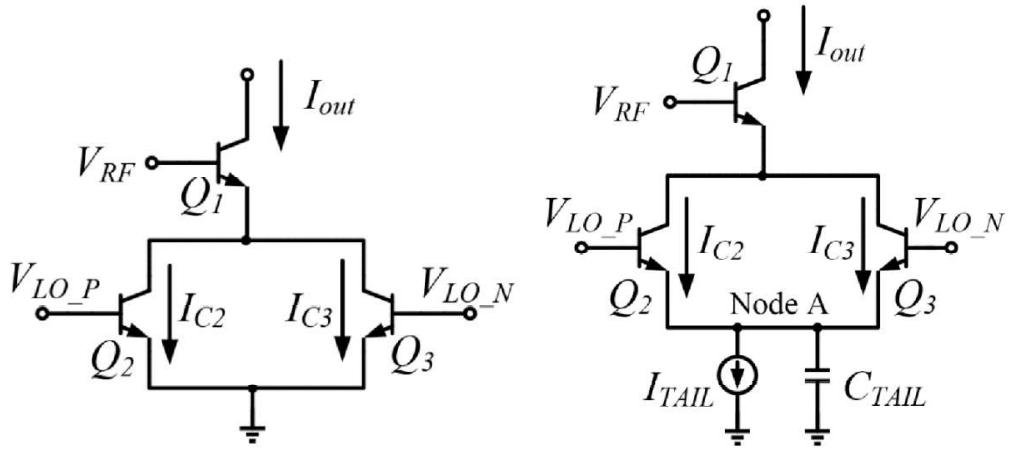


(a) (b)

Figure 4-8. (a) Simplified schematic of the conventional top-LO-configured CECCTP SHM. (b) Modelling of the LO frequency doubling stage.

3.3.1-b) Improvedbottom-LO-configured CECCTP SHM

Figure 4-9 shows the simplified schematic of the core of the bottom-LO-configured CECCTP SHM. Since the common emitter point of Q2 and Q3 is connected to ground, the CECCTP effectively enlarges the generation of 2* f_{LO} for mixing. Since this is a voltage-biased structure and the base-to-emitter bias voltage of Q2 and Q3 are constant, DC and 2*f_{LO} component of I_{out} are very sensitive to LO power. Hence, a tail current source is employed to stabilize the DC biascurrent, as shown in Fig. 2(b). Large shunt capacitor (C_{TAIL}) provides an ACground. This is a current-biased structure, and the potential of node A is floated. Thus, the base-to-emitter bias voltage (V_{be_bias}) of Q2 and Q3 could be adaptively changed to keep DC component of I_{out} constant and to flatten the 2*f_{LO} generation.



(a) (b)

Figure 4-9. Simplified schematic of the (a) bottom-LO-configured CECCTP SHM. (b) bottom-LO-configured CECCTP SHM with tail current source.

3.3.1-b) Comparison of the SHMs with top and bottom LO configurations

Figure 4-10shows the simulated load-lines of the HBT Q1 (solid line) in the top-LO-configured SHM in Fig. 1(a) and that of the HBT Q1 (dotted line) in the bottom-LO-configured SHM in Fig. 2(b), respectively. Since RF input is small signal and LO input is large signal, both SHMs are applied with no RF power and an LO power of -7 dBm at 39.5 GHz to simulate the load-lines of HBT Q1. In the top-LO-configured SHM, the 2*f_{LO} modulates the collector-to-emitter voltage (V_{ce}) andcollector current (I_c) of Q1. The RF stage operates between the saturation and slightly forward active region and generates the f_{IF} signal.In the bottom-LO-configured SHM, the 2* f_{LO} modulates the base-to-emitter voltage (V_{be}) and collector current (I_c) of Q1. The RF stage operates in the forward active region and generates thef_{IF} signal. When the LO power is low, the bottom-LO-configured SHM generates higher 2* f_{LO} current swing than the top-LO-configured one, as shown in Fig. 3.

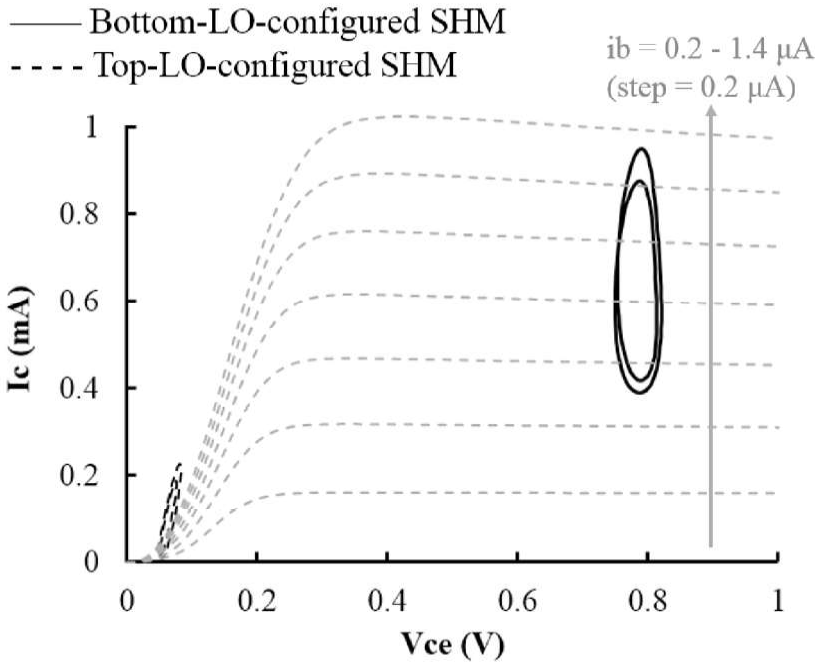


Figure 4-10.Simulated load-lines of the HBT Q1 (RF stage) in the SHMswith top and bottom LO configurations.

4.2.2 Bottom-LO-configured SHMs with and without a tail current source

In order to quantitatively analyze the differenceof the 2* f_{LO} generation between the circuitsin Figure 4-9(a) and Figure 4-9(b), the collector current (I_c) of HBT is modeled as a train of rectified cosine pulses. Figure 4-11shows the calculated time-domain waveforms of the collector current and base voltage in the CECCTP stage. I_{max} is the peak current of I_c. I_{C2} and I_{C3} refer to the collector current of Q2 and Q3, respectively. V_{be2} and V_{be3} refer to the base-to-emitter voltage of Q2 and Q3, respectively. V_{be_max} and V_{be_min} refer to the HBT base-to-emitter voltage swing,V_{be_on} is the threshold voltage of HBT, t_0 is the width of the current pulses, and T is the period of the fundamental frequency.

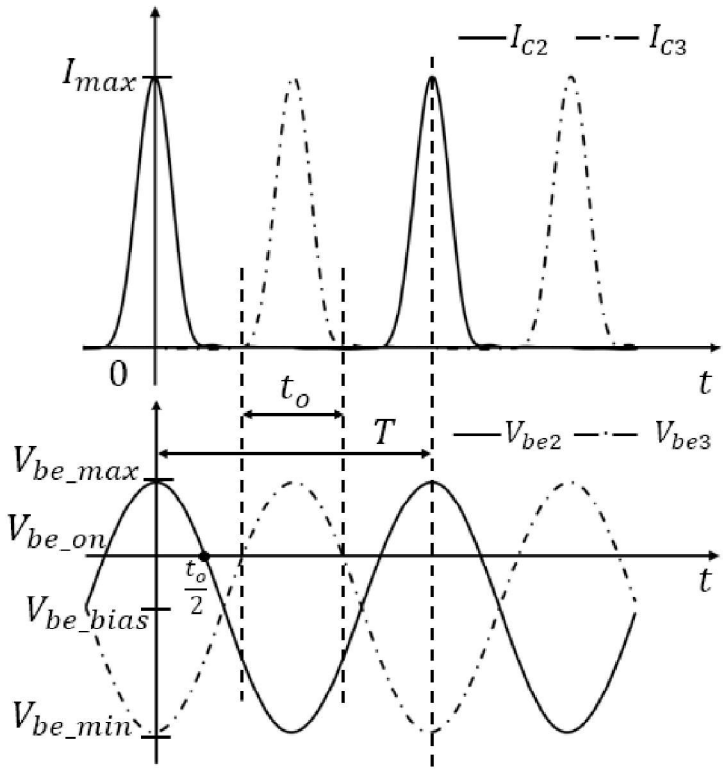


Figure 4-11. Collector current and base voltage time-domain waveforms in the CECCTP frequency doubling stage.

I_{out} can be represented using a Fourier-series expansion:

$$I_{out}(t) = I_{C2} + I_{C3} = I_o + I_1\cos(w_1 t) + \cdots + I_n\cos(w_n t) \quad (4\text{-}4)$$

where I_n is the nth-harmonic current component. The DC component I_0 in I_{out} is:

$$I_0 = I_{max}\frac{2\theta_t}{\pi^2} \quad (4\text{-}5)$$

and the second harmonic (I_2) in I_{out} is:

$$I_2 = I_{max}\left|\frac{\theta_t\cos(\theta_t)}{\pi^2/4-\theta_t{}^2}\right| \quad (4\text{-}6)$$

where θ_t is the conduction angle. When t increases from 0 to $t_0/2$, V_{be2} decreases from V_{be_max} to V_{be_on}, as shown in Figure 4-11:

$$(V_{be\_max} - V_{be\_bias}) \times \cos\left(\frac{2\pi}{T} \times \frac{t_0}{2}\right) = V_{be\_on} - V_{be\_bias} \quad (4\text{-}7)$$

Hence, θ_t can be expressed as a function ofV_{be_bias},input power of LO signal (P_{LO}) and the input impedance of CECCTP frequency doubling stage (R_{LO}):

$$\theta_t = \frac{2\pi t_0}{T} = 2\cos^{-1}\left(\frac{V_{be\_on}-V_{be\_bias}}{V_{be\_max}-V_{be\_bias}}\right) = 2\cos^{-1}\left(\frac{V_{be\_on}-V_{be\_bias}}{\sqrt{2P_{LO}\times R_{LO}}}\right) \quad (4\text{-}8)$$

For simplicity, thetransconductance performance of HBT is assumed to be constant when input power changes. Thus, current swing I_{max} is proportional to the voltage swing V_{be_max} -V_{be_on}:

$$I_{max} = g_m(V_{be\_max} - V_{be\_on}) = g_m\left(1 - \cos\frac{\theta_t}{2}\right)\sqrt{2P_{LO} \times R_{LO}} \quad (4\text{-}9)$$

Since V_{be_bias} is constant in Figure 4-9(a), θ_t drastically increases when P_{LO} increases, as shown inequation (4-8). From equations (4-6)and (4-9), I_2 can be expressed as:

$$I_2 = g_m\sqrt{2P_{LO} \times R_{LO}} \times \theta_t\left(1 - \cos\frac{\theta_t}{2}\right) \times \left|\frac{\cos(\theta_t)}{\pi^2/4-{\theta_t}^2}\right| \quad (4\text{-}10)$$

Since I_0 is constant (I_0=I_{TAIL}) and V_{be_bias} is floated in Figure 4-9, V_{be_bias} decreases and θ_t slightly decreases when P_{LO} increases, as shown in equation (4-5). From equations (4-5)and (4-6), I_2 can be expressed as:

$$I_2 = I_{TAIL}\frac{\pi^2}{2} \times \left|\frac{\cos(\theta_t)}{\pi^2/4-{\theta_t}^2}\right| \quad (4\text{-}11)$$

The I_2 in equation(4-10)has additional polynomials about θ_t and P_{LO}, compared with the I_2 in equation (4-11). Hence, a tail current source could make I_2 (2*f_{LO} in I_{out}) insensitive to θ_t, and meanwhile could make I_2 insensitive to P_{LO}.It is expected that the SHM with the tail current source inFigure 4-9(b)generates 2* f_{LO} more smoothly than the SHM inFigure 4-9(a).

Figure 4-12shows the simulated dependence of 2* f_{LO} (I_2) in I_{out} on the LO input power in the conventional top-LO-configured SHM (gray solid line), the bottom-LO-configured SHM without I_{TAIL} (black dashed line) and the improved bottom-LO-configured SHM with I_{TAIL} (black solid line). Differential LO signal at 39.5 GHz is applied to the CECCTP frequency doubling stage. The improved SHM in Fig. 2(b) effectively enlarges and flattens the 2*f_{LO} in I_{out} with low LO input power range.

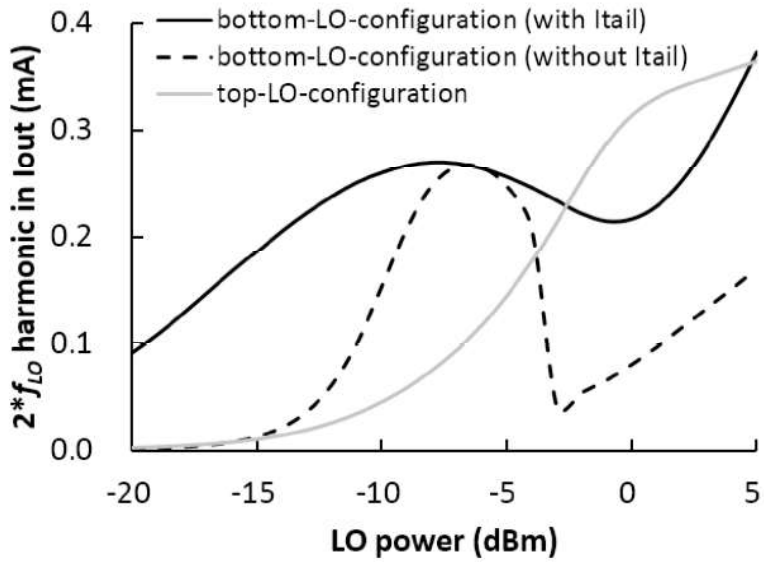


Figure 4-12. Magnitude of the $2*f_{LO}$ of *Iout*.

4.3 Circuit design

4.3.1 Schematicof VCO ICs

Figure 4-13shows the schematic of the bottom-LO-configured SHM IC with a tail current source presented in this paper. HBTsQ1, Q2, Q3, Q4 and Q5 form the SHM core, where Q4 and Q5 serve as the tail current mirror. The supply voltage for the SHM core is 3.3 V. A one-stageemitter follower with a supply voltage of 1.8 V is employed as the IF buffer amplifierto drive a 50 Ω load.For on-wafer measurements, integrated Marchand balun is designed at the LO input port to transfer the differential balanced 50 Ω port to a single-ended unbalanced 50 Ω port. Since the center frequenciesof LO and RF signals are 39.5 GHz and 80 GHz, respectively, spiral inductors are utilized for the LO matching circuit and a microstrip line is used for the RF matching circuit.

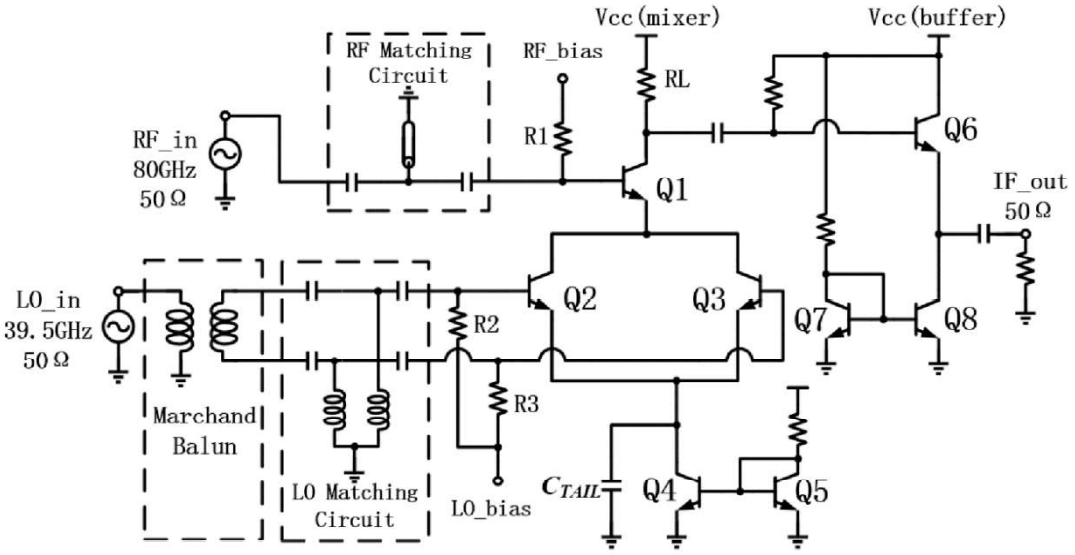


Figure 4-13.Schematic of theimproved bottom-LO-configured CECCTP SHM IC with tail current source.

For comparison,the conventional top-LO-configured CECCTP SHM IC is also designed, as shown in Figure 4-14. HBTs Q1, Q2 and Q3 form the SHM core. The supply voltage for the conventional SHM core is 2.5 V.Both theimproved and conventionalSHMs employ the same IF buffer amplifiers.

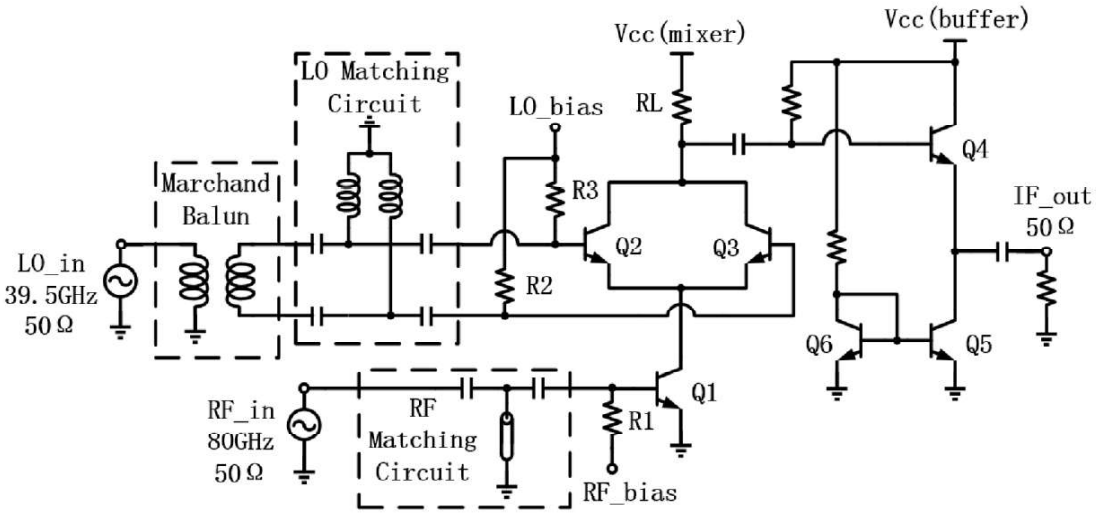
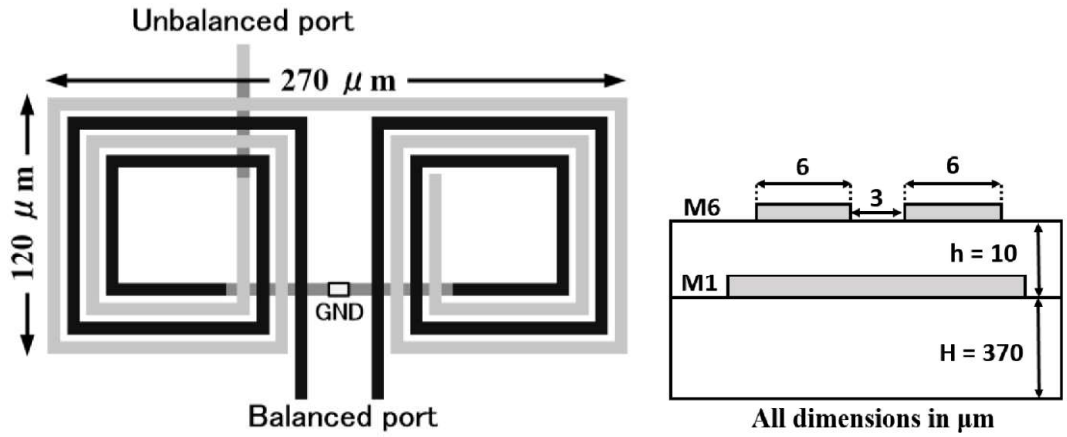


Figure 4-14. Schematic of the conventional top-LO-configured CECCTP SHM IC.

4.3.2 Marchand balunand layoutdesign

Figure 4-15(a) and (b) illustrate the top and side view of the Marchand Balun IC design, respectively. As shown in Figure 4-15(a), a pair of spiral transmission lines are

employed for magnetic coupling and port transformation. As shown in Figure 4-15(b), the microstrip line consists of a signal line in the top metal M6 and a ground plane in the bottom metal M1.The M1 and M6 are separated by a 10μm thick dielectric material. It is noted that the line width, line space and dimension have large influence on the balun performance. Ifthe line width is decreased, the size of balun is reduced and the parasitic capacitance between M1 and M6 is decreased, however, the line resistance is increased. If the line space is decreased, magnetic coupling and capacitive coupling between the balanced and unbalanced lines are increased simultaneously. The dimension of the balun influences the length of the transmission line and shifts the operational frequency. The Marchand Balun is simulated and optimized by electro-magnetic solver, Momentum. Thus, the line width and space are optimized to 6 μm and 3 μm, respectively, as depicted in Figure 4-15(b). The dimension is optimized to 270-μm length (L) and 120-μm width (W) as shown in Figure 4-15(a).



(a) (b)

Figure 4-15.(a) Top view and (b) sideview of the Marchand balun IC.

To compare the simulated and measured performance of the Marchand balun, the balun is designed and simulated with the RF pads for on-wafer probing. Figure 4-16(a) illustrates the layout of balun and Figure 4-16(b) shows the 3D image of the current distributionof the balun in Momentum EM simulation.

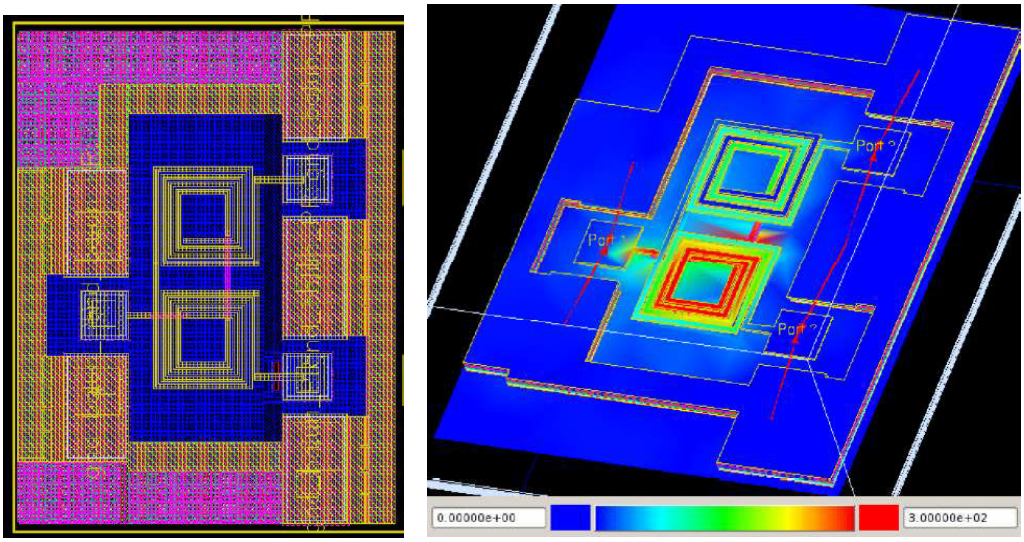
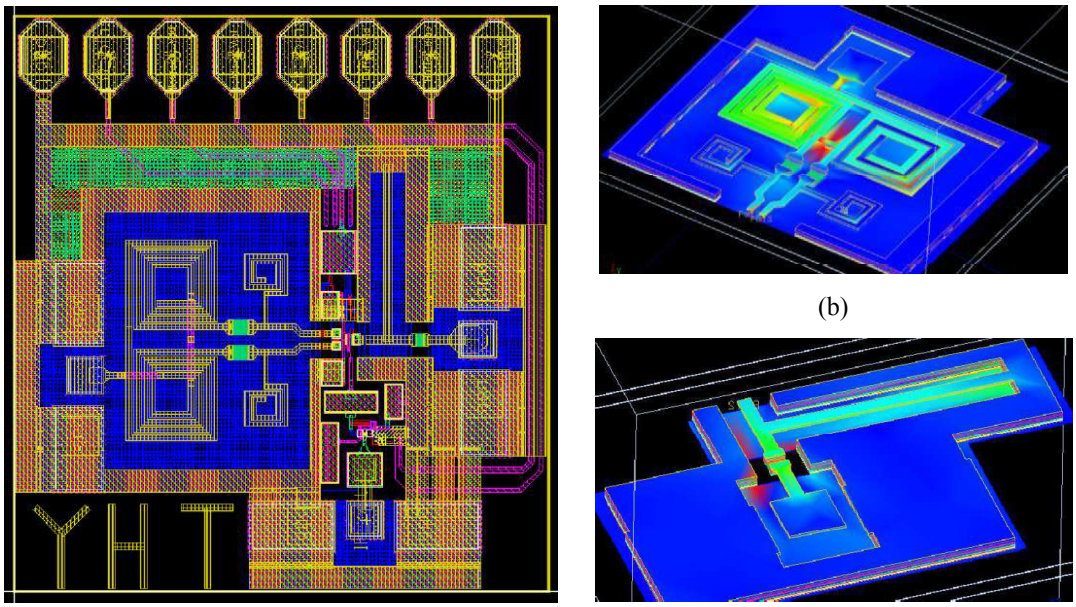


Figure 4-16. (a) layout of the Marchand balun with RF probes. (b) 3D image of current distributionof Marchand balun in Momentum EM simulation.

Figure 4-17(a)shows the layout of the improved bottom-LO SHM IC. Figure 4-17(b) and Figure 4-17(c) depict theMomentum 3D image of the LO and RF matching circuits, respectively. The design procedure for passive matching circuit is initially designing each devices, such Marchand balun, MOM capacitors and spiral inductors with EM simulation. After combining the individualdevices in schematic and matching input impedance to 50 Ω, all the devices are put together in layout as a whole matching circuit. Finally the performance of the entire LO and RF matching circuits are simulated and optimized by EM simulation, as shown in Figure 4-17(b) and (c).

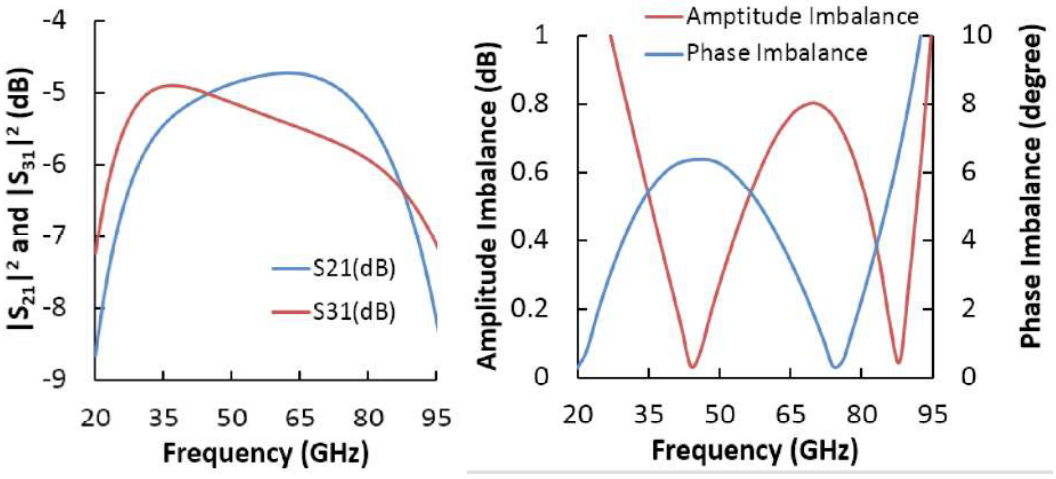


(a) (b) (c)

Figure 4-17. (a) layout of the improved bottom-LO-configured SHM IC, Momentum 3D image of (b) LO matching circuit and (c) RF matching circuit.

4.3.3 Simulated performance

Figure 4-18(a) shows the measured insertion loss performance. From 26 to 66 GHz, the balun IC exhibits measured insertion loss of less than 3 dB. Figure 4-18(b) illustrates the measured imbalance performance. From 20 to 66 GHz, the amplitude imbalance is less than 0.9 dB and the phase imbalance is less than 2.5 degrees.



(a) (b)

Figure 4-18.Simulated(a) insertion loss and (b)amplitude and phase imbalance.

Figure 4-19shows the simulated dependence of the conversion power gain of both SHM ICs on the LO power. The frequencies of RF, LO and IF signals are 80 GHz, 39.5 GHz and 1 GHz, respectively. The RF power is fixed to -40 dBm, and LO power (P_{LO}) is swept from -20 to 10 dBm.The improved SHM in Figure 4-13has a conversion power gain of 6.9 dB (including the buffer gain) at P_{LO} =-7dBm. The core circuit of the improved SHM (without the buffer) consumes a DC current of 0.64 mA at a supply voltage of 3.3 V. The conventional SHM in Figure 4-14requires P_{LO} =-1.5 dBm to have similar conversion power gain of 6.7 dB (including the buffer gain). The core of the conventional SHM (without the buffer) consumes a DC current of 0.27 mA at a supply voltage of 2.5 V. The dependence of the conversion gain on the LO poweris similar to that of 2* f_{LO} in I_{out} shown in Figure 4-12. In the top-LO-configured SHM, since the RF stage is the emitter degeneration for LO stage and the generation of 2*f_{LO} is critically suppressed, the conversion gain is lower than that of the bottom-LO-configured SHM with P_{LO} lower than -2 dBm. In the bottom-LO-configured SHM, since the LO stage becomes the emitter degeneration for RF stage and the transconductance of RF stage is limited, the conversion gain is lower than that of the top-LO-configured SHM with P_{LO} higherthan -2 dBm. As shown in Figure 4-19, the conversion gain of the improved SHM is higher and less sensitive to the variation of P_{LO} than that of the conventional one under P_{LO} less than -2 dBm.

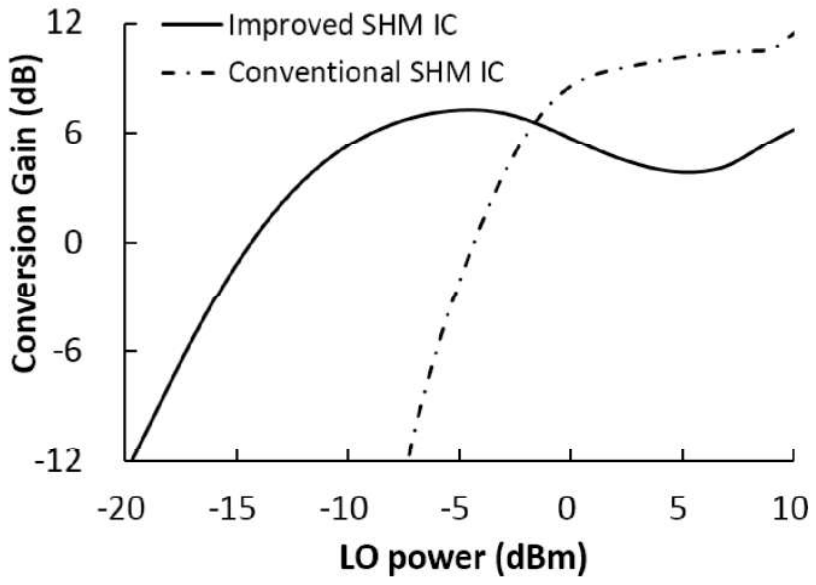


Figure 4-19.Simulated dependence of the conversion gain on LO power.

Figure 4-20shows the simulated Double Side Band Noise Figure (DSB NF) of both SHM ICs with sweeping the LO power from -20 to 10 dBm. The frequencies of RF, LO and IF signals are 80 GHz, 39.5 GHz and 1 GHz, respectively. When P_{LO} is lower than 0 dBm, the DSB NF of the improved SHM is much lower than that of the conventional SHM.

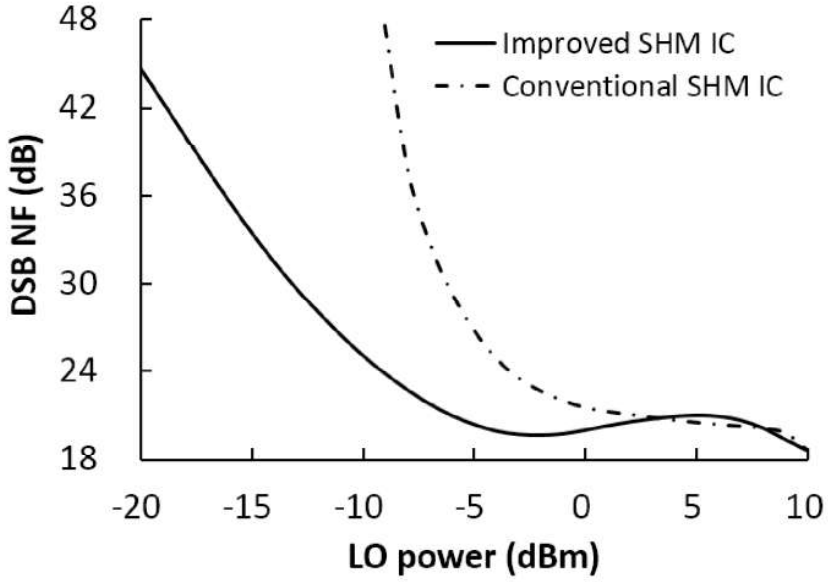


Figure 4-20. Simulated dependence of theDSB NF on LO power.

Since the noise coming from the tail current source (Q4 and Q5) is shunted by the C_{TAIL}, the tail current source has only 6.4 % noise contribution. Figure 4-21shows the dependence of conversion gain and DSB NF on the C_{TAIL} of the improved SHM. The conditions for the simulation are the same as those for the noise contribution simulation. As shown inFigure 4-21, a large C_{TAIL} for AC ground is necessary to increase the conversion gain and decrease the DSB NF. Consequently, C_{TAIL} is chosen to 10 pF in the improved SHM circuit. The C_{TAIL} for AC ground decreases the common-mode rejection of the tail current source and might be a source of instability for a common-mode signal. It is confirmed that the SHM IC is stable from the transient simulation with sweeping LO power.

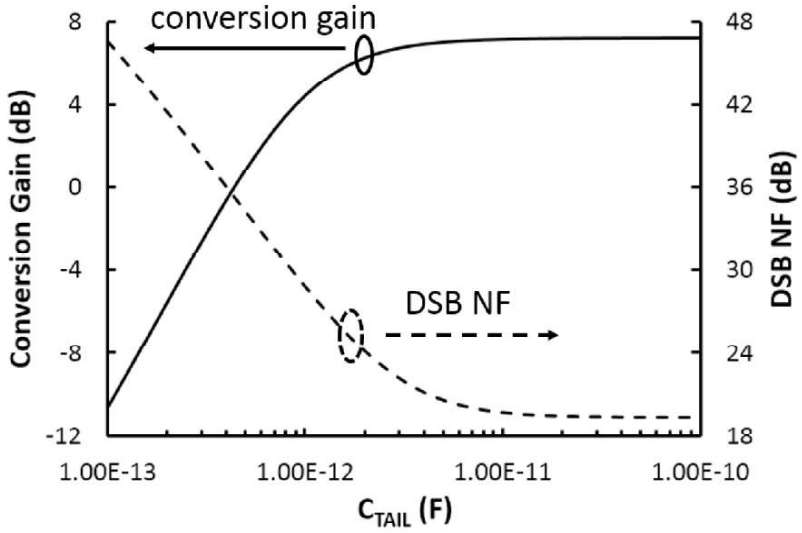
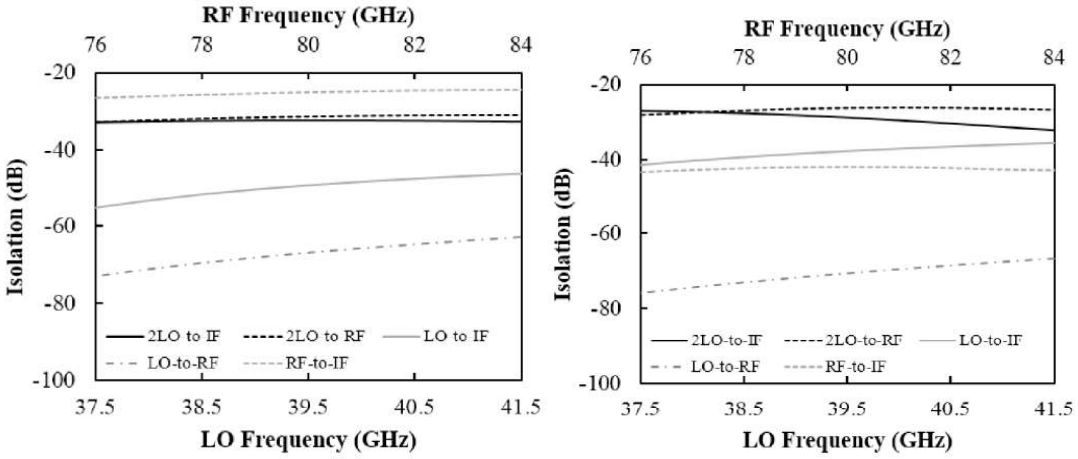


Figure 4-21. Simulated conversion gain and DSB NF of the improved SHM vs. C_{TAIL}.

Figure 4-22shows the simulated port-to-port isolation, including the 2LO-RF, LO-RF at the RF port and the RF-IF, 2LO-IF, LO-IFat the IF port of the (a) conventional and (b) improved SHM ICs. The isolations are simulated as a function of LO frequency (f_{LO}). The f_{LO} is swept from 37.5 – 41.5 GHz and the f_{RF} is correspondingly changed from 76 – 84GHz to keep the f_{IF} fixed to 1 GHz. Both two SHMs are applied with the RF power of -40 dBm. The conventional and improved SHMs are applied with the LO power of -1.5 dBm and -7 dBm, respectively. Both SHMs have excellent LO-RF isolation as a result of the CECCTP structure of the LO stage and the balance of the balun.



(a) (b)

Figure 4-22.Simulated isolation of the (a) conventional SHM and (b) improved SHM vs. LO and RF frequency (f_{IF} = 1 GHz).

Figure 4-23shows the simulated input-output response of the conventional and improved SHM ICs.The frequency conditions for the simulation are: f_{RF} = 80 GHz,f_{LO} = 39.5 GHz, f_{IF}= 1 GHz. The LO power of -1.5 dBm and -7 dBm are injected to the conventional and improved SHMs, respectively. The IP1dB and OP1dB of the conventional SHM are -27.0 dBm and -21.5 dBm. TheIP1dB and OP1dB of the improved SHM are -23.0 dBm and -17.0 dBm. In the conventional SHM, since the RF stage enters the saturation regionas shown in Figure 4-10, the voltage swing of the IF signal is suppressed. Thus, the IP1dB of conventional SHM is lower than that ofthe improved one.

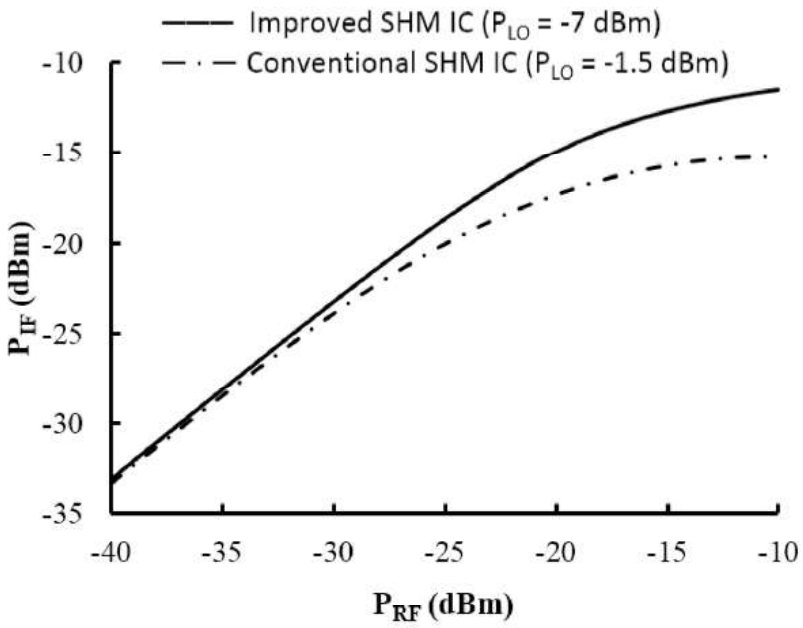


Figure 4-23.Simulated IF output power vs. RF input power.

Fig. 14 shows the simulated conversion gain of the conventional and improved SHMs as a function of the RF frequency. The f_{LO} is swept from 37.5 – 41.5 GHz and the f_{RF} is correspondingly changed from 76 – 84 GHz to keep the f_{IF} fixed to 1 GHz. The conventional and improved SHMs are applied with anLO power of -1.5 dBm and -7 dBm, respectively.

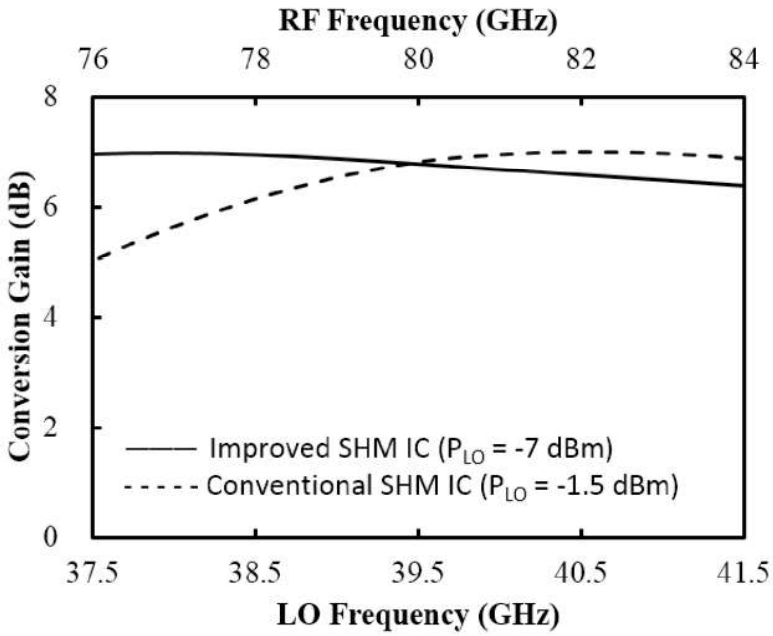


Figure 4-24.Simulated conversion gain vs. LO and RF frequency (f_{IF} = 1 GHz).

4.4 Measured performance

To confirm the performance of the Marchand balun, a balun IC is individually fabricated in 130-nm SiGe BiCMOS process. Figure 4-25shows the die photograph of the balun IC and the core size is only 270 μm by 120 μm.

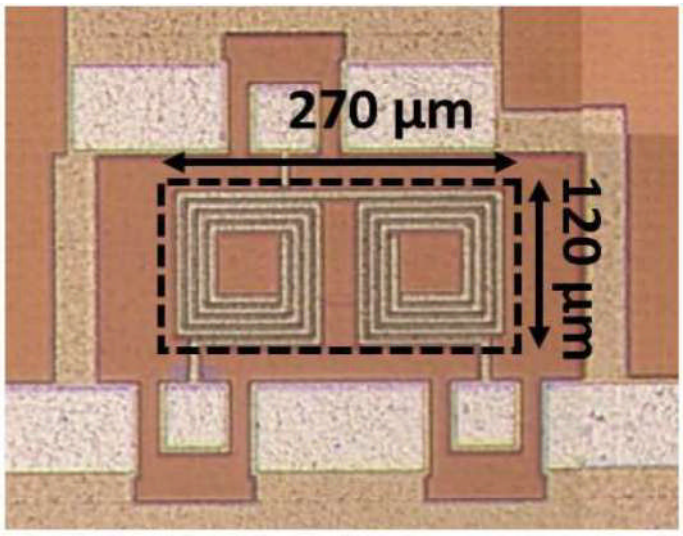
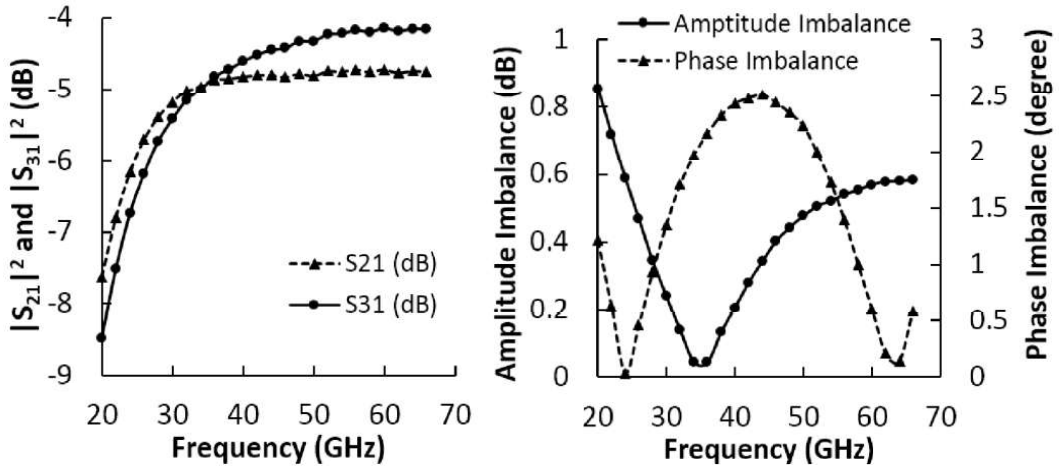


Figure 4-25.Die photograph of the Marchand Balun IC

Figure 4-26(a)shows the measured insertion loss performance. From 26 to 66 GHz, the balun IC exhibits measured insertion loss of less than 3 dB. Figure 4-26(b) illustrates

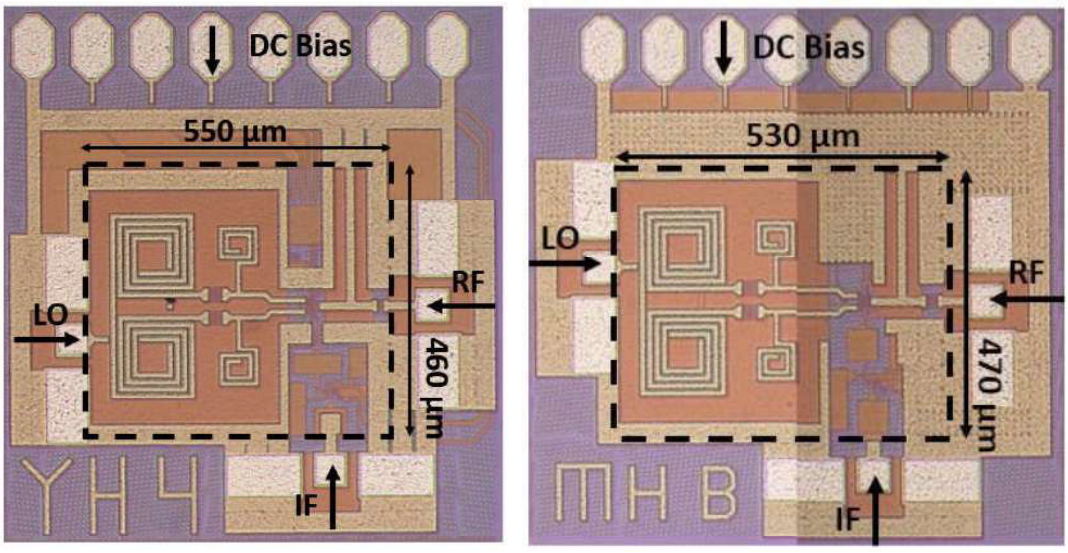
the measured imbalance performance. From 20 to 66 GHz, the amplitude imbalance is less than 0.9 dB and the phase imbalance is less than 2.5 degrees.



(a) (b)

Figure 4-26.Measured (a) insertion loss and (b) amplitude and phase imbalance.

Figure 4-27(a)shows the die photograph of the bottom-LO-configured CECCTP SHM ICwith a tail current source presented in this paper, which has a core size of 550 μm by 460 μm. In addition, the conventional top-LO-configured CECCTP SHM IC is fabricated for comparison, as shown in Figure 4-27(b).



(a) (b)

Figure 4-27.Die photograph of (a) the improved bottom-LO-configured SHM IC with a tail current sourceand (b) the conventional top-LO-configured SHM IC.

Figure 4-28shows the measured dependence of the conversion power gain of the improved and conventional SHM ICs on the LO power. The measurement was carried-out on-wafer with single-ended 50- Ω system. At an RF frequency of 80 GHz and an LO frequency of 39.5 GHz (IF output frequency is 1 GHz), the improved SHM IC achieves a conversion power gain of 3.9 dB and a DC power consumption of 2.2 mW at an LO power of only -7 dBm. Considering the insertion loss of the balun as shown in Figure 4-26(a), the actual input power is around -9 dBm. The conventional top-LO-configured one hasa conversion power gain of 1.9 dB with a power consumption of 1.1 mW at an LO power of -1.5 dBm.

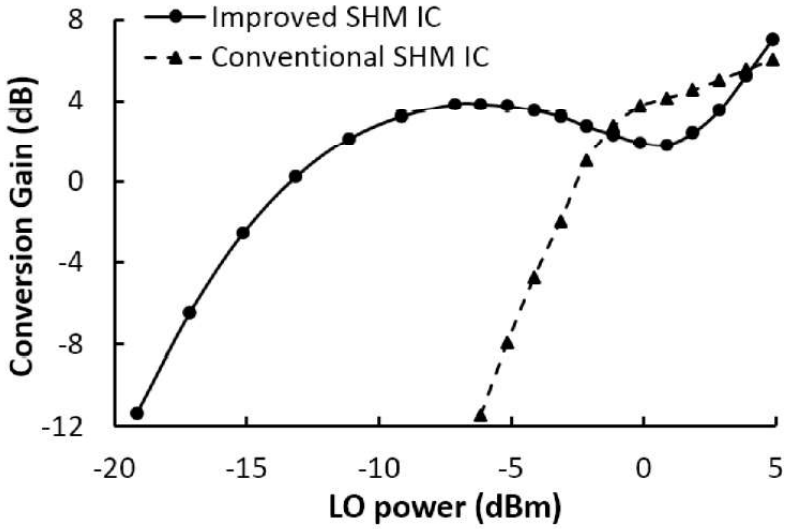
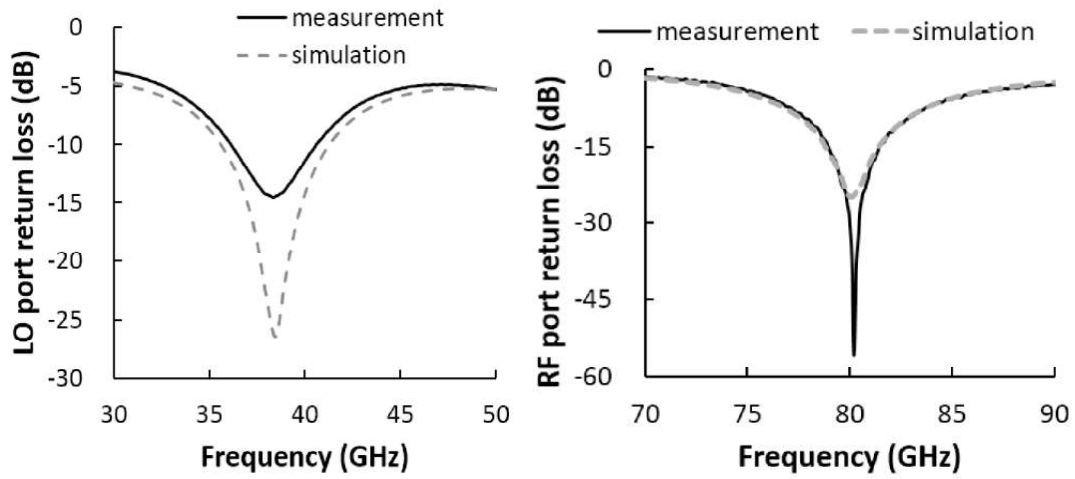


Figure 4-28.Measured dependence of the conversion gain on the LO power (conditions: f_{RF} = 80 GHz, f_{LO} = 39.5 GHz, f_{IF} = 1 GHz).

Figure 4-29shows the simulated and measured input return loss at (a) LO port and (b) RF port of theimproved SHM IC with -7 dBm LO input power injected. The return loss of the LO port is better than 10 dB from 36.1 to 40.6 GHz. The return loss of the RF port is better than 10 dB from 78 to 82.7 GHz. The measured return losses well agree with the simulation.



(a) (b)

Figure 4-29.Measured and simulated input return loss of the (a) LO port and (b) RF port of the improved SHM IC.

Figure 4-30depicts the simulated and measured IF frequency response of the conversion gain of the improved SHM IC. RF frequency is fixed to 80 GHz and RF power is fixed to -37 dBm. LO input power is fixed to -7 dBm and LO frequency is swept from 39.95 GHz to 39.25 GHz. Thus, IF frequency changes from 100 MHz to 1.5 GHz. When IF frequency is below 200 MHz, the conversion gain decreases with IF frequency decreasing because the capacitors are not large enough for DC block and AC ground. When the IF frequency is above 500 MHz, the conversion gain decreases with IF frequency increasing as a result of the frequency response of the buffer amplifier.

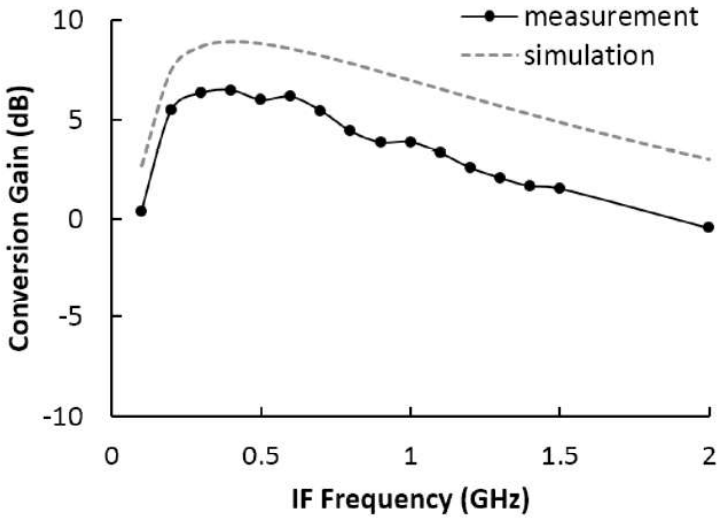


Figure 4-30. Measured and simulated conversion gain versus IF frequencyof the improved SHM IC (conditions: f_{RF} = 80 GHz, $f_{LO} = (f_{RF} - f_{IF})/2$, P_{LO} = -7 dBm).

Figure 4-31shows the simulated and measured input-output response of the improved SHM IC with an LO power of -7 dBm at 39.5 GHz. The frequencies of RF and IF signals are 80 GHz and 1 GHz, respectively. The measured IP1dB and OP1dB are -27 dBm and -25 dBm, respectively.

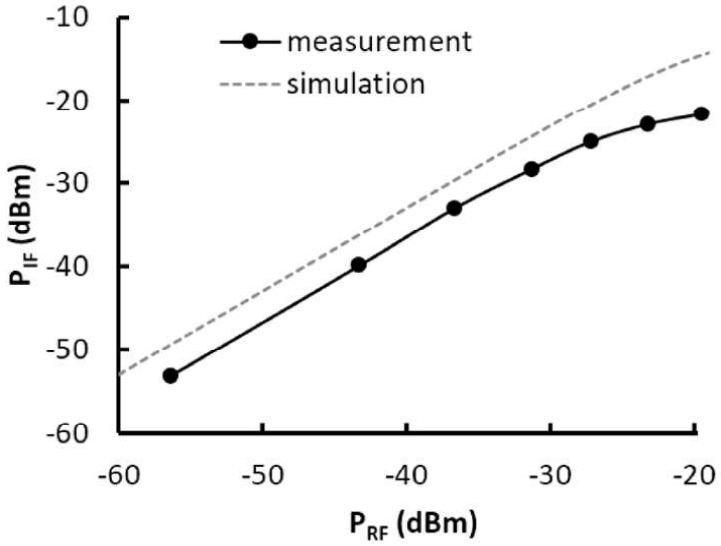


Figure 4-31. Measured and simulated IF power vs. RF power of the improved SHM IC (conditions: f_{RF} = 80 GHz, f_{LO} = 39.5 GHz, f_{IF} = 1 GHz, P_{LO} = -7 dBm).

Table 2 summarizes the measured performance of the fabricated CECCTP SHM ICs with previously published W-band SHM ICs. W-band SHM ICs utilizing the passive Sub-Harmonically Pumped (SHP) diode topology require high LO power and suffer from the conversion loss. Compared to the active SHMs in [4, 5, 15], the LO-bottom-configured SHM IC presented in this paper has exhibited higherconversion gain with lower LO power and ultra-low power consumption.

Table 2. Summary and comparison of the W-band SHM ICs

Ref	Process	fRF (GHz)	PLO (dBm)	Conversion Gain (dB)	DC power (mW)	Chip size (um * um)	Topologies
[3]	GaAs diode	90	10	-8	0	0.6*0.25	Passive diode
[4]	100-nm GaAs pHEMT	91	6	-2	12	1.4*0.8	Sub-harmonically pumped gate
[5]	0.8 μm SiGe BiCMOS	77	10	0.7 1)	22	0.9 * 0.86	Balanced SHM
[15]	90 nm CMOS	70	10	-1.5	58	0.61 * 0.58	Top-LO-levelled Gilbert-cell SHM
[23]	0.1 μm InP HEMT	94	2	-9.5	0	2.35 * 1.1	Passive diode
[24]	0.15 μm GaAs pHEMT	80	10	-10	0	1.5 * 2.0	Passive diode
[25]	0.15 μm GaAs pHEMT	77	7	-11	0	2.5 * 1	Passive diode
[26]	0.15 μm GaAs pHEMT	89	11	-4.7	0	1 * 2	Passive diode
[27]	1 um InP DHBT	83	6	1	N.A.	1.37 * 1.41	Active single HBT doubler & mixer
[28]	UMS BES Schottky diode	90	0	-13	0.	1.4 *1.4	Passive diode
[29]	Quasi-monolithic GaAs Schottky diode	90	10	-8	0	2.2 * 4.0	Passive diode
This work	130-nmSiGe BiCMOS	80	-7 2)	3.9	2.2	0.55 * 0.46	Novelbottom-LO-configured SHM with tail current source
		80	-1.5 2)	1.9	1.1	0.55 * 0.46	Previoustop-LO-configured SHM

1) Includes 11 dB gain of the IF buffer amplifier. 2) Includes 2 dB insertion loss of the balun.

4.5 Conclusion

In this chapter, aCECCTP SHM IC with a tail current source bias circuit and bottom-LO-configuration is proposed for W-band applications. The proposed SHM IC has been designed, fabricated using 130-nmSiGe BiCMOS processand testedon wafer.

In the previous top-LO-configured CECCTP SHM IC, large LO power is required to generate the $2*f_{LO}$ signal for mixing. In this work,LO stage is swapped from the top-LO configuration to bottom-LO configuration.Thus, the emitter degeneration of the LO stage is removed, which significantly decreases the LO power requirement of the SHM. Since the bottom-LO-configuration makes the conversion gain of SHM sensitive to the LO power, tail current sourcebias circuit parallel with large capacitor for ac ground is proposed. With the tail source bias circuit, the LO stage hasfloating Vgs bias

voltage and constantdc bias current. When LO power changes, the variation of conduction angle of LO stage is suppressed and the generation of $2f_{LO}$ signal is flatten. Thus, the SHM with tail current source has conversion gain insensitive to the LO power.

The SHM IC exhibits a measured conversion gain of 3.9 dB at 80 GHz with an LO power of only -7 dBm at 39.5 GHz. The DC power consumption of the SHM IC is only 2.2 mW. The measured performanceconfirmsthat the bottom-LO-configuration decreases the requirement of LO power and the tail current source makes the conversion gain insensitive to the variation of LO power. Therefore, the proposedSHM topology decreases the output power of LO buffer and removes output power control circuit of the LO buffer, which is effective to decreasethe power consumption of LO buffer. Considering that the LO buffer significantly influences the power consumption of transceiver, it is expected that the proposed topology could decrease the power consumption of transceiver.

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Chapter 5Conclusionsand Future Works

5.1 Conclusions of this dissertation

In this dissertation, adaptivebias techniquesare proposed to automatically change the bias conditions RF IC blocks and to decrease the power consumption.Three RF ICs withdifferent adaptivebias circuits including the VCO IC, PA IC and SHM IC are designed, fabricated and verified by measurement. The measurement performance confirms the effectiveness of the proposed adaptivebias circuits on decreasing the power consumption.

InChapter 2, an adaptivebias circuit is proposed to dynamically control the bias current ofthe SiGe HBT PAIC. With the utilization of an open loop common source feedback amplifier,the proposed adaptivebias circuitworks likea regulatorwith excellent DC sourcing capabilityandkeepsthe base-to-emitter (Vbe) bias voltage constant over the variation of RF input power. When RF input power is low, the bias circuit supplies low Ib and Ic, which decreases the power consumption and improves the efficiency ofPA. When RF input power is high, the bias circuitsufficientlysupplies high Ib and Ic, which increases the swing range of output current and improves the linearity of PA.

A 5-GHz band three-stage SiGe PA IC with the proposed adaptivebias circuithas been demonstrated in 350-nm SiGe BiCMOS technology for WLAN applications. Under 54 Mbps OFDM signal at 5.4 GHz, the PA IC has achieved a measured EVM of 0.9% with 284 mA DC current consumption at 17 dBm output power, andan EVM of 4.2% with 330 mA DC currentconsumption at 20.3 dBm output power. The measured linearity performance well satisfies the requirements of IEEE 802.11a WLAN standards and confirms the linearity improvement to PA IC by the proposed adaptive bias circuit. The measured performance confirms the effectiveness of the proposed adaptive bias circuit on decreasing the power consumption of PA IC.

InChapter 3, an amplitude feedback bias circuit is proposed to dynamically control the bias voltage ofthe CMOS VCO IC. Initially, the bias circuit supplies the LC-VCO withClass-AB bias for robust oscillation start-up. After oscillation, the bias circuit dynamicallydecreases the bias voltage and shifts the LC-VCO into low Vgs bias for steady low power oscillation.

A 2.4-GHz-band ultra-low-voltage VCO IC with the proposed adaptivebias circuit has been demonstrated using 65-nm CMOS process. Measurement resultsincluding a low power consumption of 0.58 mW, a phase noise of -111 dBc/Hz and an FOM of 181 dBc/Hz are achievedat a power supply of only 0.3 V.The measured performance confirms the effectiveness of the proposed adaptive bias circuit on decreasing the power consumption of VCO IC.

InChapter 4, a tail current source is proposed to dynamically control the Vbe bias of bottom-LO-configured SiGe HBT SHM IC. In this work,LO stage is swapped from the top configuration to bottomconfiguration. Thus, the emitter degeneration of the LO stage is removed, which decreases the LO power requirement of the SHM. Since the bottom-LO-configuration makes the conversion gain of SHM sensitive to the LO power, tail current sourcebias circuit parallel with large capacitor as ac ground is proposed to flatten the conversion gain. With the tail source bias circuit, the LO doubling stage has floating Vbebias voltage and constant dc bias current. When LO power changes, the variation of conduction angle inthe LO doubling stage is suppressed and the generation of $2*f_{LO}$ signal is flattened. Thus, the SHM with tail current source has conversion gain insensitive to the LO power.

A W-bandbottom-LO-configureddown-conversion SiGe HBT SHM IC with the proposed adaptivebias circuithas been demonstrated in 130-nm SiGe BiCMOS process. The SHM IC has exhibiteda measured conversion gain of 3.9 dB at 80 GHz with an LO power of only -7 dBm at 39.5 GHz. The DC power consumption of the SHM IC is only 2.2 mW. The measured performanceconfirmsthat the bottom-LO-configuration decreases the requirement of LO power and the proposed tail current source makes the conversion gain insensitive to the variation of LO power.The measured performance confirms the effectiveness of the proposed adaptive bias circuit on decreasing the power consumption of LO buffer.

In summary, chip fabrications and measurementshave confirmed that the proposed adaptive bias circuits are effective to decreasethe power consumption of PA, VCO and LO buffer.In the transceiver,PA is most power consuming block. VCO and LO buffer have significant power consumption.Consequently, it is expected that the proposed RF ICs with adaptive bias circuitscoulddecrease the power consumption of the transceiver for wireless communications.

5.2 Futureworks

Futureworkson the adaptivebias circuits will be considered toimprove the reliability of the adaptivebias circuitswhenthere are variations of process, voltage and temperature (PVT). Since the PVT characteristics of the CMOS devices and HBT device are quite different, the brief direction to design the adaptivebiascircuits with PVT compensationwill be independently described in the following.

5.2.1 Future workonbias techniques forPA IC

Future work of adaptivebias circuit for PAICpresented in Chapter 3 will be focus on improving the reliability of the regulatorbias circuit over the variations of PVT.A small numberof paper temperature compensation for HBT PA IC were reported [11], [12].In the future, the regular bias circuitwould be improvedby adding temperature compensationand improving the Power Supply Rejection Ratio (PSRR).

The transconductance (gm) of NPN HBT is:

$$g_m = \frac{I_S}{V_T} e^{\frac{V_{BE}}{V_T}} = \frac{qAT^{3-n}}{k} e^{\frac{q}{kT}(V_{BE}-V_{G0})} \propto T^{3-n} e^{\frac{V_{BE}}{T}} \quad (5\text{-}1)$$

where V_T is the thermal voltage and Is is the reverse saturation current of the base emitter diode, respectively. VBE is the base-to-emitter bias voltage of HBT. A is a temperature-independence quantity. V_{G0} is the band-gap voltage of silicon extrapolated 0 °K, n is dependent on the doping level in the base.It is noted by n ≈0.5 in the SiGe process and the influence of T^{3-n} on gm is much larger than that of $e^{\frac{V_{BE}}{T}}$.

Figure 5-1shows an image of the dependence of gm on Vbe with temperature increasing from -40 to 120 °C(HBT with emitter finger length of 20 μm, finger width of 0.8 μm and emitter stripes of 3, and Vce = 3.3 V). When the temperature increases, gm dramatically increases. Hence, when temperature increases,Vbe of RF amplifying HBT should be decreased by the adaptivebias circuit to suppress the variation of gm and to maintain the power gain of PA. Since the gm is sensitive to Vbe bias voltage, the bias circuit should provide a constant Vbe bias voltage over the variation of supply voltage.It is noted that for the PA IC design in Chapter 2, the bias voltage of RF HBT as shown in Figure 2-9is:

$$V_{be} = V_{TH3} + \sqrt{\frac{2I_{REF}W_2L_1L_3}{\mu C_{OX}W_1W_3L_2}} \quad (5\text{-}2)$$

Hence, when temperature increases, the reference current (I_{REF}) should de decreased to decrease Vbe bias, to keep the HBT gm constant and to keep the PA gain constant.In addition, improving thePSRRof the bias circuit is also an important work in the future.

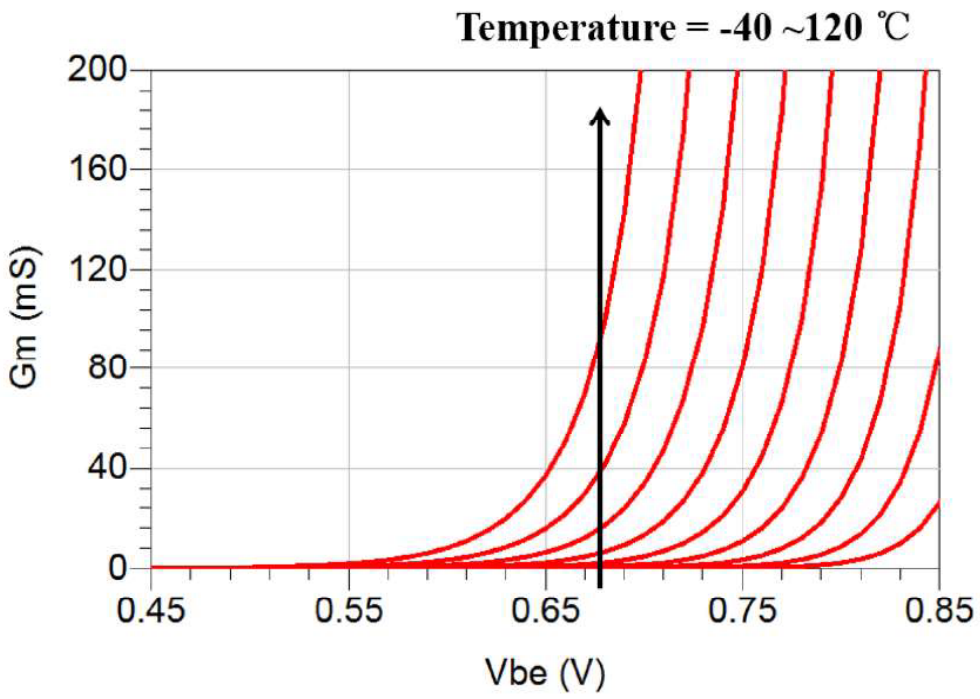

Figure 5-1. g_m of NPN HBT vs. Vbe with temperature increasing from -40 to 120 °C.

5.2.2 Future work on bias techniques for VCO IC

Future work ofadaptivebias circuit for VCO ICpresented in Chapter 2will be focus on improving the reliability of the amplitude feedback loop over the variations of PVT. The CMOS VCO ICs with temperature compensationoperating at a standard power supply (generally higher than 1 V) were previously reported in [1]-[9]. Few papers reported temperature compensation solutions for ultra-low-voltageVCO ICs. In the future, I will improve the amplitude feedback loop to make the bias voltage at the low power oscillation state dynamically changed over the PVT variations for ultra-low-voltage applications. The critical issue is how to make the transconductance of the cross-coupled nMOSFETs constant and to realize a reliable oscillation.

The transconductance (gm) of nMOSFET is:

$$g_m = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})(1 + \lambda V_{DS}) \quad (5\text{-}3)$$

where μ is the charge-carrier effective mobility.Cox is capacitance of the oxide layer. λ is the channel-length modulation parameter. V_{TH} is the threshold voltage of nMOSFET. V_{GS} and V_{DS} are the gate-to-source and drain-to-source bias voltage of the nMOSFET, respectively.

Figure 5-2shows an image of the dependence of gm on Vgs with temperature increasing from -40 to 120 °C. When the temperature increases, V_{TH} decreases and μ decreases. As shown in Figure 5-2, if the Vgs bias is low, gm increases with temperature increasing, which is mainly caused by the decrease of V_{TH}. If the Vgs bias is high, gm decreases with temperature increasing, which is mainly caused by the decrease of μ.

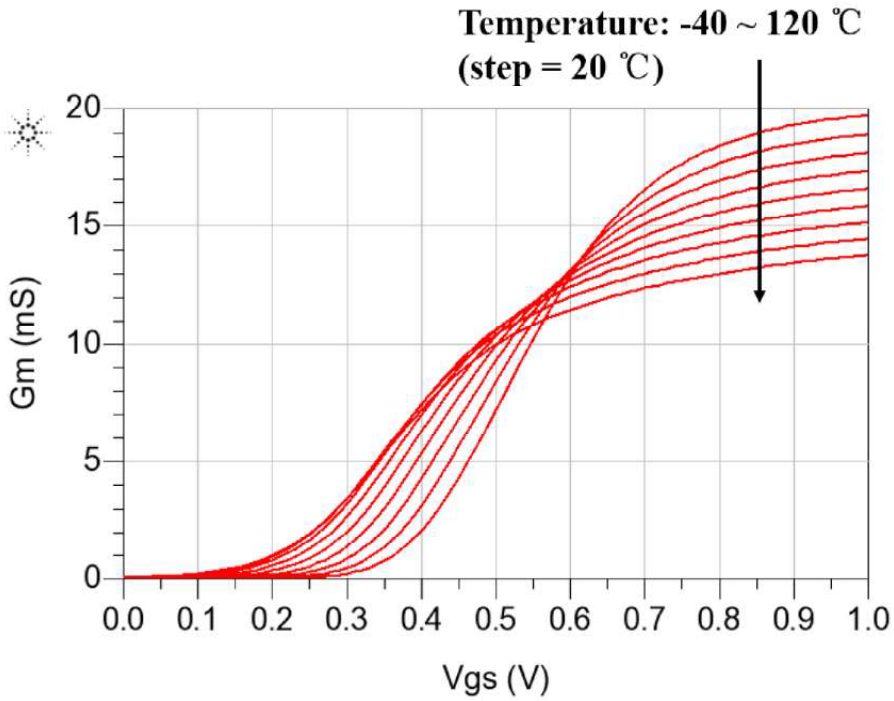

Figure 5-2. g_m of nMOSFET vs. Vgs with temperature increasing from -40 to 120 °C.

Considering the low power VCO IC in Chapter 2 is biased at low Vgs for steady oscillation, the bias voltage should be decreased to maintain the gm with temperature increasing. Similarly, the process variation mainly influences the VTH of transistor. If theprocess at FF corner, VTH are low and the bias voltage should be decreased should maintain the VGS-VTH. Vice versa, if the process at SS corner, the bias voltage should be increased. When the supply voltage (Vdd) increases, pMOSFET bias voltage should be increased simultaneouslywith Vdd and nMOSFET bias voltage should be keep

constant.

The paper [1]presents a considerable solution for the reliability improvement. However, temperature and voltage variation ranges in [1]are narrow and the process only contains the FF, SS and TT. Hence, further researchwill be conducted on how to provide a more accurate bias voltage to compensate PVT variations and cover all the process variations (FF, FT, FS, TF, TT, TS, SF, ST, SS).

In the frequency synthesizer, the control voltage for frequency tuning (Vctrl) of VCO is controlled by a Phase Locked Loop (PLL), and bias voltage (Vbias) of VCO is controlled by the proposed adaptive bias circuit (amplitude feedback loop). Hence, to ensure the operation of PLL, the settling time of adaptive bias circuitshould be shorter than the settling time of PLL. To decrease the settling time ofadaptive bias circuit, it is considerable to simplify the amplitude feedback loop with removing some dc level shifters and dc buffer amplifiers. In addition, decreasing the resistance and capacitance of the RC low-pass filter could also decrease the time constant (=RC) of filter and could decrease the settling time. However, decreasing RC increases the fluctuation of VCO bias voltage, which might decrease the stability of feedback loop and degrade the VCO phasenoise. Hence, the parameter of RC filter should be carefully designed by transient simulation.

5.2.3 Future work on bias techniquesfor SHM IC

Future work of adaptivebias circuit for SHM ICpresented in Chapter 4will be also focus on improving the reliability of the regulator bias circuit over the variations of temperatureHowever, the temperature compensation method for Chapter 3 and Chapter 4 are quite different.

In Chapter 3, the proposed bias circuit fixes the Vbe bias voltage of the RF amplifying HBT anddynamically increases the bias current with RF input power increasing. In the Chapter 4, the proposed tail current bias configuration fixes the bias current in the LO doubling stage of the bottom-LO-configured SHM IC, and dynamically decreasesthe Vbe bias voltage of the LO doubling HBTs to flatten the conversion gain with LO power increasing. Hence, the temperature compensation will be considered to control the bias current of the tail current source.The transconductance (gm) of NPN HBT in equation (5-1)can also be expressed as:

$$g_m = \frac{I_C}{V_T} = \frac{qI_C}{kT} \tag{5-4}$$

Figure 5-3shows an image of the dependence of gm on Vbe with temperature increasing from -40 to 120 °C (HBT with emitter finger leng th of 10 μm, finger width of 0.12 μm and emitter stripes of 1, and Vce = 1.2 V). When the temperature increases, gm with the same Ic bias slightly decreases. Hence, when the temperature increases, thetail current source should increase bias current of the SHM IC to maintain the gm of the LO doubling HBT and to make the 2* f_{LO} generation and conversion gain insensitive to the temperature variation.

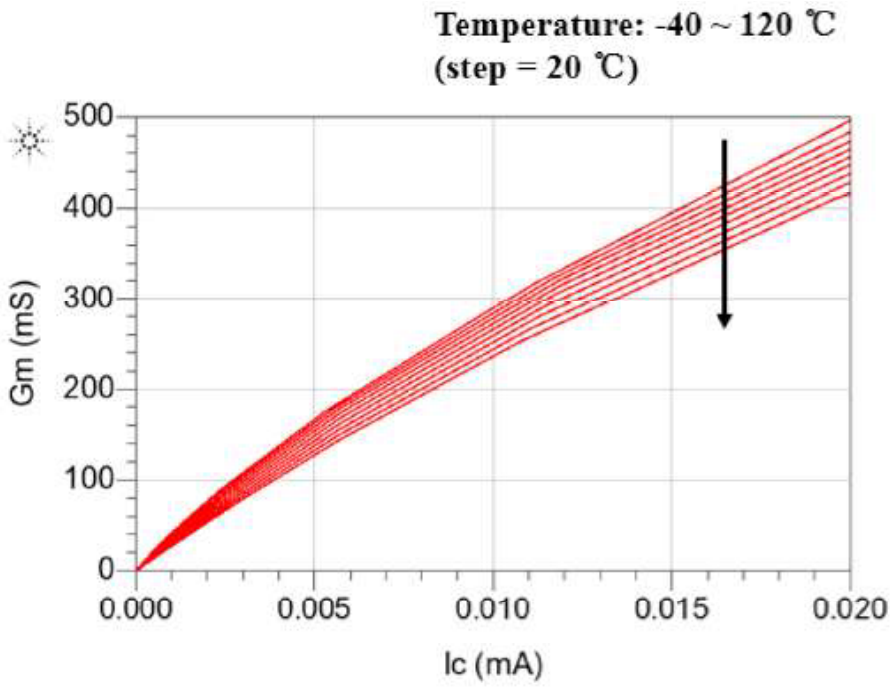

Figure 5-3. g $_m$ of NPN HBT vs. Ic with temperature increasing from -40 to 120 °C.

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