Study on Numerical Integration Algorithms and Time-Step Control Methods in Pseudo-Transient Analysis for Solving Nonlinear DC Circuit Equations

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Abstract

Recently, engineering productivity in integrated circuit product design and development is limited largely by the effectiveness of the computer-aided design (CAD) tools, in which the SPICE-like simulators are perhaps the most important one. The circuit simulation includes three parts: (a) model circuit devices mathematically, (b) form equations for the circuit, and (c) solve these equations with numerical analysis algorithms. As circuits of more complexity and mixed types of functionality, these equations are much more difficult to be solved. Therefore, the study on improving the convergence of the numerical analysis algorithms for solving the integrated circuit equations is an important task.

Nowadays, the pseudo-transient analysis (PTA) methods are considered as the most practical methods. All the studies in PTA previously published are from the pseudo-element viewpoint. To improve the PTA method from the different viewpoint (numerical integration algorithm viewpoint), (1) a PTA method using numerical integration algorithms with artificial damping is proposed. Moreover, (2) a switching algorithm, and (3) a time-step control method for the new PTA method are proposed. All the proposed methods are implemented on our spice simulator, Waseda SPICE (WSPICE), and they have been applied to the practical large-scale analog circuits to verify the effectiveness.

The dissertation contains the following five chapters.

Chapter 1 "Introduction" presents the background of the circuit simulation. The circuit analysis modes in the circuit simulators are introduced, in which the Direct Currents(DC) analysis is the most fundamental task. Then, the formulation of nonlinear circuit equations for DC analysis is reviewed. After that, the drawbacks of the conventional continuation methods for solving the nonlinear DC equations including source stepping, Gmin stepping and pseudo-transient analysis

(PTA) methods are analyzed. As the most promising method from the practical viewpoint, all conventional PTA methods are reviewed. At last, the challenges and innovation of my study are described.

Chapter 2 "Preliminaries" introduces some important methods in DC analysis, including the numerical integration methods and the artificial numerical damping. After that, the conventional time-step control methods used in circuit simulator are reviewed including local truncation error (LTE) method, iteration count method, and switched evolution/relaxiation (SER) method. At last, the convergence of PTA method is analyzed.

Chapter 3 "A PTA Method Using Numerical Integration Algorithms with Artificial Damping for Solving Nonlinear DC Circuit Equations" proposes a new PTA method and an effective switching algorithm. All the previous studies are from the pseudo element viewpoint. However, the use of capacitors in pure pseudo element is easy to convert the target circuit into an oscillator, which causes the oscillation problem. The use of time-varying resistor in compound pseudo element might cause the discontinuity problem. To solve the oscillation problem and discontinuity problem simultaneously, damped pseudo-transient analysis (DPTA) is proposed from the different viewpoint (numerical integration algorithm viewpoint). The k-step damped differential formulas (DDF-k) used in DPTA artificially enlarge the damping effect in the numerical integration algorithms to weaken the oscillation. Besides, capacitors and inductors are used only as the pseudo-elements, so that the proposed DPTA method has no discontinuity problem. Furthermore, an effective switching algorithm for the DPTA method is proposed to improve the convergence and efficiency. It automatically switch among different numerical integration algorithms to obtain varying degrees of damping effect. To verify the effectiveness, the proposed algorithms are implemented on our spice simulator WSPICE and applied to practical large-scale analog circuits (the

number of devices > 1000). Numerical examples demonstrate that the proposed methods solve the oscillation and discontinuous problems. With the proposed method, 100% test circuits in INOUE Lab. are solved (62/62). Compared with conventional PTA methods, DPTA has $0.81X \sim 4.79X$ speedup of CPU time. Among them, using DPTA for the practical and large-scale circuit (1516 MOS-FETs), the CPU time has 4.79X speedup, and the number of NR iterations is reduced to 18.03% of the iterations by using CEPTA.

Chapter 4 "An Adaptive Time-Step Control Method in Damped Pseudo-Transient Analysis for Solving Nonlinear DC Circuit Equations" proposes an adaptive time-step control method for DPTA. At the beginning, the features of DPTA are analyzed. The whole procedure of DPTA is divided into searching phase and converging phase. For each phase, the demands of time-step size are quite different. Based on these demands, the new time-step control method considers the residuals of pseudo-circuit equations, the relative change of node voltages and currents, and the iteration count of Newton-Raphson together to predict the circuit state at the next pseudo-step. The proposed method adapts the time-step size without constant upper limit, which means that it obtains the damping effect as large as possible. Moreover, the proposed method has a wider applicability to the pseudo-capacitor value since it can automatically and effectively adapt the time-step size according to the circuit state during the simulation. Compared with conventional DPTA, the proposed method has $0.86X \sim 104.82X$ speedup of CPU time. Compared with conventional SER, the proposed method has $1.22X \sim 76.34X$ speedup of CPU time. It is also proved that, DPTA with the proposed time-step control method has the ability to 100% solve all test circuits in INOUE Lab. and the benchmark circuits (113/113). Moreover, the robustness of DPTA is enhanced. Compared with other time-step control methods, the proposed method can expand the range of capacitor value used in the pseudo-element.

Chapter 5 "Conclusions" concludes the dissertation and gives the future works.

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Chapter 1

Introduction

Recently, engineering productivity in integrated circuit product design and development is limited largely by the effectiveness of the computer-aided design (CAD) tools, in which the SPICE-like simulators [7, 8, 9, 10] are perhaps the most important one. The circuit simulation combines (a) mathematical modeling of the circuit devices, (b) formulation of the circuit equations, and (c) numerical analysis algorithms for solution of these equations. As circuits of more complexity and mixed types of functionality, these equations are much more difficult to be solved. Therefore, the study on improving the convergence of the numerical analysis algorithms for solving the integrated circuit equations is an important task. For the circuit simulation, the most important and difficult task is to find the DC operating point of the nonlinear resistive circuit in DC analysis. All other analysis types (AC analysis, transient analysis) need the result of DC analysis. In DC analysis, the numerical analysis algorithms are used to solve the system of nonlinear algebraic equations. The most typical algorithm is the Newton-Raphson (NR) method. This method has the very desirable property of quadratic convergence. However, it may fail to converge if the initial guess is not sufficiently close to the real solution [12, 13]. Nowadays, the pseudo-transient analysis (PTA) methods are considered as the most practical methods. The main idea of the PTA methods is to insert the pseudo-element (capacitor and inductor) into the original circuit to form a pseudo-circuit. So that the DC problems are converted to the transient problems. The efficiency of the conventional PTA methods, including constant pure PTA (ASTAP, 1973 [3]) and time-varying PTA (R. Wilton, 1993 [6]), is not satisfactory. Moreover, the insertion of the pure pseudo-element is easy to form an oscillator. To overcome the oscillation and time-consuming problems, the compound element PTA (CEPTA) method is proposed (Hong Yu, IEICE Trans 2006 [43]). After that, the improvement algorithms of CEPTA are proposed to further improve the convergence and efficiency (Zhou Jin, IEICE Trans 2013 [44]). The

effectiveness of the improved CEPTA method is verified by the practical and large-scale circuits. However, the convergence consideration of all CEPTA methods is based on the assumption that the solution curve is continuous. So that even the improved CEPTA method may fail to converge due to the discontinuity problem. Moreover, the robustness of the PTA methods need to be improved.

In this chapter, the background of circuit simulation is introduced. Firstly, circuit analysis modes are reviewed. Secondly, the formulation of nonlinear DC circuit equations is introduced. Thirdly, the drawbacks of the conventional continuation methods including source stepping, Gmin stepping, homotopy and PTA methods are analyzed. As the most promising method from the practical viewpoint, all conventional PTA methods are reviewed. Finally, the challenges and the innovation of my studies are presented.

1.1 Circuit Simulation

Circuit simulation techniques mainly include the mathematical modeling of the circuit elements, the formulation of the circuit equations and the methods for solution of these equations. The circuit equations are formulated and numerically solved by the simulator. An overall flow chart of circuit simulation is shown in Fig. 1.1.

Solving the system of nonlinear equations formulated by the simulator is not easy, so that some less direct methods is needed. These less direct methods include the Newton-Raphson (NR) method and many continuation methods. There are many limitations which make the NR method non-convergence. Also, some discontinuous phenomenons cause non-convergence problem for the continuation methods.

1.1.1 Circuit Analysis Modes

Several circuit analysis modes are offered in the circuit simulators [7, 8, 22, 23, 24]. They help the designers to verify their circuit from many different viewpoints.

1.1.1.1 Direct Current Analysis

In direct current (DC) analysis, the operating points are solutions that do not change with time [1]. The first step of DC analysis is to generate all independent sources to make sure that they are constant. Then, the capacitors and inductors are removed away. When the circuit achieves the steady state, the capacitors are acting as open circuits and inductors are acting as short circuits. Therefore, we have such algorithm for computing an operating point [22].
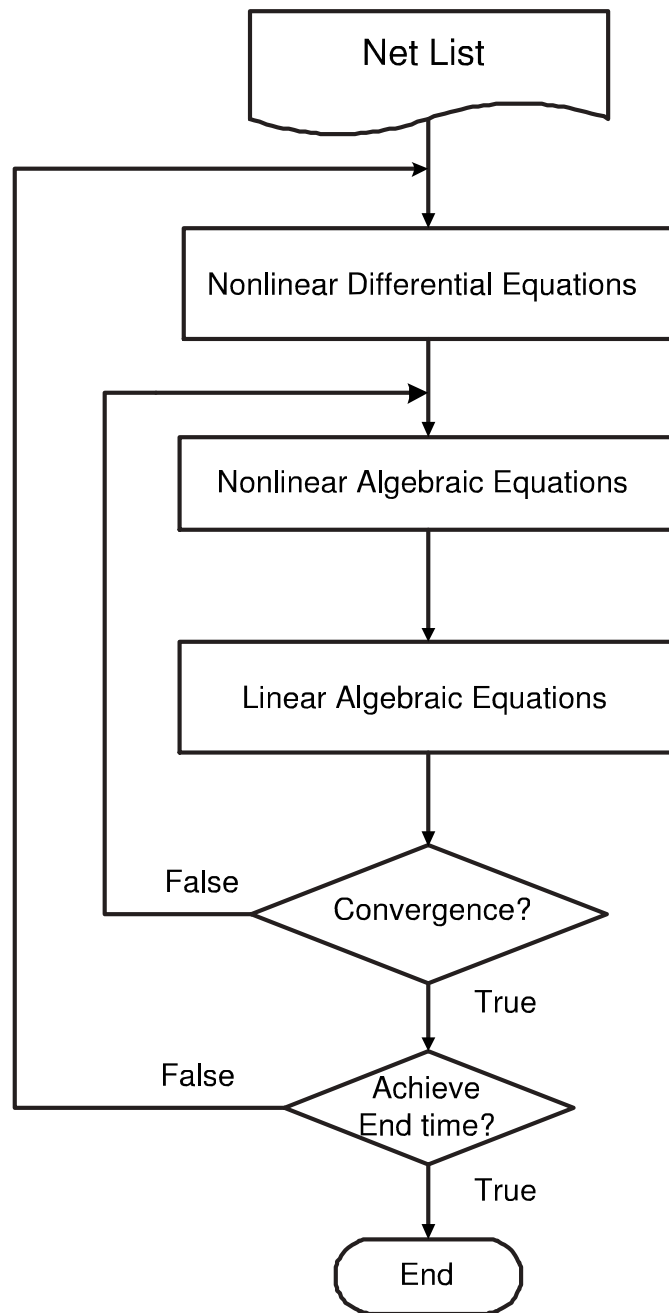
FIGURE 1.1: The flowchart of circuit simulation [9].

Step 1: Configure all independent sources to be constant valued.

Step 2: Replace all capacitors with open circuits.

Step 3: Replace all inductors with short circuits.

Step 4: Construct the circuit nodal equations.

Step 5: Solve the equations.

The system of equations constructed in step 4 is nonlinear and algebraic. These large nonlinear systems of algebraic equations are not easy to be solved. The only way is to use iterative methods such as NR method and the continuation methods. However, as mentioned before, these methods cannot make sure that we will get the solution successful. Convergence is still a big challenge for circuit simulators, especially for some large-scale and complex circuits. Before solving the nonlinear equations, we must note that,

1. Sometimes, there are more than one DC solutions.

2. The circuit simulator may get some unstable DC solutions.

The DC analysis is the most fundamental and important task for other analyses. It determines the linearized, small signal models of the nonlinear devices for the small signal AC analysis. It is also the prior to the transient analysis, since the DC solution is used as the initial condition of transient analysis. Therefore, finding the DC solution shows great importance.

1.1.1.2 AC Small-Signal Analysis

As a function of frequency (transfer function), the AC output variables are computed by AC small-signal analysis, over a user-specified range of frequencies [9, 22]. It is useful for the design of analog circuits which operate in small-signal modes. The perturbational response of the circuit is obtained by using linearized models
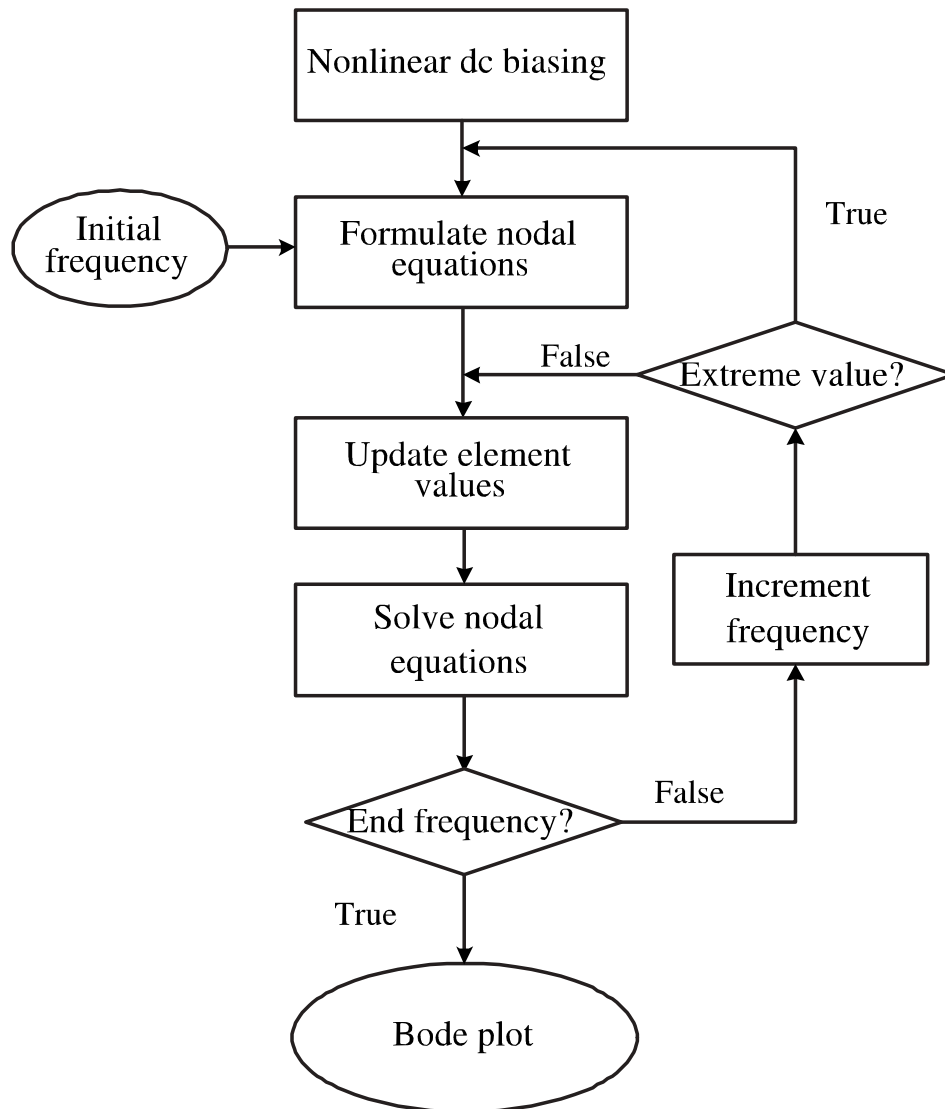
FIGURE 1.2: AC small signal analysis flowchart [9, 22].

for the nonlinear elements. The parameters for these linearized models are determined by the DC operating point analysis. The flowchart of AC small-signal analysis is shown in Fig. 1.2.

1.1.1.3   Transient Analysis

As functions of time over a user-specified time interval, the transient output variables, voltages and currents are found by the transient analysis [9, 47]. The large signal time domain behavior of circuits containing nonlinear elements is determined over a specified time interval $(0, t_f)$. The initial solution is either specified by user or determined by the DC analysis.

   By dividing the time interval $(0, t_f)$ into discrete time points $(0, t_1, t_2, \cdots, t_n, \cdots, t_f)$, the transient solution is determined computationally. The differential model equations are transformed into equivalent algebraic equations by applying a numerical integration algorithm at each time point. Then the NR method is used to solve these equations.

1.1.2   Nonlinear DC Circuit Equations

Firstly, the computer-aided engineering (CAE) tools will convert the graphical representation into a netlist description [13, 20, 21]. The model parameters and the connectivity information are introduced in the netlist file of the target circuit. From the information, the circuit simulator forms a set of ordinary differential equations (ODEs), which describe the target circuit. The Kirchhoff's Voltage Law, Kirchhoff's Current Law and the current-voltage relationships are used to load the circuit structure into the simulator. For DC analysis, the energy storage devices are removed from the target circuit. Then, the commercial circuit simulators commonly use the modified nodal analysis (MNA) [20] method to formulate the DC circuit equations.
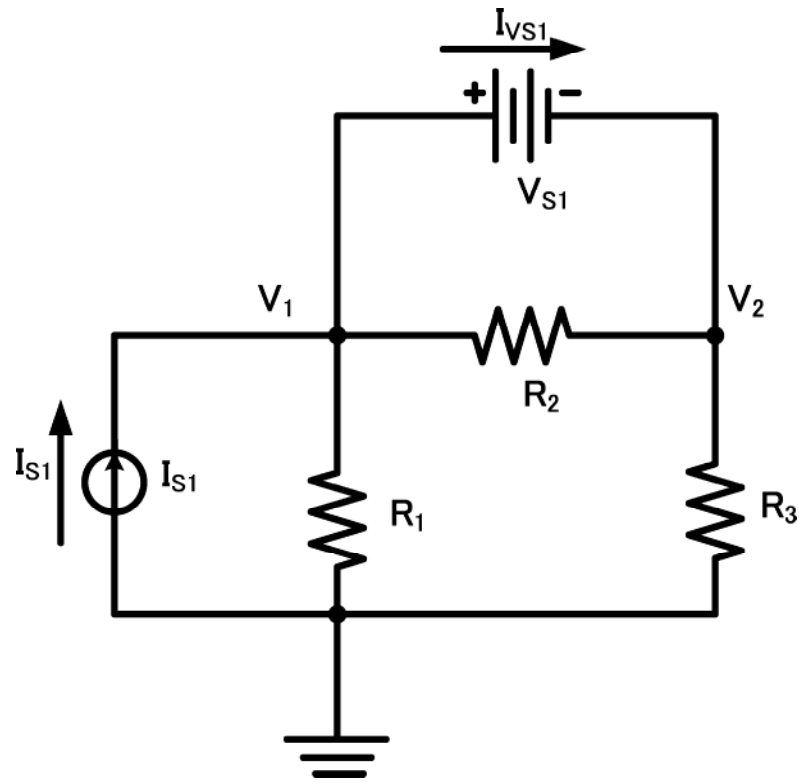
FIGURE 1.3: A simple example to show the modified nodal analysis.

1.1.2.1 Modified Nodal Analysis

To formulate the nonlinear DC circuit equations for the large-scale circuits, an automatic and systematic approach method is required. The modified nodal analysis (MNA) [20] is widely used in circuit simulator. Although, MNA might result in larger systems of equations, it is easier to implement on the circuit simulator algorithmically. This property is a substantial advantage for automated solution [20]. Here, a simple linear resistive circuit shown in Fig. 1.3 is used as an example to describe MNA method.

Firstly, apply Kirchoff's Current Law (KCL) to each node (take currents out of the node to be positive). Then, we obtain:

$$\frac{V_1}{R_1} + \frac{V_1 - V_2}{R_2} - I_{s1} + I_{Vs1} = 0 \cdots (node1) \tag{1.1}$$

$$\frac{V_2 - V_1}{R_2} + \frac{V_2}{R_3} - I_{Vs1} = 0 \cdots (node2) \tag{1.2}$$

$$V_1 - V_2 = V_{s1} \cdots (V_{s1}) \tag{1.3}$$

Secondly, move all known variables to the right hand side (RHS), and form:

$$\begin{bmatrix} \frac{1}{R_1} + \frac{1}{R_2} & -\frac{1}{R_2} & 1 \\ -\frac{1}{R_2} & \frac{1}{R_2} + \frac{1}{R_3} & -1 \\ 1 & -1 & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ I_{Vs1} \end{bmatrix} = \begin{bmatrix} I_{s1} \\ 0 \\ V_{s1} \end{bmatrix} \tag{1.4}$$

Obviously, such linear DC circuit equations are easy to be solved. If the target circuit includes nonlinear devices, like MOS transistor, the nonlinear DC circuit equations are difficult to be solved.

The general form of DC circuit equations is defined as:

$$\mathbf{F}(\mathbf{x}) = \mathbf{0}, \tag{1.5}$$

where $\mathbf{x} = (\mathbf{v}, \mathbf{i})^T \in \mathbb{R}^n$, $\mathbf{F} : \mathbb{R}^n \to \mathbb{R}^n$, and $n = N + M$. The variable vector $\mathbf{v} \in \mathbb{R}^N$ denotes the node voltages to the datum node and the variable vector $\mathbf{i} \in \mathbb{R}^M$ denotes the branch currents of the independent voltages sources.

1.1.2.2 Mathematical Modeling

The semiconductor circuit is made up of basic devices, including inductors, capacitors, diodes, resistors, bipolar transistors, MOS transistors, and so on. The actual behavior of these devices are described by the mathematical modeling based on the physical experimental experiences [14, 15, 16, 17, 18, 19].

The linear devices like resistors, inductors and capacitors are easy to be modeled, since their values are linear with their physical size. For the nonlinear devices, including bipolar transistors, MOS transistors and diodes, there are many effects need to be considered into the models. Therefore, there are many researches for improving the device models of the nonlinear devices to describe their action more accurate.

Here, a transistor model is shown as an example. The appropriate equation to simultaneously represent the transistor in the linear and saturation regions is obtained from an observation of the measured characteristics[19]:

$$
I_D = \begin{cases}
\frac{W}{L}\mu_n C'_{ox}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}(1+\delta)V^2{}_{DS}\right] & : \quad V_{DS} \leq V_{DS,sat} \\
\frac{W}{L}\mu C'_{ox}\frac{(V_{GS}-V_T)^2}{2(1+\delta)} & : \quad V_{DS} > V_{DS,sat}
\end{cases}
\tag{1.6}
$$

It is obviously that applying this kind of nonlinear models shown in Eq. (1.6), the matrix formed by MNA is complex and the $\mathbf{F}(\mathbf{x})$ is difficult to be solved.

1.1.3 Numerical Analysis

After the circuit nodal equations are formulated, the simulator solves these equations to find the solution. The Gaussian elimination is used to solve the circuit,

which is composed of linear elements. For the nonlinear dc circuit, the SPICE-like simulators firstly apply Newton-Raphson (NR) algorithm. By applying the NR method, the simulators try to find the solution of a sequence of linear equations rather than the solution of a nonlinear equation.

1.1.3.1   Newton-Raphson Method

Suppose Eq. (1.5) is the unknown nonlinear circuit equation, where the initial guess is $\mathbf{x}^0$ and solving the NR iteration Eq. (1.7) [13] repeatedly.

$$J(\mathbf{x}^m)(\mathbf{x}^{m+1} - \mathbf{x}^m) = -\mathbf{F}(\mathbf{x}^m), \tag{1.7}$$

$$J(\mathbf{x}^m) = \left.\frac{\partial \mathbf{F}(\mathbf{x})}{\partial \mathbf{x}}\right|_{\mathbf{x}=\mathbf{x}^m}, \tag{1.8}$$

where $\mathbf{x}^i$ is the value of $\mathbf{x}$ at the ith iteration, and $J : \mathbb{R}^n \to \mathbb{R}^n$ is the Jacobian matrix of $\mathbf{F}(\mathbf{x})$. The process of the NR method is started with an initial guess $\mathbf{x}^0$. According to the Eq. (1.7), $\mathbf{x}^1$ is obtained. Until the convergence conditions are achieved, we will get the solution $\mathbf{x}^{m+1}$ which is the value of $\mathbf{x}$ on the $(m+1)^{th}$ iteration [2]. The example of this process is shown in Fig. 1.4.

There are three conditions which can guaranty the convergence of NR method. The first one is that the $\mathbf{F}$ is continuously differentiable. The second one is that the the solution is isolated. The third one is that the $\mathbf{x}^0$ is sufficiently close to $\mathbf{x}^*$ [2, 23]. It is probably impossible to guarantee the third condition in circuit simulation. As shown in Figs. 1.5 and 1.6, the simple diode circuit is used as an example. The NR method is failed to converge due to the overflow problem and cycle phenomenon. The convergence is the biggest problem for the designers by using the NR method.
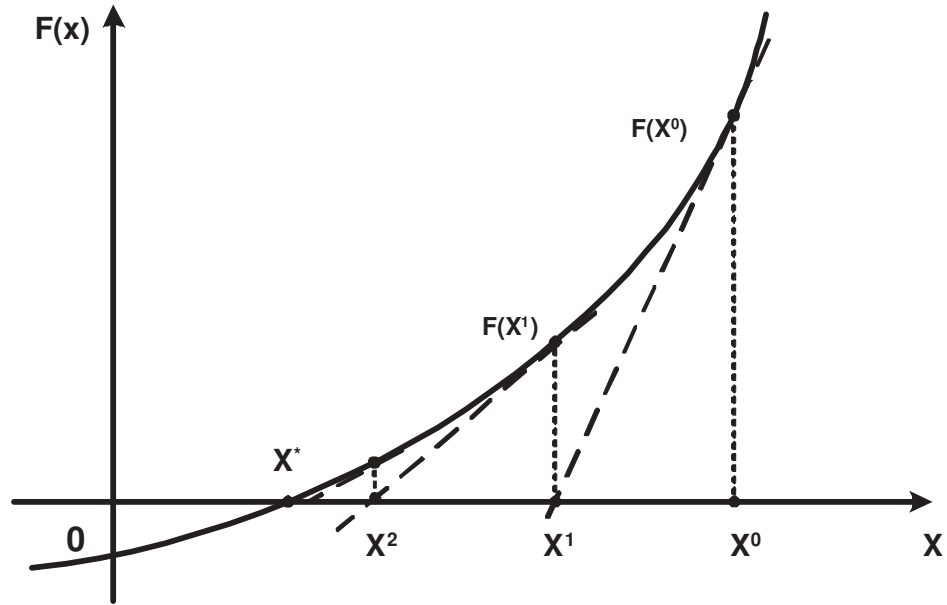
FIGURE 1.4: NR algorithm used to find the solution $\mathbf{x}^*$ of $\mathbf{F}(\mathbf{x}^*) = 0$.
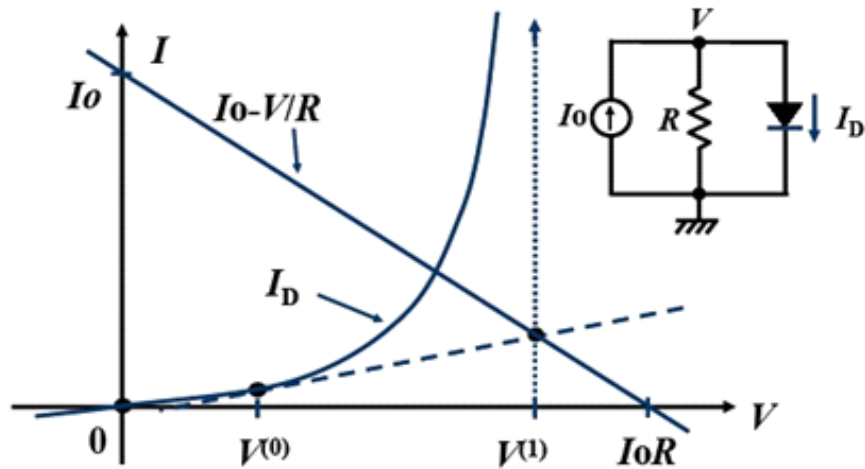
FIGURE 1.5: A graphical illustration of overflow problem of the NR method [7].

The convergence speed of the NR method is good. It is quadratic convergence. Which means the method squares the error on each iteration to reduce it, if the solution is close. So that the NR method can find the solution accurately with only a few more iterations once it is close to the solution [2, 23].
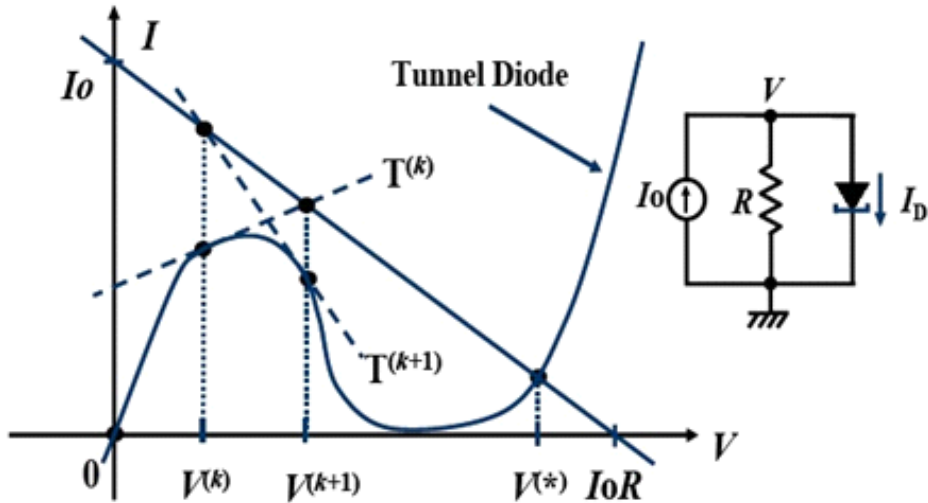
FIGURE 1.6: A graphical illustration of cycle phenomenon of the NR method [7].

1.1.3.2 Continuation Methods

If the NR method is unsuccessful, the SPICE-like simulators attempt to use the continuation methods to find the solution (in SPICE2, the option itl6 should be nonzero) [9]. Compared with NR method, the continuation methods are more robust but slower. All continuation methods start by modifying the circuit. After the modification, it is easy to compute or already known the solution. There should be a parameter which controls the amount of modification. Once the modified circuit achieves the solution, the control parameter is slowly returned to the original value. Thus, the modified circuit returns to its original form [1]. With the change of this control parameter, the solution in each step is computed by using the starting point getting from previous step. This starting point is the solution of previous step since the step size is small enough and the solution changed continuously.

The modification transfers Eq. (1.5) into Eq. (1.9)

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$$\mathbf{G}(\mathbf{x}(\lambda), \lambda) = 0, \tag{1.9}$$

where λ is the control parameter of the modified circuit, and we have to make sure that,

1. When $\lambda = 0$, we should already known the solution or the solution is easy to compute.

2. When $\lambda = 1$, the modified circuit should change to the original circuit which means that $\mathbf{G}(\mathbf{x}(1), 1) = \mathbf{F}(\mathbf{x})$.

3. The $\mathbf{x}(\lambda)$ is a continuous function of λ for $0 \leq \lambda \leq 1$.

Thus, between the initial solution and the final solution, a continuous curve is obtained. The final solution is regarded as the real solution of the original circuit. Source stepping, Gmin stepping, and pseudo-transient are three commonly used continuation methods in the commercial simulators. Source stepping and Gmin stepping are implemented in SPICE2 and SPICE3 seperatly [9], while pseudo-transient is provided by ASTAP [3]. Spectre and HSPICE provide not only all these methods but also an additional option named as damped pseudo-transient or dptran. However, this dptran method are confidentiality and not published anywhere.

Source Stepping and Gmin Stepping

In the source stepping method, firstly the source voltages and currents are set to be zero. Then, the value of them are ramped slowly to their final values. In every time the values of these sources are changed, the solution of the system is

recomputed one more time. The source stepping method may fail to converge due to the discontinuity problems, which will be described later. There are other methods, such as Gmin stepping and pseudo-transient analysis (PTA).

In Gmin stepping method, firstly a solution can be obtained easily, since all nonlinear devices are swamped out by adding small resistors in parallel. Then, with the increasing of these resistors, the simulator will compute the solution again and again. Once the resistors have no effect to the circuit, the DC solution is computed. There are some different Gmin stepping methods, in which the conductances are connected across pn-junctions, or similar. These Gmin stepping methods are easy to be implemented in the circuit simulator. Similar with other continuation methods, if Gmin stepping fails to converge, one can use a smaller step size. If it is really difficult to converge, the pseudo-transient analysis is the last chance.

There are three discontinuity types which will cause the non-convergence problem. The first one is the simple discontinuity. The second one is fold. The third one is called bifurcation [1]. As shown in Fig. 1.7, the simple discontinuities have a jump point, which are difficult for the NR method.

The folds phenomenon occur when there are multiple solutions at one time point, which are shown in Fig. 1.8. The bifurcations occur when there are some branches after a certain point, which are shown in Fig. 1.9.

Homotopy Methods

Another important method is homotopy method which has been researched for many years [25, 26, 27, 28, 29, 30, 31, 33, 36]. It is a method from theoretical viewpoint. Compared with all the continuation methods mentioned above, which are not necessary to guarantee global convergence, the theoretical standpoint methods are mainly focus on resolving the non-convergent problems fundamentally and
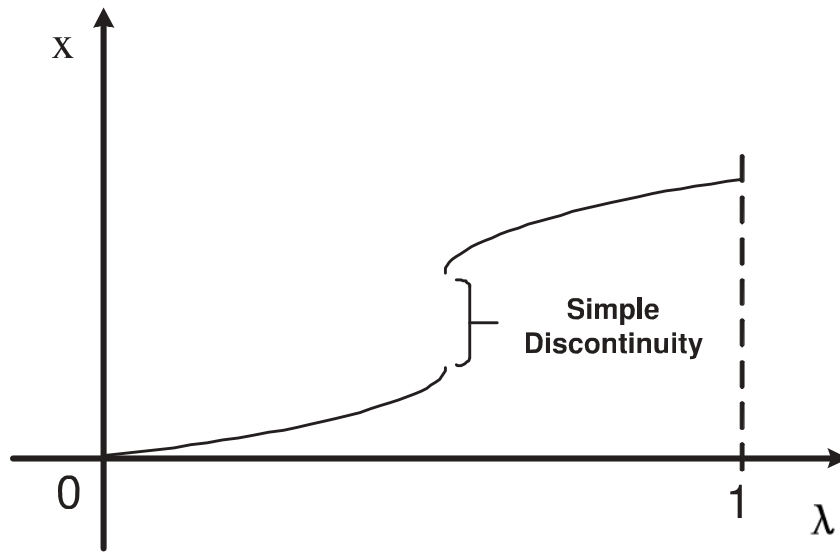
FIGURE 1.7: Simple discontinuity in homotopy due to discontinuous models causes Gmin and source stepping to fail.
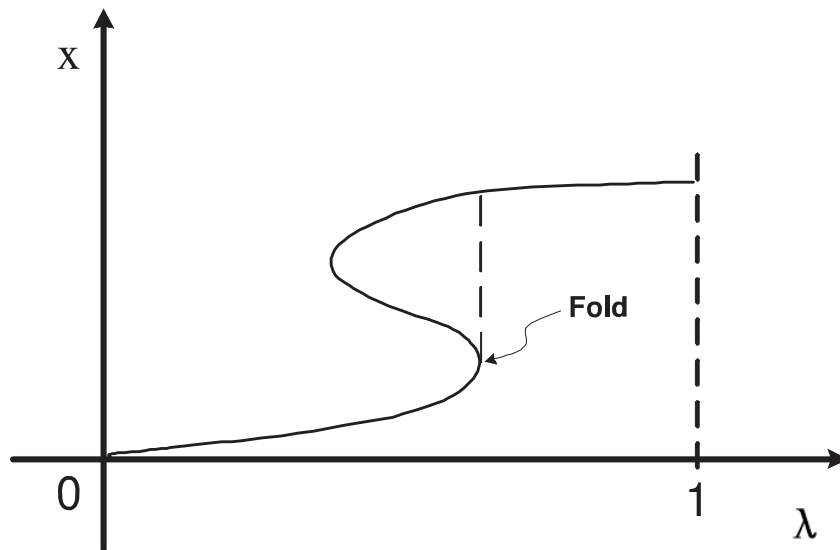
FIGURE 1.8: Fold in homotopy causes Gmin and source stepping to fail.

strictly guarantee globally convergent [25, 26, 27, 28, 29, 30, 31]. Basic concept of homotopy methods is continuous deformation of functions. In 1953, Davidenko raised predictor-corrector continuation method from mathematic viewpoint. After that, piecewise linear continuation method from the circuit simulation viewpoint,
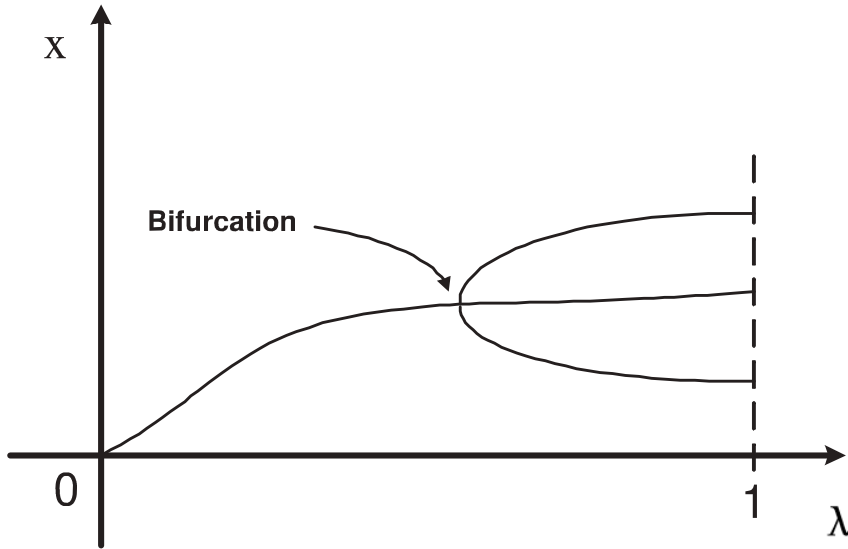
FIGURE 1.9: Bifurcation in homotopy caused by symmetry causes Gmin and source stepping to fail.

in which globally convergent is guaranteed, and simplistical algorithms are raised. Recently studies mainly focus on efficiency improvement. The homotopy method is a semi-analytical algorithm to solve nonlinear ordinary differential equations and partial differential equations. The homotopy technique employs the concept of the homotopy from topology to generate a convergent series solution for nonlinear systems. The basic concept of homotopy is continuous deformation of functions. In the homotopy methods, the fixed-point (FP) and the Newton homotopy method are well known [26, 30, 31]. These methods are proved to be globally convergent for modified nodal (MN) equation. In particular, the FP homotopy method has an excellent property that a random choice of initial point gives a bifurcation free homotopy path with probability-one [26, 28, 31, 36]. Nowadays, the practical standpoint methods are mainly implemented in commercial circuit simulators. The homotopy method is dependent on device models so that with rapid semiconductor technology progress, it is not easy to implement in commercial simulator [37].

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Pseudo-Transient Analysis

Recently, the pseudo-transient analysis (PTA) techniques are regarded as the most practical methods to solve the DC operating point of the nonlinear DC circuit. In PTA method, firstly the capacitor is added in parallel for all nonlinear devices as shown in Fig. 1.10. The original DC circuit equations are rewritten as Eq. (1.10)

$$\mathbf{F}(\mathbf{x}(t), t) + \mathbf{D}\dot{\mathbf{x}}(t) = \mathbf{0}, \tag{1.10}$$

where $\mathbf{D}$ is the incidence matrix to represent the connection information for all pseudo-elements, and $\dot{\mathbf{x}}(t)$ represents the derivative of x with respect to t.

These pseudo-elements are with a zero initial condition. Then, we have the time or called pseudo-time for these capacitors. A transient analysis will be done and the circuit continuously deformed to its original. The pseudo-time is approaching to infinity. The capacitors should cause the solution waveform to be a continuous function of time. When the transient analysis settled done, the pseudo-capacitors are disappeared and the final solution is obtained, which is the DC solution. The PTA method works well when it does not convert the circuit into an oscillator [3, 4, 5].

In [43], the compound element pseudo-transient analysis (CEPTA) method is proposed. This method uses the compound pseudo-elements, shown in Fig. 1.11, to avoid the oscillation problems. However, when the time-varying resistors and conductances are used in the pseudo-elements, the continuation of the solution waveform can not be guaranteed. Note that, both source stepping, Gmin stepping, and CEPTA cannot avoid the three types of discontinuous shown in before.
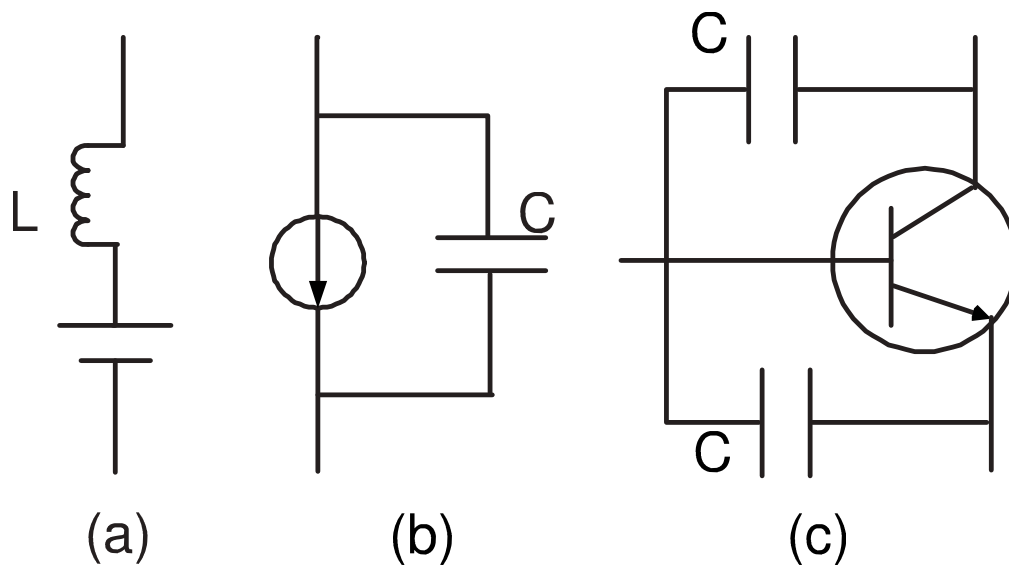
FIGURE 1.10: Pseudo-elements in constant pure PTA method [43].
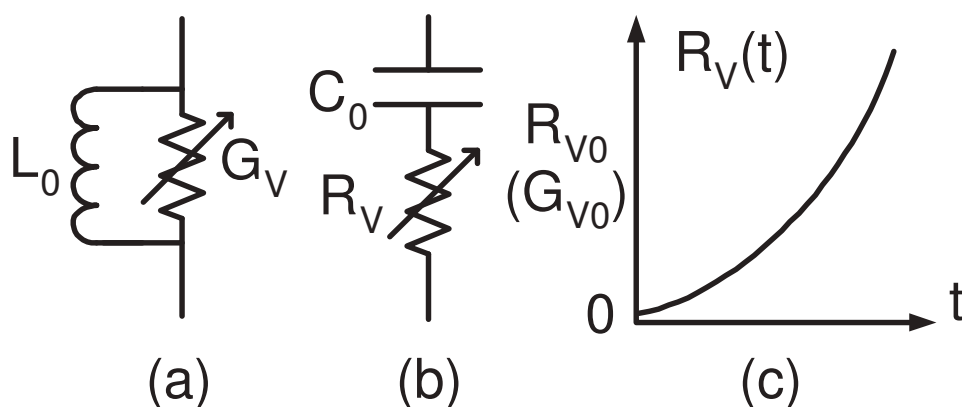
FIGURE 1.11: Compound pseudo-elements for CEPTA method [43].

There are some improvement methods proposed for CEPTA method in [44, 45], including the implementation algorithms, the embedding algorithms, and the ramping algorithms. There are 4 new SPICE3 implementation algorithms, which are distinguished by applying backward Euler method to different formulas. The algorithms also realize branches GVL and RVC by companion models without increasing additional nodes in the circuit. The obtained companion model is as
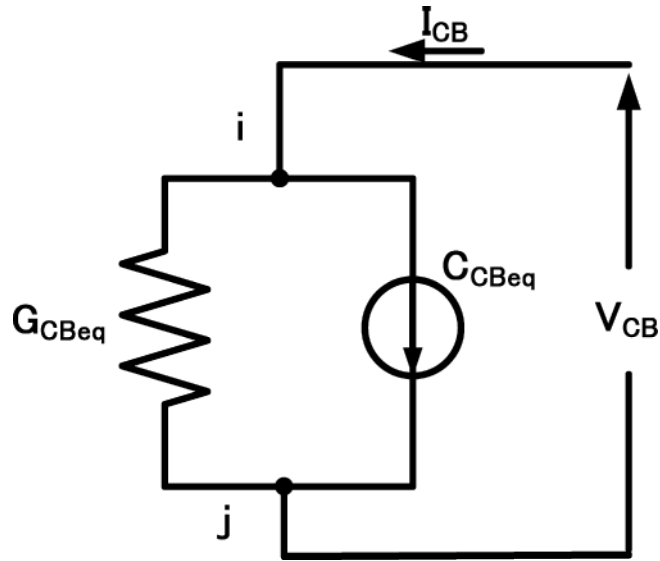
FIGURE 1.12: Companion model for RVC branch obtained from implementation algorithm [44].

shown in Fig.1.12 [44]. There is no additional node k and only insert into the circuit between nodes i and j. Thus, they do not enlarge the structure of Jacobian matrix, and ensure the simulation efficiency. Besides, these algorithms do not have some limitations compared with conventional one by applying numerical integration method to differential parts in a different way. Therefore, these improvement methods have the ability to improve the convergence and efficiency.

The embedding and ramping algorithms are proposed to improve the convergence and efficiency for all PTA techniques. However, they still cannot help the CEPTA method to solve the discontinuous problems. The ramping algorithms can vanish the oscillation problem caused by inductor and capacitor together, since it does not insert any inductor. However, we still have the risk on that the capacitors could convert the circuit into an oscillator.

The embedding algorithm provides extra insert positions for pseudo capacitors, which are applied to MOS and BJT transistors. In CEPTA, the insertion position
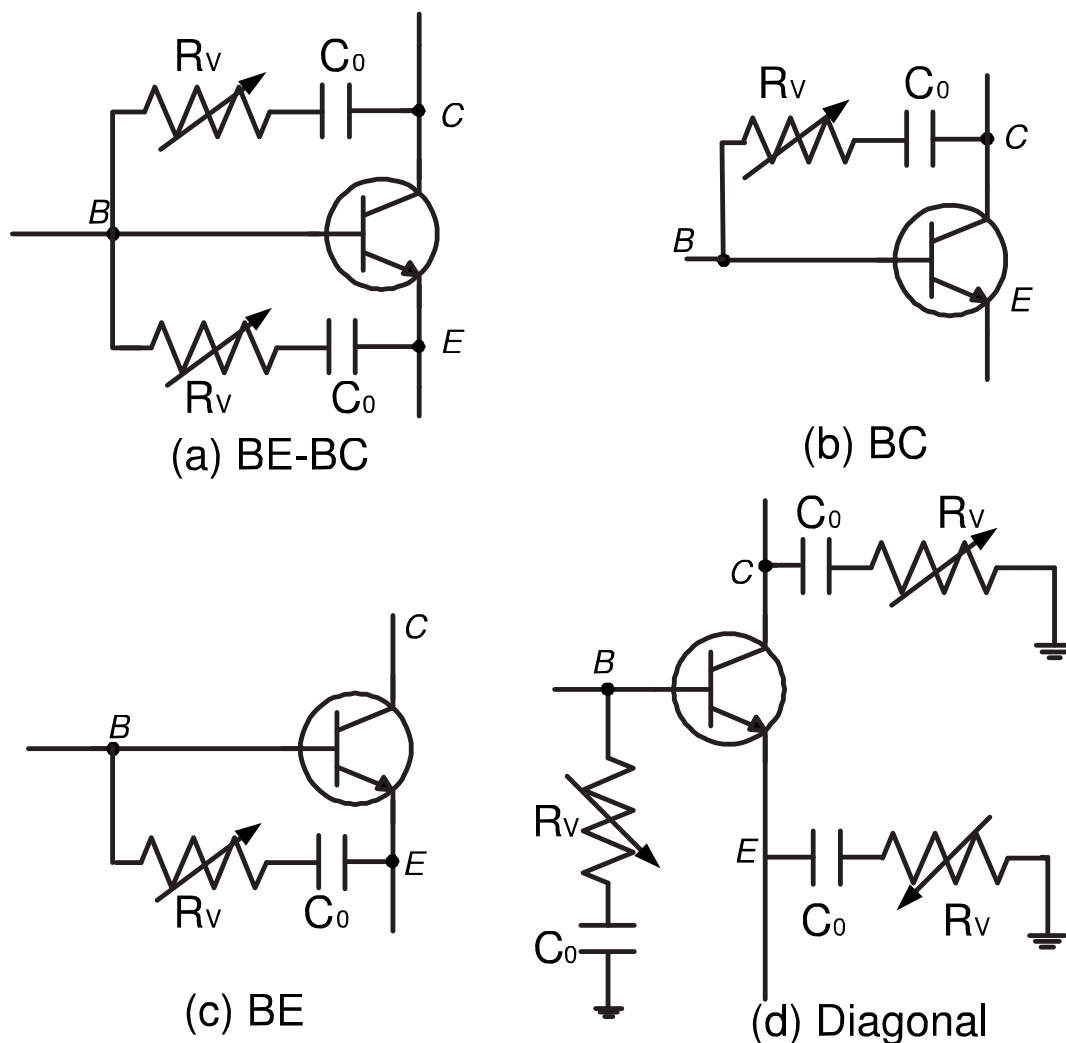
FIGURE 1.13: Embedding positions of pseudo elements [44].

of pseudo element is capable to influence the simulation results. In [43], for BJT transistors, the compound pseudo-capacitors are inserted between Base-Collector and Base-Emitter, which is shown in Fig.1.13.(a). In the homotopy method, the BE-BC position is chosen for the bipolar transistors [47]. In [44], three embedding positions are extended to improve the convergence and efficiency. However, the embedding algorithms cannot eliminate the oscillation problem.

1.2   Challenges for PTA

As mentioned before, the NR method and the continuation methods may fail to converge in some conditions. The pure PTA (pseudo elements are pure capacitors and inductors) methods may have oscillation problem, and CEPTA method probably has discontinuous problems. Moreover, the numerical examples of previous studies are mainly for small-scale circuits or single type of circuits. Therefore, a new way to solve all these problems is needed. The pure PTA technique is the best choice of my research since it has no discontinuous problems. This method works well if the pseudo-element does not convert the circuit into an oscillator. Therefore, a new method to solve the oscillation problem is needed.

The new method should solve three challenges:

Ch1. Convergence: solve both oscillation and discontinuity problems of PTA technique, and get the DC solution of all test circuits in INOUE Lab.;

Ch2. Efficiency: reduce the CPU time for DC analysis as much as possible;

Ch3. Robustness: the change of parameters' value should not largely infect the result of DC analysis.

1.3   Innovation

All the research studies previously published of PTA techniques are from the pseudo element viewpoint [1]. In this work, to address these issues from the different viewpoint (numerical integration algorithm viewpoint), a PTA method using

---

[1]Commercially available circuit simulator's PTA algorithms are not published and details are not known.

numerical integration algorithms with artificial damping is proposed. The proposed PTA method artificially enlarges the damping effect in the numerical integration algorithms to weaken the oscillation. Moreover, a switching algorithm in the SPICE3 implementation and a new time-step size method are proposed for this new PTA method to improve the simulation speed (CPU time) and make the PTA method much more robust. The switching algorithm changes among the numerical integration methods automatically according to the simulation status, which efficiently improve the convergence performance of the proposed PTA method. The proposed time-step control method determines the time-step size according to the circuit status at each time-step during the pseudo-transient process. It adapts the time-step size automatically and intelligently without constant upper limit. With this method, heavier damping effect is obtained and it makes the proposed PTA method has a wider compatibility with control parameter values. The effectiveness of the proposed methods are illustrated by the verification of LSI analog circuits.

Chapter 2

Preliminaries

It is difficult to directly solve the ordinary differential equations. What we can do is to find an approximation to the real solution. In transient analysis, the simulation is divided into some small steps, some simplifying approximation is made in order to evaluate the time-domain derivative, so that we can solve the equation over the span of one time-step at a time [1]. Three commonly used numerical integration algorithms including backward Euler, forward Euler, and trapezoidal rule are reviewed in this chapter. The damping effect in the numerical methods is also introduced, which is also an importance technique used in the PTA method to eliminate the oscillation problems.

The conventional time-step control methods used in circuit simulator are reviewed including local truncation error (LTE) method, iteration count method, and switched evolution/relaxiation (SER) method. Moreover, the convergence of pseudo-transient continuation method is described in this chapter. During the simulation, at each step of the pseudo iteration, the simulator will do the convergence check. If the convergence conditions are satisfied, the procedure will get out from the pseudo-iteration loop and the DC solution is found. The convergence check analysis shows that in the PTA techniques, it is no need to consider the local truncation error. Thus, the time-step should be as large as possible as if the Newton-Raphson method can converge.

2.1 Numerical Integration Methods

The backward Euler (BE), forward Euler (FE), trapezoidal rule (TR), and the Gear's methods are the four commonly used numerical integration algorithms [2, 4, 6, 7, 9]. The first order methods include backward and forward Euler. The Gear's methods contain any order, and only the first six orders are implemented in SPICE [9].

Assume that the constant time-step size is used as $h = t_{n+1} - t_n$, and $x(t_n)$ is the exact solution at t_n. Then, the definition of the integration algorithms are written in the Eqs. (2.1,2.2,2.3) [1, 2, 47].

Forward Euler

$$\frac{d}{dt}x(t_n) \approx \frac{1}{h}[x(t_{n+1}) - x(t_n)]. \tag{2.1}$$

Backward Euler

$$\frac{d}{dt}x(t_{n+1}) \approx \frac{1}{h}[x(t_{n+1}) - x(t_n)]. \tag{2.2}$$

Trapezoidal Rule

$$\frac{d}{dt}x(t_{n+1}) \approx \frac{2}{h}[x(t_{n+1}) - x(t_n)] - \frac{d}{dt}x(t_n). \tag{2.3}$$

By using these numerical integration algorithms, an approximate solution, x_n at t_n, is obtained. In circuit simulation, the TR and Gear 2 methods are commonly used in the majority of cases. The Gear's methods with higher order are available, but they are not commonly used. At the beginning of simulation or on the break points, the BE method is often used. The TR, FE, and BE methods are all one-step methods. The calculation of x_{n+1} using only x_n, not $x_{n-1}, x_{n-2}, x_{n-3} \dots$. N^{th} order Gear's methods are N-step methods.

2.1.1 Numerical Damping Effect

The numerical damping effect occurs in some integration methods [1, 9]. In some conditions, this effect changes an unstable circuit to a stable one. Gear 2 and BE method have the heavy damping effect, while TR does not exist any numerical
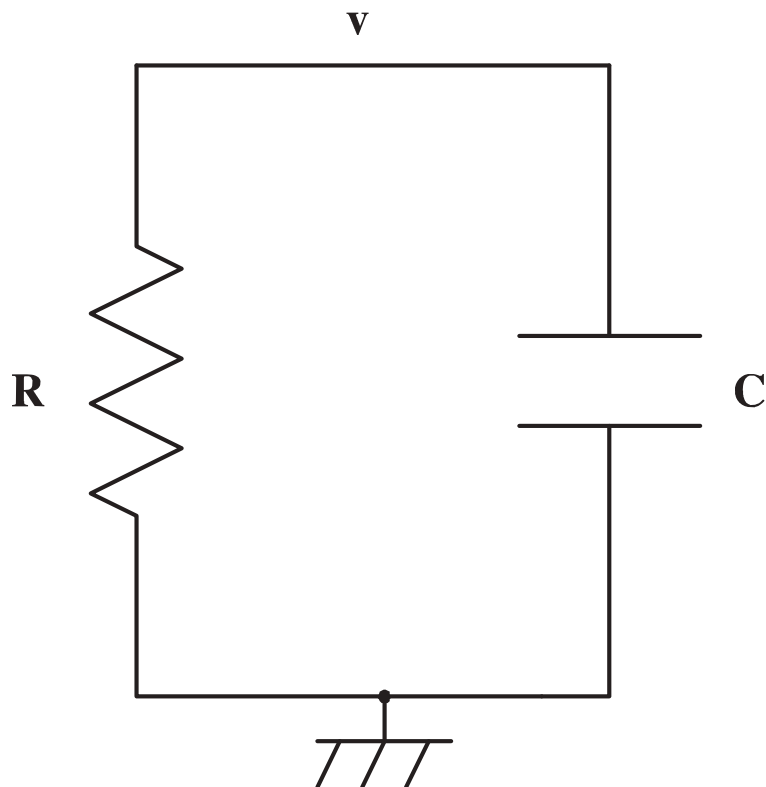
FIGURE 2.1: Linear RC circuit used to explore the numerical damping.

damping. The damping effect will be decreased when the smaller time-step size is used. Here, a simple RC circuit is used to explore the the numerical damping. The linear RC circuit is shown in Fig. 2.1. This linear circuit has a single real pole at $\lambda = -1/RC$. Writing KCL equations [1, 7, 9, 13]:

$$\frac{1}{R}v(t) + C\dot{v}(t) = 0, \tag{2.4}$$

$$\dot{v}(t) = -\frac{1}{RC}v(t), \tag{2.5}$$

$$\dot{v}(t) = \lambda v(t). \tag{2.6}$$

The Eq. (2.6) are mapped into a difference equation by using the integration

algorithms. Firstly, the BE method is applied with a uniform time-step size to Eq. (2.6) [1, 7, 9, 13],

$$\frac{1}{h}[v(t_{n+1}) - v(t_n)] = \lambda v(t_{n+1}), \tag{2.7}$$

$$\Rightarrow v(t_{n+1}) = \frac{v(t_n)}{1 - \lambda h}. \tag{2.8}$$

Let $\sigma = \lambda h$ be the pole frequency normalized by the time-step [9].

$$v(t_{n+1}) = \frac{v(t_n)}{1 - \sigma}. \tag{2.9}$$

Replace the unit delays with multiplications by z^{-1}, and convert the Eq. (2.9) into the frequency domain by z-transform.

$$v(t) \rightarrow V, \tag{2.10}$$

$$V = \frac{Vz^{-1}}{1 - \sigma}, \tag{2.11}$$

$$z = \frac{1}{1 - \sigma}. \tag{2.12}$$

This equation maps poles in the s-plane ($\sigma = h\lambda$) intopoles in the z-plane, which is shown in Fig. 2.2. If the poles are included in the left-half of the s-plane, this differential equation is stable. Also the equation is stable if its poles are contained within the unit disk of the z-plane [9].

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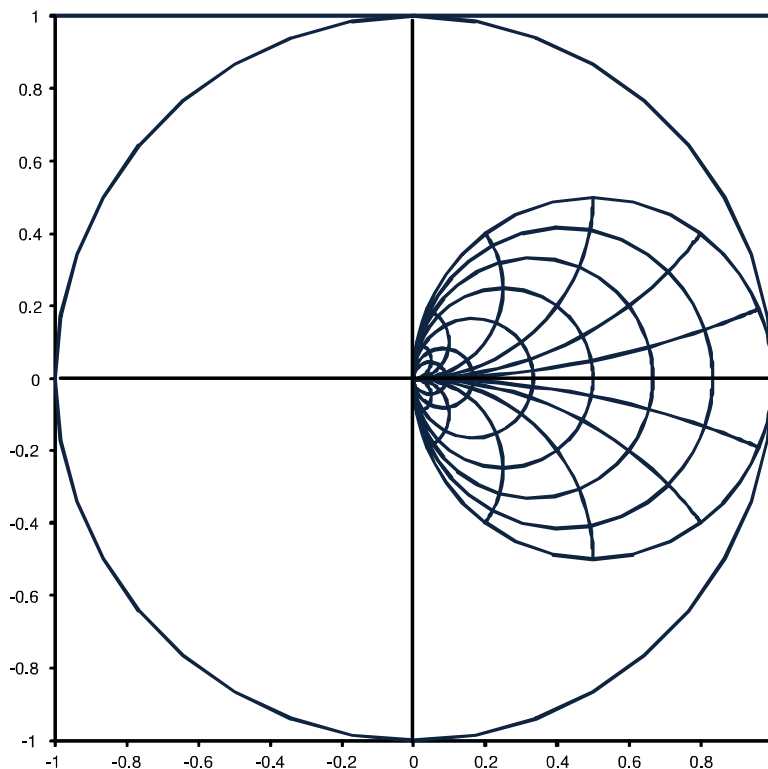
Figure 2.2: Left half of s-plane mapped into z-plane by backward Euler [9].

As shown in Fig. 2.2, the whole left-half of the s-plane maps into the unit circuit of the z-plane. Therefore, by using BE method, stable differential equation is mapped into a stable difference equation. Moreover, a portion of the right-half of the s-plane is mapped inside the unit circuit of the z-plane. It means that by using BE method, some unstable differential equations are mapped into stable difference equations. This phenomenon called over stable which will lead to the numerical damping effect.

2.2   Time-Step Control Methods

The SPICE3 provides 2 kinds of time-step control methods [1, 7, 9, 38]. The first one is the local truncation error (LTE) method, which uses estimates of the local truncation error to obtain the time-step size. The second one is the iteration count method, which uses the number of iterations required for convergence at a step to decide the value of next time-step size. Moreover, the Switched evolution/relaxiation (SER) method [32, 34, 35, 46, 50] is reviewed in this section.

2.2.1   LTE Time-Step Control Method

During transient analysis, numerical integration methods are used to determine the solution x_{n+1} at time point t_{n+1} given the previously computed solutions$(x_n, x_{n-1} \ldots)$. Since there exists the approximation of the algorithm, there will be some errors between the numerical results and the exact results as shown in Fig. 2.3, which is called the local truncation error [38].

In SPICE-like simulators, the LTE is used for time-step control during transient analysis. The LTE is the function of time-step size in the following form [38]:

$$LTE = lte(h) \leq Tolerance. \tag{2.13}$$

The interval $[0, t_f]$ is replaced by the discrete time points $t_0, t_1, \ldots, t_n, t_{n+1}, \ldots, t_f$, where the time-step size is $h_n \equiv t_n - t_{n-1}$.

There are two kinds of LTE estimations. The first one uses of two steps. The local error of a numerical method of order p is given by Eq. (2.14) [1, 7, 9]
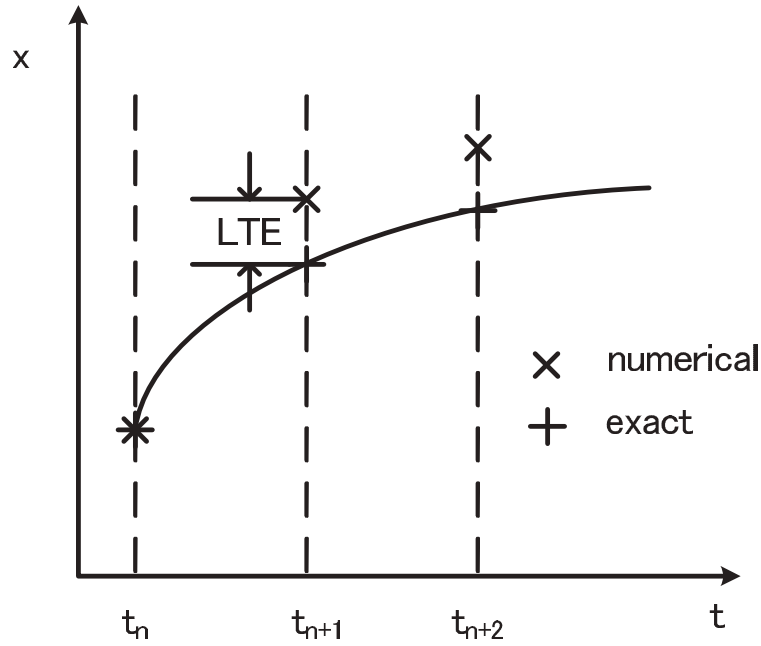
FIGURE 2.3: LTE during transient analysis [38].

$$\mathbf{x}(t_n + h) - \mathbf{x}_{n+1} = h^{p+1}\psi(t_n, \mathbf{x}_n) + O(h^{p+2}), \tag{2.14}$$

where ψ is the principal error function of the numerical method. After that, two steps of $h/2$ are used. The local error is [1, 7, 9]:

$$\mathbf{x}(t_n + h) - \tilde{\mathbf{x}}_{n+1} = 2(h/2)^{p+1}\psi(t_n, \mathbf{x}_n) + O(h^{p+2}), \tag{2.15}$$

where $\tilde{\mathbf{x}}_{n+1}$ is the solution after two steps of $h/2$. We can obtain an estimate for the LTE by subtracting Eq. (2.14) from Eq. (2.15),

$$LTE^{est} = \left(\frac{2^p}{2^p - 1} \right) |\tilde{\mathbf{x}}_{n+1} - \mathbf{x}_{n+1}|. \tag{2.16}$$

Suppose LTE^{tol} is the maximum allowed LTE. If $LTE^{est} < LTE^{tol}$, the current step is accepted, and the next step is allowed to increase. If $LTE^{est} > LTE^{tol}$, the current step is not allowed, the new step is computed such that it would result in an new LTE^{est} equal to LTE^{tol}.

Another LTE estimation uses of methods of different orders. Specifically, one method is pth-order accurate, and the other is $(p + 1)$st-order accurate. Assume that $\mathbf{x}_n = \mathbf{x}(t_n)$. Then, we get [1, 7, 9]:

$$
\begin{aligned}
LTE^p &= \mathbf{x}(t_{n+1}) - \mathbf{x}_{n+1}, &\tag{2.17}\\
LTE^{p+1} &= \mathbf{x}(t_{n+1}) - \tilde{\mathbf{x}}_{n+1}, &\tag{2.18}
\end{aligned}
$$

where the superscript on LTE indicates the order of the method, and $\mathbf{x}(t_{n+1}), \tilde{\mathbf{x}}_{n+1}$ denote the numerical solutions corresponding to the two methods. Subtracting Eq. (2.18) from Eq. (2.17),

$$LTE^p - LTE^{p+1} = \tilde{\mathbf{x}}_{n+1} - \mathbf{x}_{n+1}. \tag{2.19}$$

Since LTE^{p+1} is for a higher-order method compared with LTE^p, we can ignore LTE^{p+1}. Thus, $LTE^{est} = \tilde{\mathbf{x}}_{n+1} - \mathbf{x}_{n+1}$.

2.2.2 Iteration Count Method

This method counts the number of NR iterations, and uses this number to choose the size of next time-step [1, 7, 9]. Here, the LTE time-setp control method is not used for PTA techniques. Therefore, this section mainly focus on the iteration-count time-step control method.

The iteration-count method [1, 7, 9] is controlled by two options: IMAX and IMIN. If the number of iterations per timepoint exceeds the IMAX value, it will roll back to the previous step and do it again with a smaller timestep size. If the number of iterations per timepoint is between the IMIN and the IMAX, it will no change for the timestep size. If the last timepoint solution took fewer than the IMIN iteration, the timestep size is increased.

In SPICE3f5, the t_{max} (maximum time-step size) is defined as follow:

$$t_{max} = \frac{t_{stop} - t_{start}}{50}.$$ (2.20)

2.2.3 Switched Evolution/Relaxiation

In [50], the numerical methods for solving problems of steady compressible flow are useful to distinguish between two phases of the circuit simulation. In the first phase (searching phase), the numerical solution follows a path to the steady state with reasonable time-accuracy. In the second phase (converging phase), the numerical solution feels the attraction of the steady state and converges to the final solution rapidly. In each phase, the requirement of the time-step size is different. Therefore, the automatically and intelligently determined time-step size shows great importance. The SER method is time-accurate for small time-steps and turn into a relaxation method for large time-steps; the spatial discretization

is upwind biased [50]. It is a good way to adapt the time-step size automatically in order to optimise the time-step control parameters for different phases. There are several SER methods used in [32, 34, 35, 50] which increase the time-step in inverse proportion to the residual reduction [46]. Equation (2.21) is the simplest form of conventional SER method [46], where $\|\mathbf{F}(\mathbf{x})\|$ is the residual of Eq. (3.12a).

$$h_{n+1} = h_n \cdot \|\mathbf{F}(\mathbf{x}_{n-1})\|/\|\mathbf{F}(\mathbf{x}_n)\|. \qquad (2.21)$$

The change of the residual reduction shows the speed of convergence. This method is proposed to solve the problems in arithmetic and its schemes should be changed for different problems. However, the problems in circuit simulation are much more difficult since the waveform of residual reduction may not that idealized.

2.3 Convergence of Pseudo-Transient Analysis

The convergence check for PTA [46] mainly includes two parts. Firstly, all pseudo-elements should be vanished, which means that $\dot{\mathbf{x}}(t)$ in Eq. (1.10) is smaller than the error tolerance (in this research, the absolute error tolerance is 10^{-12}, and the relative error tolerance is 10^{-3}). Secondly, $\|\mathbf{F}(\mathbf{x})\| \rightarrow 0$, which means that the average residual reduction is smaller than the error tolerance. Finally, the DC solution is obtained. If there is no change in $\mathbf{F}(\mathbf{x})$, the accuracy of DC operating point is only affected by the error tolerance. Therefore, the consideration of local truncation error of PTA technique during the pseudo-transient analysis is not needed.

Chapter 3

A PTA Method Using Numerical Integration Algorithms with Artificial Damping for Solving Nonlinear DC Circuit Equations

3.1 Introduction

The task of finding DC operating points is the first job for the SPICE-like circuit simulators, since it is the fundamental for all other analysis models. As the circuit size grows, convergence is the most difficult task to achieve when the circuit simulation uses the Newton-Raphson (NR) iterative algorithm. The NR algorithm is commonly used in many circuit simulators for solving modified nodal (MN) equations since it converges fast with quadratic convergence. However, this algorithm may fail to converge unless the process is started with an initial guess which is sufficiently close to the solution [2].

There are many methods and improvements implemented in SPICE-like simulators such as Gmin stepping, source stepping and pseudo-transient [4, 7, 9]. However, the non-convergence problem still often occurs [8]. For SPICE-like simulators, the homotopy method should do a complex modification for different device models. Therefore, compared with other methods, homotopy is not practical even it is globally convergent [25, 26, 27, 40, 41, 42]. Therefore, a practical method which succeed in all of these cases is needed.

The pseudo-transient analysis (PTA) methods, which are considered as the most practical methods, have been researched for many years [3, 5, 43, 44]. The first PTA method appeared in the ASTAP [3] using constant capacitor and inductor to constitute pseudo elements. This PTA method inserts such elements into the target circuit to get a pseudo-circuit. After that do transient analysis for this pseudo-circuit with some specified initial values. The operating point is obtained when the pseudo-circuit reaches a steady state. Another PTA method reported by R. Wilton and L. Gold geisser uses time-varying pseudo-capacitor [5]. These two PTA methods are grouped into "pure PTA methods", where pure pseudo elements are used. However, after applying the pure pseudo capacitors and inductors to the

circuit, it is possible for the pseudo circuit to oscillate owing to the insertion of such pseudo elements [43]. Moreover, the efficiencies for these PTA techniques are not that satisfactory.

To overcome these problems in the pure PTA methods, the compound element pseudo-transient analysis (CEPTA) method is studied, which has the ability of avoiding oscillation problem and of improving efficiency [43, 44]. Compared with pure PTA, CEPTA uses the compound pseudo-elements instead of just the capacitors and inductors to avoid oscillation during the transient analysis. However, some experimental results demonstrate that the CEPTA method may fail to converge, especially for some large-scale and complex circuits. The convergence of the CEPTA method is considered and proved in [43, 44]. However, the convergence proof is based on the assumption that the waveform is continuous. The convergence performance of the CEPTA method is still not that satisfactory. In order to improve the convergence of the CEPTA method for variety of circuits, the embedding positions for compound pseudo-elements are extended. However, it cannot fundamentally solve the non-convergence problem, and such limitation still exists. Moreover, a large number of iterations, steps and CPU time are needed in the former researches to make the circuit converge. The efficiency still needs to be improved.

All the research studies previously published are from the pseudo element viewpoint. In this work, to address these issues from the different viewpoint (numerical integration algorithm viewpoint), a PTA method using numerical integration algorithms with artificial damping is proposed. The proposed method artificially enlarges the damping effect in the numerical integration algorithms to weaken the oscillation. The consistency and convergence of the proposed numerical integration algorithms are proved. Furthermore, an effective switching algorithm for the

PTA method is proposed to improve the convergence and efficiency. Numerical examples demonstrate that the proposed method has much better convergence and higher efficiency performance compared with previous studies of PTA method. Moreover, the proposed method can efficiently find the DC operating points of some large-scale circuits and complex circuits (the combination of various types of circuits, such as oscillation circuits, multiple solutions circuits and practical circuits).

3.2   Proposed Method

In this section, the new numerical integration algorithms are firstly presented, in which the damping effect is artificially enlarged. The mathematical description, consistency, convergence and stability of the proposed method are considered. Then, a PTA method using the presented numerical integration algorithms with artificial damping is proposed, which eliminates the oscillation problem effectively and improve the convergence performance. In order to further improve the convergence performance, a switching algorithm for the PTA method is also proposed. A complete PTA method includes two major parts: the pseudo-elements and the numerical integration algorithms. The proposed PTA method uses the pure and constant capacitors and inductors as pseudo elements.

3.2.1   Proposed Numerical Integration Algorithms

Consider a m-dimensional ordinary differential equation (ODE) system,

$$\dot{\mathbf{x}}(t) \quad = \quad \mathbf{f}(\mathbf{x}, t), \qquad\qquad 0 \le t \le t_f \qquad\qquad (3.1)$$

where $t \in \mathbb{R}$, $\mathbf{x} : \mathbb{R} \to \mathbb{R}^m$, $\dot{x}$ is the derivative of x, and $\mathbf{f} : \mathbb{R}^m \times \mathbb{R} \to \mathbb{R}^m$. In order to artificially enlarge the damping effect, the k step numerical integration algorithms shown in Eq. (3.2) is proposed to solve the ODE system in Eq. (3.1). For the proposed numerical integration algorithms, the interval $[0, t_f]$ is replaced by the discrete time points $t_0, t_1, \ldots, t_n, t_{n+1}, \ldots, t_f$, where the step size is $h_n \equiv t_n - t_{n-1}$.

$$\mathbf{x}_{n+1} \quad = \quad \mathbf{x}_{n+1-k} + \mathbf{f}(\mathbf{x}_{n+1}, t_{n+1}) \sum_{j=0}^{k-1}(h_{n+1-j}). \tag{3.2}$$

They are first order multi-step linear integration algorithms which are called k step damped differentiation formulas (DDF-k). Step $k = 1$ yields the backward Euler method. The damping effect will be artificially enlarged as k is increased. The step-number k is free to vary, depending on the requirement of damping effect. The start-up function procedure with DDF-k is that at t_0, a given initial condition $\mathbf{x}_0$ and DDF-1 are used to solve $\mathbf{x}_1$. Then, DDF-2 is used to compute $\mathbf{x}_2$, and so on. After k steps have been taken, DDF-k is used.

By applying the proposed numerical integration algorithms DDF-k to the differential part in Eq. (3.1), a set of nonlinear algebraic equations at each advanced discrete time point t_{n+1} is obtained, which is solved by Newton's iteration for $\mathbf{x}_{n+1}$. Since the proposed numerical integration algorithms are implicit, the following predictor algorithm is used to solve the prediction of the solution $\mathbf{x}_{n+1}$.

$$\mathbf{x}_{n+1}{}^{P} = (t_{n+1} - t_n)\frac{\mathbf{x}_n - \mathbf{x}_{n-1}}{t_n - t_{n-1}} + \mathbf{x}_n. \tag{3.3}$$

Note that in the predictor algorithm the backward value $\mathbf{x}_n$ at the previous time point t_n is effectively used to improve the prediction. Note also that higher order predictor algorithms are applicable. This is the reason that the proposed method can have a good convergence of Newton iteration method when the time-step size is artificial enlarged.

For the new numerical integration algorithms used in pseudo-transient analysis method, the consistency, stability and convergence should be analyzed [47]. In

order to prove the convergence of the proposed numerical integration algorithms, consider the following Theorem 3.1 [48]. Consistency and zero-stability are the two key ingredients required to ensure that a numerical method is convergent. Thus, consider the following notation of Lambert [47], the general form of numerical method:

$$\sum_{j=-1}^{k-1} \alpha_j \mathbf{x}_{n-j} = h\phi_{\mathbf{f}}(\mathbf{x}_{n+1}, \mathbf{x}_n, \cdots, \mathbf{x}_{n-k+1}, t_{n+1}; h), \tag{3.4}$$

where the step size h has been assumed fixed, $k \geq 1$ is the step-number for multistep method, and $\phi_{\mathbf{f}}(\cdot)$ is the function that depends on the system function $\mathbf{f}(\cdot)$. For our proposed algorithms, $\alpha_{-1} = 1, \alpha_{k-1} = -1$ and all other coefficients are 0.

Theorem 3.1. *A difference system is convergent if and only if it is both consistent and zero-stable.*

For the general numerical algorithm, the first characteristic polynomial is defined as shown in Eq. (3.5), in $z \in c$ [47]:

$$\rho(z) = \sum_{j=-1}^{k-1} \alpha_j z^{k-j-1}. \tag{3.5}$$

Theorem 3.2. *A numerical method is consistent if and only if, for any $t \in [t_0, t_f]$, the following two conditions hold:*

$$\rho(1) = 0, \tag{3.6}$$

$$\phi_{\mathbf{f}}(\mathbf{x}(t), \mathbf{x}(t), \cdots, \mathbf{x}(t), t; 0) = \rho'(1)\mathbf{f}(\mathbf{x}(t), t). \tag{3.7}$$

For the proposed integration algorithms, we get $\rho(z) = z^k - 1$ and $\rho'(z) = kz^{k-1}$, so that $\rho(1) = 0$ and $\rho'(1) = k$, and since h is constant,

$$
\begin{aligned}
h\phi_{\mathbf{f}}(\mathbf{x}_{n+1}, \mathbf{x}_{n+1-k}, t_n; h) &= \mathbf{f}(\mathbf{x}_{n+1}, t_{n+1}) \sum_{j=0}^{k-1} (h_{n+1-j}) \\
&= hk\mathbf{f}(\mathbf{x}_{n+1}, t_{n+1}),
\end{aligned} \tag{3.8}
$$

then, as $h \to 0$, $n \to \infty$, all the time-points approach t, and all the values $\mathbf{x}_{n+1}, \mathbf{x}_n, \mathbf{x}_{n-1}, \cdots, \mathbf{x}_{n-k+1}$ approach $\mathbf{x}_t$. Thus, it is obtained:

$$
\phi_{\mathbf{f}}(\mathbf{x}(t), \mathbf{x}(t), t; 0) = k\mathbf{f}(\mathbf{x}(t), t). \tag{3.9}
$$

Therefore, the proposed integration algorithms are consistent.

It is defined that a numerical method is said to satisfy the root condition if every root of the first characteristic polynomial $\rho(z)$ is either inside the unit circle, or on the unit circle but with multiplicity 1 [47].

Theorem 3.3. *A difference system is zero-stable if and only if it satisfies the root condition.*

For $\rho(z) = z^k - 1$, all the roots are on the unit circle and with multiplicity 1. The proposed integration algorithms satisfy the root condition. Thus, the proposed methods are zero-stability. Since the proposed integration algorithms are consistent and zero-stable, they are convergent.

In order to compare the damping effect of the proposed DDF-k algorithms, a simple LGC parallel circuit shown in Fig. 3.1 is used. The DDF-1, DDF-2 and
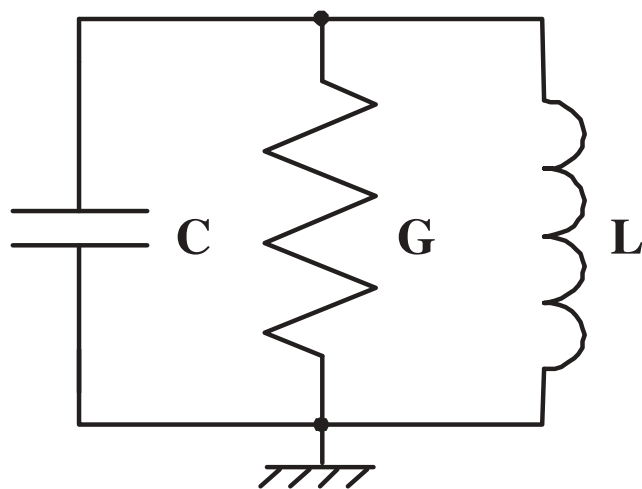
FIGURE 3.1: An LGC parallel circuit.
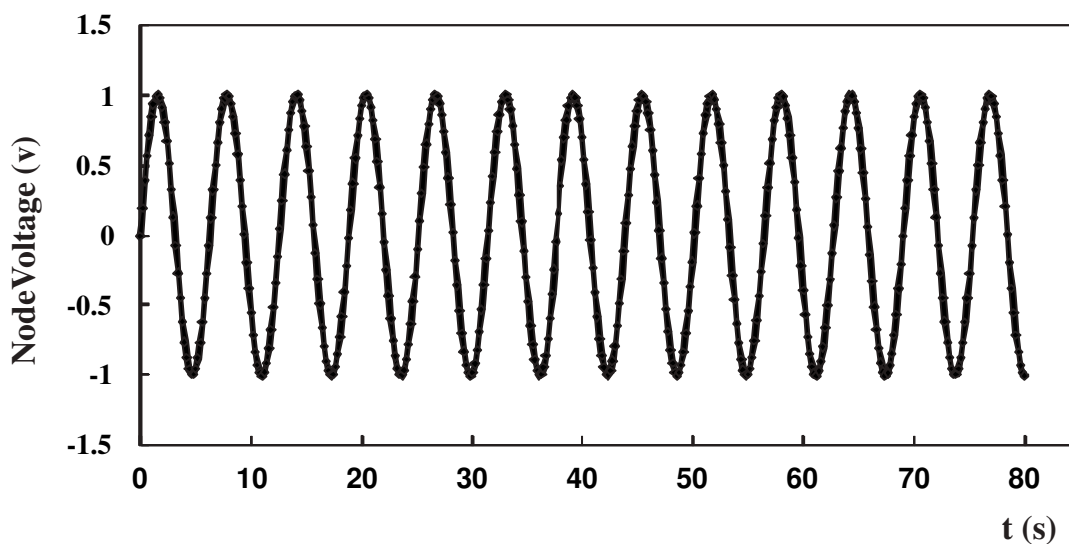
FIGURE 3.2: The node voltage waveform of LGC parallel circuit by using backward Euler.

DDF-3 are shown here as the examples. The sources of LGC circuit are set as follows: $L = 1$H, $C = 1$F, $G = -0.2$S and the step-size h is a constant value 0.2s. The initial condition of voltage and current are set to 0V and -1A. As shown in Fig. 3.2, it should oscillate forever by using the backward Euler method, since the loss mechanisms are not included in the simulation. If DDF-2 and DDF-3

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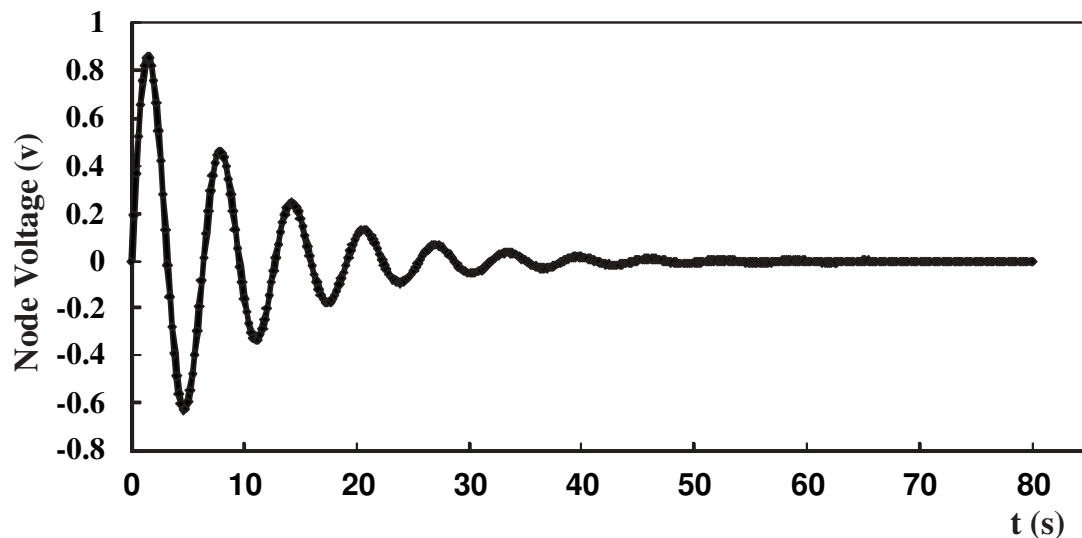
FIGURE 3.3: The node voltage waveform of LGC parallel circuit by using DDF-2.
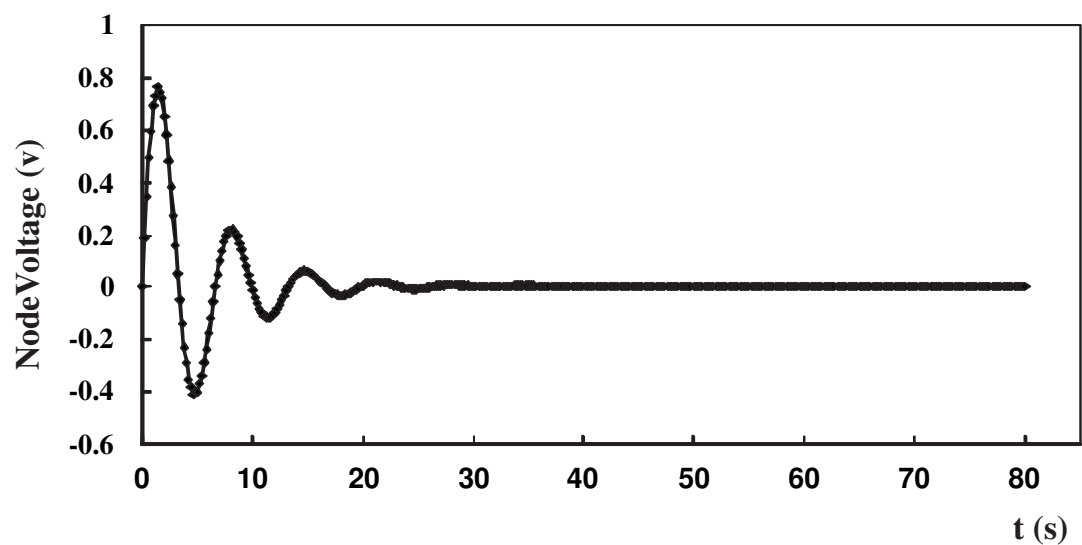
FIGURE 3.4: The node voltage waveform of LGC parallel circuit by using DDF-3.

methods are used, the amplitude of the oscillation asymptotically decays which is shown in Figs. 3.3 and 3.4. Easy to find that DDF-2 and DDF-3 add more damping effect compared with the DDF-1.
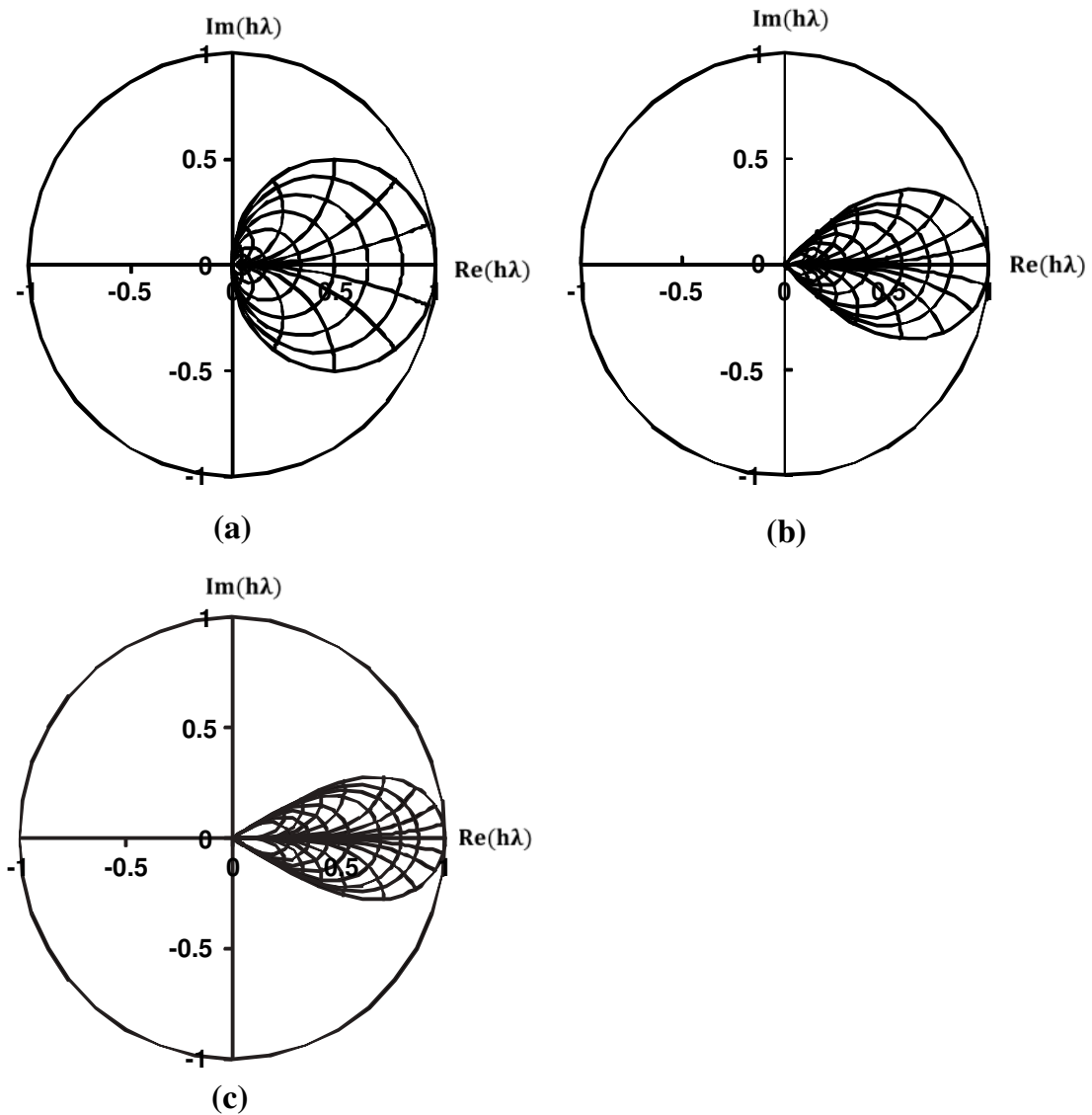
FIGURE 3.5: The region of absolute stability for different methods, (a) the backward Euler method,(b) DDF-2, and (c) DDF-3.

In Fig. 3.5, the z-transform of $h\lambda$ plane shows the stability region [1, 49] for the numerical methods. For $Re\lambda < 0$, the stability region is obtained, which contains the unit circle. Note that the stability region ameliorates as k increased. These over stable phenomenons will cause positive damping effect. By comparing the size of the stability region, it is obviously that the DDF-3 integration algorithm

has larger damping effect than the BE method.

3.2.2 Proposed PTA Method

The proposed PTA method is named as damped PTA (DPTA) for its damping effect. The resistive portion of a DC circuit is shown in Eq. (1.5). The solutions of this nonlinear algebraic equations are the DC operating points. The constant, pure pseudo element is composed of capacitors and inductors. For the capacitor and inductor, the relationship between voltage and current is expressed as:

$$
\begin{aligned}
I_C(t) &= C\frac{dV_C(t)}{dt}, & (3.10) \\
V_L(t) &= L\frac{dI_L(t)}{dt}. & (3.11)
\end{aligned}
$$

Therefore, after the insertion of pseudo-elements, the original circuit is modified to the PTA case. The common mathematical equations set is written as [43]

$$
\begin{aligned}
&\mathbf{F}(\mathbf{x}(t), t) + \mathbf{D}\dot{\mathbf{x}}(t) = \mathbf{0} & \text{(3.12a)} \\
&\mathbf{x}(t_0) = \mathbf{x_0} & \text{(3.12b)} \\
&\dot{\mathbf{x}}(t)\big|_{t=t_f} = \mathbf{0}, & \text{(3.12c)}
\end{aligned}
$$

where $\dot{\mathbf{x}}(t) = (\dot{\mathbf{v}}(t), \dot{\mathbf{i}}(t))^T$ is the derivative of $\mathbf{x}$ with respect to the time t, $\mathbf{D}$ is a matrix used to represent the pseudo capacitance and inductance matrix, t_0 is the start time of the transient analysis, $\mathbf{x_0}$ is the initial value of $\mathbf{x}$, and t_f means the

time when the pseudo circuit is settled down. Equation (3.12a) is numerically integrated to the steady state using a variable timestep scheme that attempts to increase the timestep as $\mathbf{F}(\mathbf{x}(t), t)$ approaches $\mathbf{0}$. Then applying the proposed numerical integration algorithms to Eq. (3.12).

Algorithmically, the procedure of the proposed DPTA method is concluded as following:

Step 1: insert the pseudo-elements and obtain the Eq. (3.12a);

Step 2: set the initial value for $\mathbf{x}$ and time-step size h at the start time of the transient analysis;

Step 3: use Eq. (3.3) to obtain $x_{n+1}{}^P$;

Step 4: apply DDF-k to the Eq. (3.12) and solve it at each time point t_{n+1} by Newton's method with $x_{n+1}{}^P$ as first guess;

Step 5: count the iteration number for Newton's method and by comparison with some user-specified control parameters, select a new time-step size h; if the number of iteration is too large reject the old step;

Step 6: convergence check with Eq. (3.12c) and if the circuit gets into the steady state, the pseudo-transient analysis converges to the solution;

Step 7: set $n = n + 1$ and go to Step 3.

3.2.3 Switching Algorithm for DPTA

In this section, an effective switching algorithm for the damped pseudo-transient analysis is proposed. From the convergence viewpoint, the switching algorithm

shows great importance. The convergence and efficiency are improved by switching numerical integration algorithms during the implementation.

The timestep control method used in the proposed PTA method is a simple iteration count method which has no additional calculation and quickly enlarge the timestep size. This method is controlled by two options: IMAX and IMIN. If the number of iterations per timepoint exceeds the IMAX value, it will roll back to the previous step and do the NR iteration again with a smaller timestep size. If the number of iterations per timepoint is between the IMIN and the IMAX, it will no change for the timestep size. If the last timepoint solution took fewer than the IMIN iteration, the timestep size is increased.

Consider the conventional timestep control algorithm with the Eq. (3.2). Here, the DDF-2 method is used as an example. When the NR method is difficult to get the solutions, it will roll back to the previous step and do it again with a smaller timestep size which means h_{n+1} is decreasing until the NR method gets a solution. The step size for backward Euler is $\xi(h_{n+1})$ and for DDF-2 is $\xi(h_{n+1}) + h_n$, where the choice of $\xi(h)$ is

$$\xi(h) = \left\{ \begin{array}{lcl} h/8 & : & h > h_{min} \\ h_{min} & : & h < h_{min} \end{array} \right. . \tag{3.13}$$

To maintain high efficiency and heavy damping effect, only the h_{n+1} is reduced, rather than decrease h_{n+1} and h_n together. However, in the proposed DPTA method, if the pseudo-circuit is so difficult that NR cannot get the solutions, h_{n+1} will be divided by 8 many times. Thus, h_{n+1} may far less than h_n. Thus, the step size for DDF-2 may have no change even the step size is smaller than a specific value like 10^{-9} which means non-convergence for NR method. From this
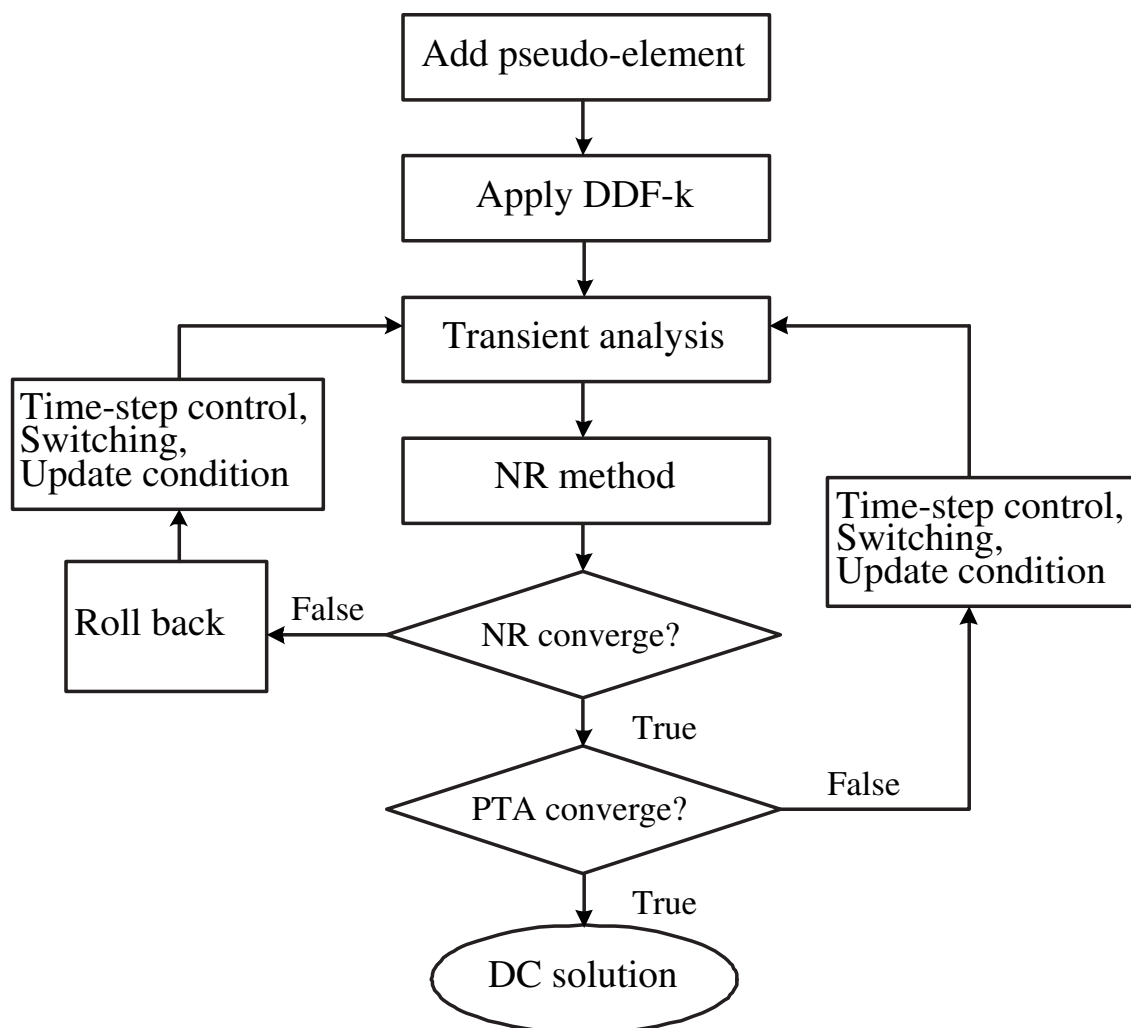
FIGURE 3.6: Proposed switching algorithm in DPTA.

view point, the convergence of DPTA cannot be guaranteed with this step control algorithm.

In order to deal with this problem, a switching algorithm is proposed which can automatically change among the different numerical integration algorithms. The DDF-k methods with varying degrees of damping effect are realized in proposed switching algorithm. As shown in Fig. 3.6, when the NR cannot get the solution, it will roll back to the previous step and use backward Euler algorithm with a

smaller timestep size. After that, if the NR method successfully converged, the DDF-k algorithm will be used again.

3.3 Numerical Examples

In order to get a good performance of convergence and efficiency, the proposed DPTA method with DDF-3 is used to do the test. There are totally 62 test circuits in INOUE laboratory. All of them have been solved with DPTA. However, most of them are also very easy to be solved by using CEPTA (CPU time < 0.01s). Therefore, only three typical circuits are shown in this section to demonstrate the DPTA method. First one is a 15 stage inverter chain to do the comparison between pure PTA and DPTA. Second one is a large scale circuit, which demonstrates that DPTA is more effective than CEPTA for large, complex circuits. Third one is a combinational circuit. It combines the oscillation circuits, multiple solutions circuits and practical circuits together to show that the DPTA method has the ability to deal with the complex circuits. The same convergence condition as in [44] is used. The simulator (Waseda SPICE) is based on SPICE3F5, and all simulations are running on Windows 7 operating system (CPU: 2.80GHz Core(TM), Memory: 8GB, Compiler: Visual Studio 2008). The hyphens "-" in each Table means that the method is failed or has no such information. The CPU time cannot be compared with HSPICE due to the reason that it depends on the computer performance and our computer performance is different from the server of HSPICE.

3.3.1 15-stage CMOS Inverter Chain

Fifteen stage CMOS inverter chain as shown in Fig. 3.7 is the example for group one which is used as an example in [44]. Due to the 15-stage negative feedback, the loop gain of the circuit is large. Figure 3.8 shows one node voltage in 15 stage CMOS inverter chain with the original pure PTA method. The result of DPTA is shown in Fig. 3.9. Obviously, from Figs. 3.8 and 3.9, it can be seen that DPTA is more powerful to prevent oscillation problem.
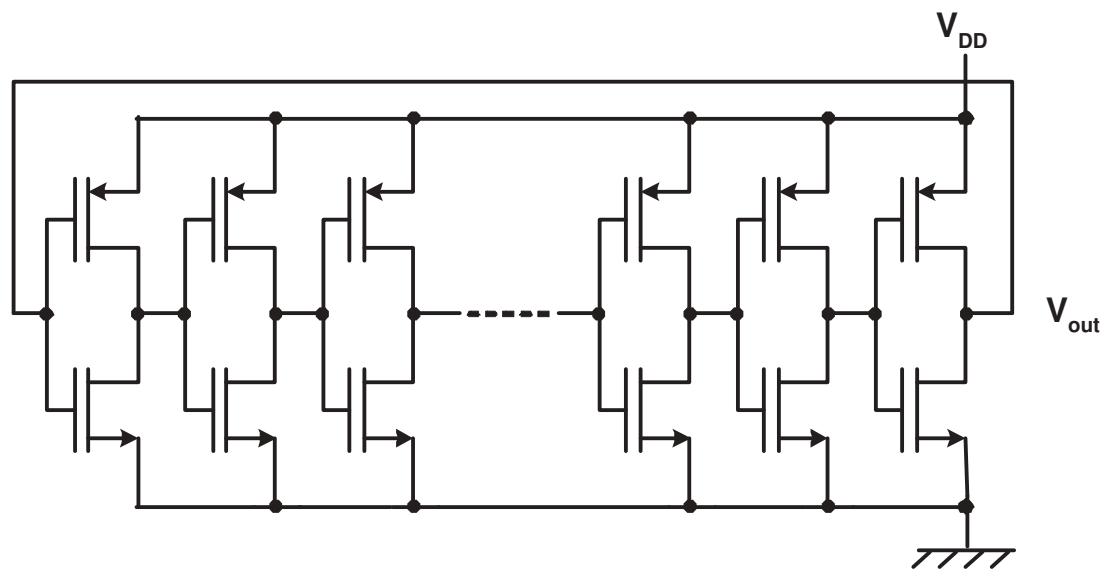
FIGURE 3.7: Fifteen stage CMOS inverter chain. Vdd = 5(V).
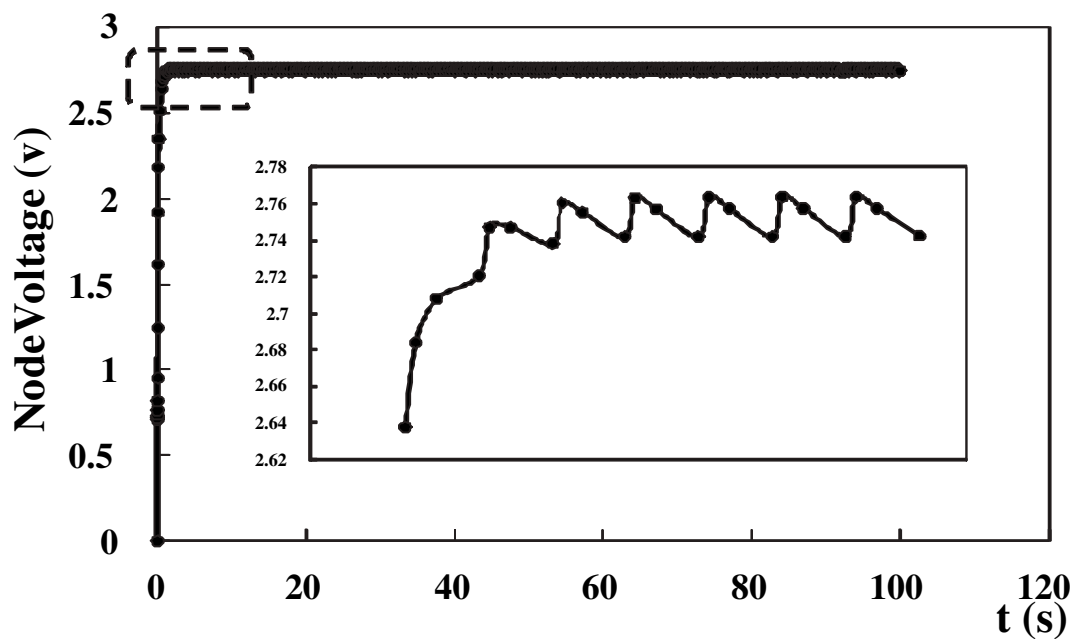
FIGURE 3.8: Waveform result of a node voltage in 15-stage CMOS inverter chain which oscillates by using pure PTA method.
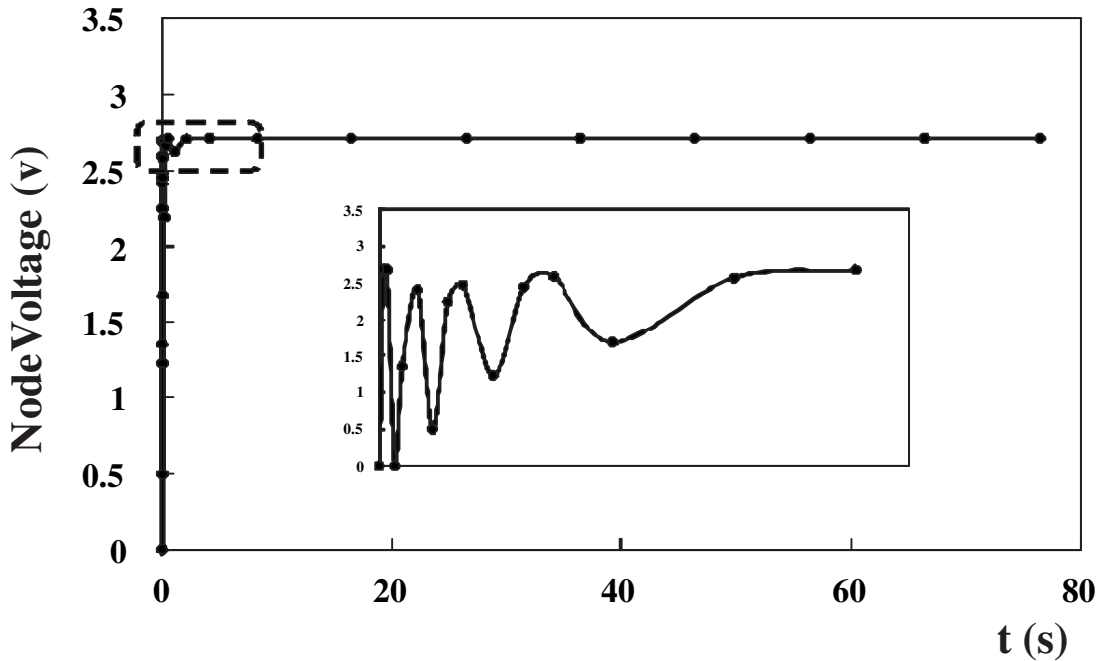
FIGURE 3.9: Waveform result of a node voltage with the DPTA method.

In [44], this circuit converges easily by using CEPTA with base-emitter embedding position. However, this embedding position is not the most widely used one. As a typical class of oscillation circuits, inverter chain circuits are often used as sub-circuit for some large-scale circuits. Thus, it is much better that if this circuit is solved with other embedding positions. The simulation results are shown in Table 3.1. DPTA succeeded to converge for all embedded positions. Compared with CEPTA, the worst speedup ratio is 0.81X, which is acceptable.

3.3.2   Practical Analog CMOS Circuits

Test circuit for this group is the automobile intake system in [51] which has 1096 nodes, 1909 elements and 1516 MOSFETs. The structure of the intake system is shown in Fig. 3.10, and two components are shown in Figs. 3.11, 3.12. Table

TABLE 3.1: Simulation performance comparison of 15-stage CMOS inverter chain.

Circuit	Algorithm	# of Iters	# of Steps	CPU time (s)	Speedup of CPU time
	HSPICE	-	-	-	-
	CEPTA(BE)	48	17	0.013	1X
15-stage CMOS	CEPTA(BE-BC)	-	-	-	-
inverter chain	CEPTA(diagonal)	-	-	-	-
(47 nodes,	DPTA(BE)	94	25	0.015	0.87X
30 MOSFETs)	DPTA(BE-BC)	94	25	0.0158	0.82X
	DPTA(diagonal)	103	28	0.016	0.81X

TABLE 3.2: Simulation performance comparison of the intake system.

Circuit	Algorithm	# of Iters	# of Steps	CPU time (s)	speedup of CPU time
Intake system	HSPICE	-	-	-	-
(1096 nodes,	improved CEPTA [44]	6984	1226	44.008	1X
1516 MOSFETs)	DPTA(Diagonal)	1259	430	9.194	4.79X

3.2 shows the simulation performance comparison between the improved CEPTA method [44] and the proposed DPTA method. Compared with CEPTA, DPTA has 4.79X speedup of CPU time, and the number of NR iterations is reduced to 18.03%. HSPICE cannot get the solution.

After that, the test part is added into the intake system and do the simulation again. The result is shown in Table 3.3. The non-convergence problem occurs by using improved CEPTA method while DPTA has no such problem. Although a experimental designer can change the simulation condition to make this circuit converged, the problem is not fundamentally solved.
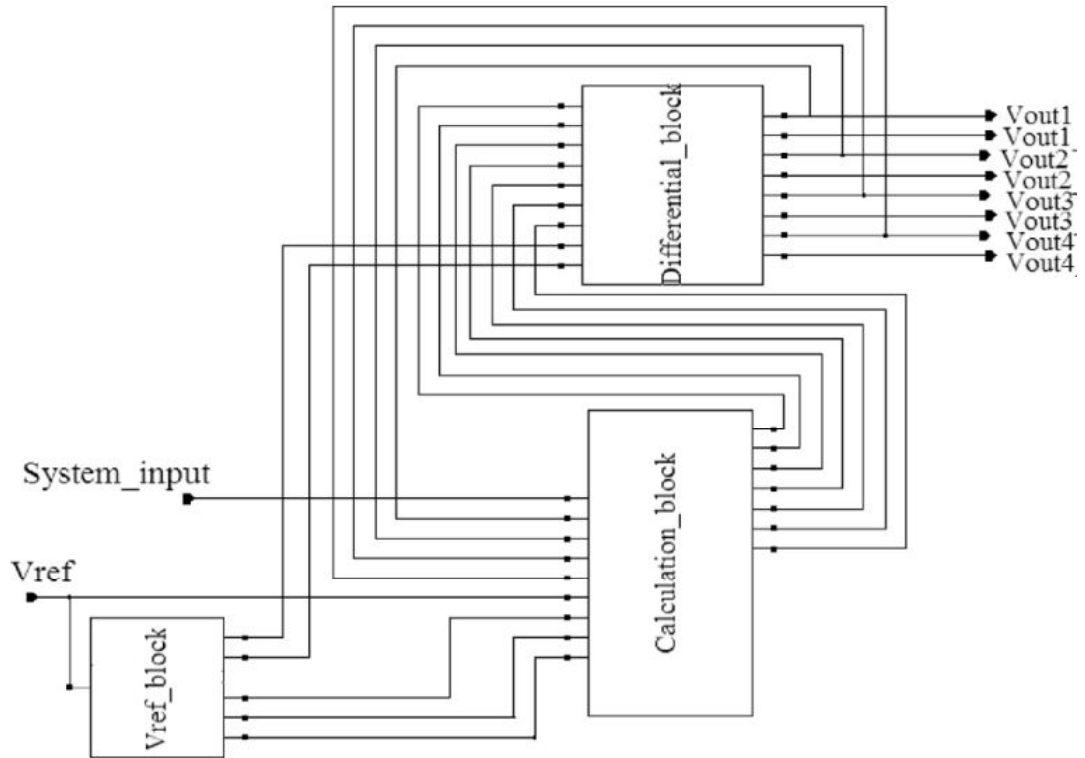
FIGURE 3.10: The analog circuit system structure fo1r the engine intake system [51].

TABLE 3.3: Simulation performance comparison for the top of the intake system with testing part.

Circuit	Algorithm	# of Iters	# of Steps	CPU time (s)	speedup of CPU time
Top of the	HSPICE	-	-	-	-
intake system	improved CEPTA [44]	-	-	-	-
with testing part	DPTA(Diagonal)	1316	441	9.514	no comparison

57
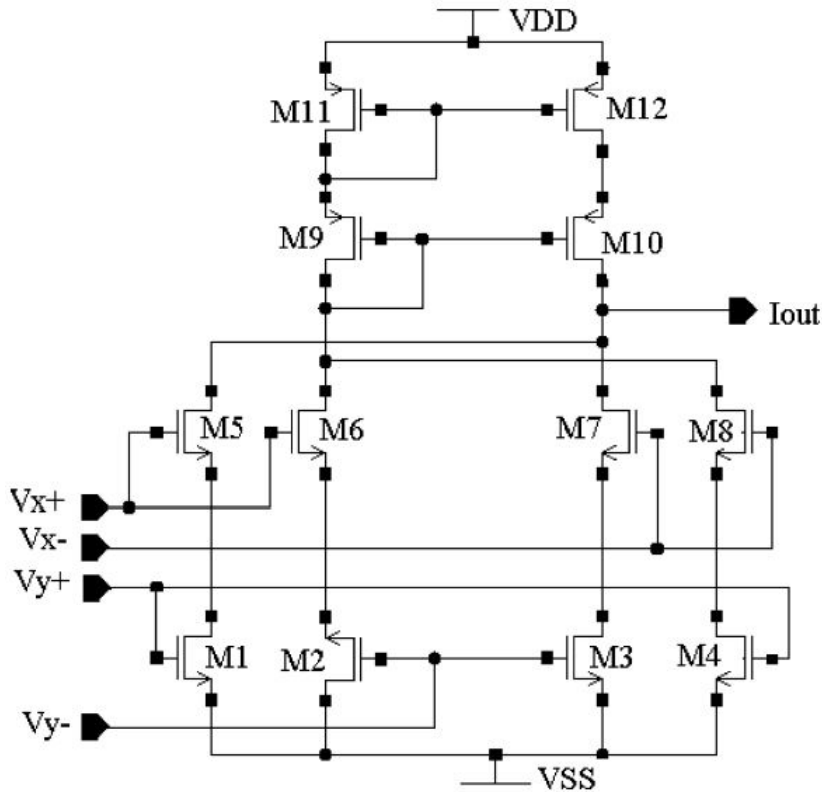
FIGURE 3.11: CMOS analog four-quadrant multiplier cell [51].

3.3.3 Combinational Circuit

The main part of this combinational circuit is a UA 741 5-stage PFB OP AMP circuit which is composed of 188 elements including 115 BJT's, and the total number of nodes is 234. The open-loop gain of this circuit is high, and the circuit has multiple solutions due to the 5-stage connected. Part of this circuit is presented as difficult example in [7, 26, 44]. The other parts of this combinational circuit are some simple but difficult circuits which need hundreds of iterations by using NR method. Thus, the whole combinational circuit has 272 elements including 144 BJT's and 12 MOSFETs, and the total number of nodes is 282.
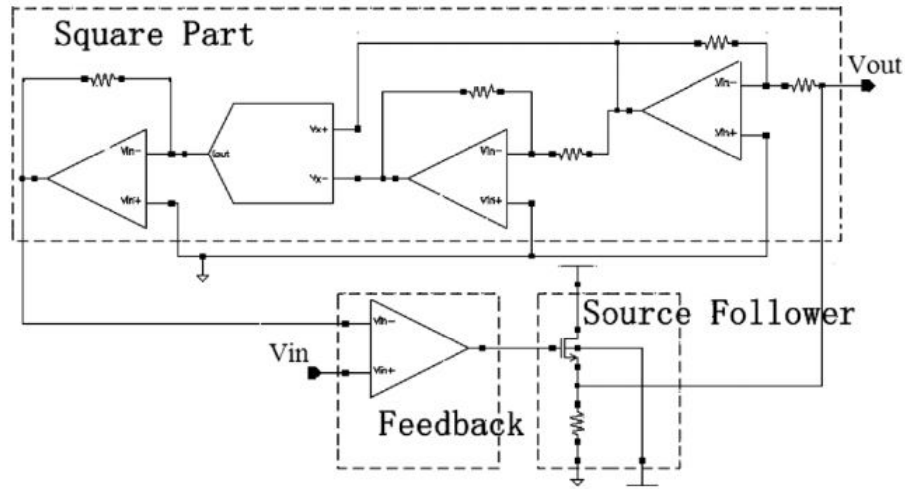
FIGURE 3.12: Analog square root circuit [51].

TABLE 3.4: Simulation performance comparison of the combinational circuit.

Circuit	Algorithm	# of Iters	# of Steps	CPU time (s)	speedup of CPU time
Combinational circuit	HSPICE	3026	-	1.16	1.97X
	CEPTA	-	-	-	-
	pure PTA (Diagonal)	5878	2252	2.285	1X
	DPTA (Diagonal)	2793	769	1.109	2.06X

Table 3.4 shows the simulation efficiency results of HSPICE, CEPTA, the conventional pure PTA method, and the proposed DPTA method. The efficiency of propose DPTA method is 2.06X faster than pure PTA method. The output file for HSPICE shows that this circuit cannot be solved by NR, Gmin stepping and source stepping method. At last, HSPICE uses their own PTA method, which is not public, to solve this combinational circuit with 3026 iterations. The proposed DPTA method has the best efficiency for this combinational circuit.

3.4   Conclusions

In this work, the damped pseudo-transient analysis (DPTA) method is proposed. It uses new numerical integration algorithms with larger artificial damping effect to overcome the oscillation problem of PTA technique. Moreover, a switching algorithm is proposed to improve the convergence and efficiency of DPTA. With this new PTA method, 100% test circuits in INOUE Lab. are solved (62/62). Compared with conventional PTA methods, DPTA has $0.81X \sim 4.79X$ speedup of CPU time. Among them, using DPTA for the practical and large-scale circuit (1516 MOSFETs), the CPU time has 4.79X speedup, and the number of NR iterations is reduced to 18.03% of the iterations by using CEPTA.

Chapter 4

An Adaptive Time-Step Control Method in Damped Pseudo-Transient Analysis for Solving Nonlinear DC Circuit Equations

4.1   Introduction

Time-dependent methods for computing DC operating points have been researched for years [2, 3, 5, 6, 43, 44], but only a few studies are about the time-step control method. In commercial SPICE-like circuit simulators, the time-step control method is complex because it includes a large number of parameters and functions. In the majority of cases, these parameters and functions are in fact used to limit the growth of time-step size, since transient analysis methods are sensitive to truncation errors [1, 9]. In contrast, the time-step size chosen for pseudo-transient analysis (PTA) methods does not need to consider accuracy. In fact, the time-step should be made large enough, as if the NR can converge [7]. Thus, an effective time-step control method is highly desirable.

The time-step control method used in [43, 44] is a simple iteration count method, which has no additional calculation. It is controlled by two options: IMAX and IMIN. If the number of iterations per timepoint exceeds IMAX, it rolls back to the previous step and reduces the time-step size. If the number of iterations per timepoint is between IMIN and IMAX, it does not change the time-step size. If the number of iterations is smaller than IMIN, the time-step size is increased. This method has the advantage of being simple and efficient since it can quickly enlarge the time-step size. However, choosing suitable parameters, which include IMAX, IMIN, initial time-step size, and the growth rate of time-step size, is a difficult problem.

As mentioned in Chapter 2, the SER method increases the time-step in inverse proportion to the residual reduction [46]. The idea of SER provides a way to automatically optimise the time-step size, since the change of the residual reduction shows the speed of convergence.

The k step damped differentiation formulas (DDF-k), proposed in chapter 3, are the numerical integration algorithms with artificial damping applied to the PTA techniques. This method is named damped pseudo-transient analysis (DPTA). To improve the efficiency of the DPTA method, an effective implementation based on SPICE3f5 is shown in chapter 3. From a practical standpoint, this implementation uses the DPTA method of step 1 through 3. The damping effect is enlarged as step k increases. Thus, an effective switching algorithm for DPTA is proposed to obtain a different damping effect. However, the damping effect is still limited by the value of step k. If the pseudo-control parameter values are not carefully chosen, the simulation efficiency of DPTA still needs to be improved.

4.2 Proposed Time-Step Control Method

The pseudo-transient analysis can be divided into two phases, and each of them has its own initial and final states. The searching phase begins with an inaccurate solution $\mathbf{x}$ and a time-step h that may be small and produces an accurate $\mathbf{x}$ and a large h. In this phase, the changes might be frequent and rapid since the inaccurate solution $\mathbf{x}$ is approaching to the real solution. In the converging phase, the solution for the pseudo-circuit is close to the steady state of the original circuit. Therefore, even a large time-step size is used in this phase, the change of $\mathbf{x}$ is small and the NR method can solve it easily. Thus, the upper limit of time-step size value in this converging phase can be large. If the time-step size in the converging phase is limited to a small and constant upper limit, the large number of iterations are needed, which leads to the low efficiency. In each phase, the requirement of the time-step size h is quite different. Therefore, we have to pay attention to the updating rules of h.

The conventional time-step control method does not fully consider the convergence of NR. Besides, it does not try to take the time-step size as large as possible. These two features may have some fatal problems when the control parameters of the time-step control method are not chosen carefully. Therefore, based on the idea of SER method [46, 50], an enhanced time-step control method is proposed, which can improve the robustness of DPTA.

Figure 4.1 shows the process of the proposed time-step control method. This new method includes two parts. The first part takes charge of the increment of time-step size by considering the number of iterations needed for NR, the relative change of $\mathbf{x}$, and the residual reduction of $\mathbf{F}(\mathbf{x})$. The second part takes charge of the decrement of time-step size, when NR fails to converge.
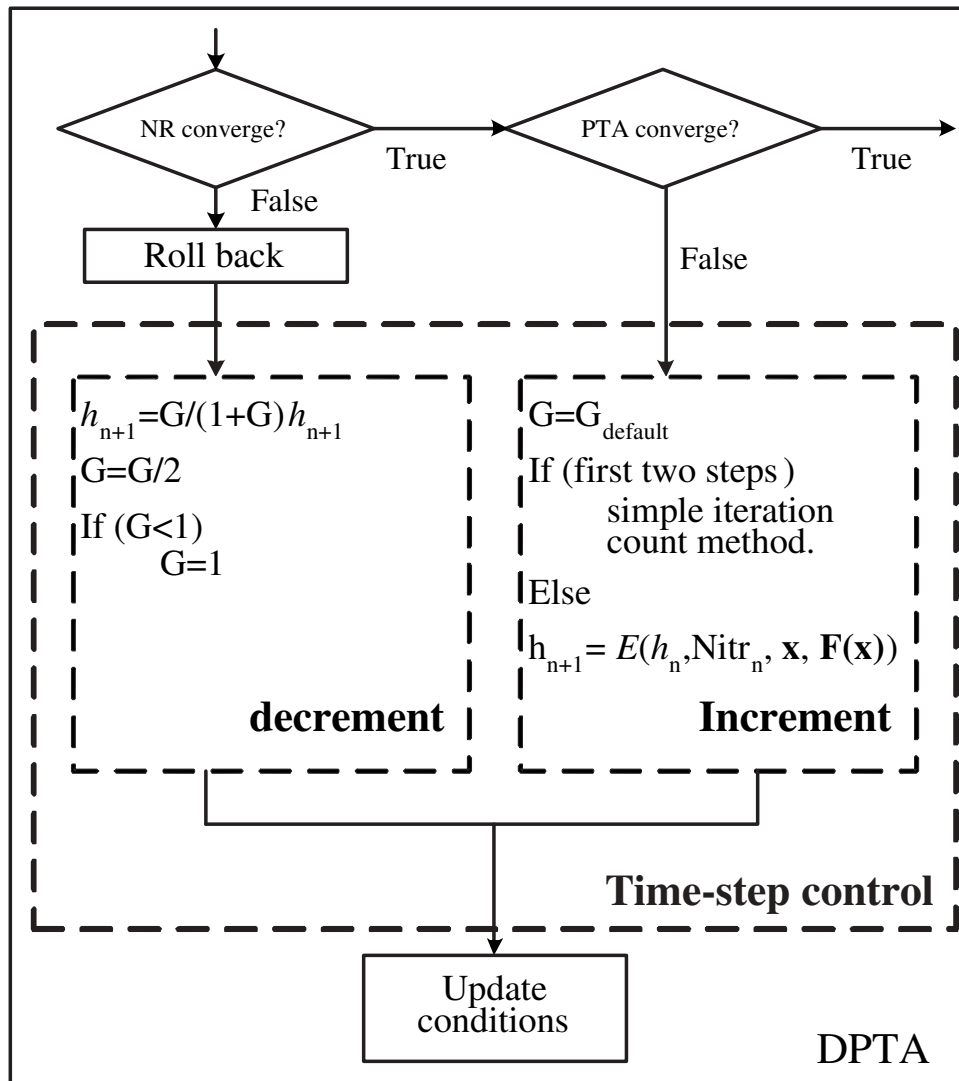
FIGURE 4.1: The process of the proposed time-step control method.

The new control algorithm is capable to adapt the time-step size without constant upper limit, which means that it can obtain the damping effect as large as possible. Moreover, the proposed method has a wider applicability to the pseudo-capacitor value, since it can automatically and effectively adapt the time-step size according to the circuit state during the simulation.

4.2.1 Increment Algorithm

An effective ODE integrator should have an adaptive control over its own progress, making frequent changes in its step size. Commonly, the purpose of such adaptive step size control is to achieve some predetermined accuracy in the solution with minimum computational effort [52]. A commonly implementation of adaptive step size control requires that the stepping algorithm signal information about its convergence, efficiency, most important, a evaluation of its local truncation error (LTE) [52]. However, the purpose of DPTA is finding the DC operating points of Eq. (1.5), rather than tracing the solution curve of Eq. (3.12a). Also notice that for DPTA, the larger time-step size is, the larger damping effect can be obtained. Therefore, the ideal time-step control method for DPTA only cares the convergence of NR.

This work considers the residuals reduction, the relative change of $\mathbf{x}$ and the iteration count together to predict the circuit state and to optimize a larger time-step size. The increment algorithm, in its simplest, unprotected form, is

$$
\begin{aligned}
h_{n+1} &= E(h_n, Nitr_n, \mathbf{x}, \mathbf{F}(\mathbf{x})) \\
&= h_n \cdot MAX\left(1, \delta \cdot \gamma \cdot \|\mathbf{F}(\mathbf{x}_{n-1})\|/\|\mathbf{F}(\mathbf{x}_n)\|\right),
\end{aligned}
\tag{4.1}
$$

where δ determines the relative change of $\mathbf{x}$ per time-step, γ assesses the difficult level for the convergence of NR in previous steps, and $\|\mathbf{F}\|$ is the norm of $\mathbf{F}$. It is defined that

$$
p = \frac{\|\mathbf{x}_{n-1} - \mathbf{x}_{n-2}\|/\|\mathbf{x}_{n-2}\|}{\|\mathbf{x}_n - \mathbf{x}_{n-1}\|/\|\mathbf{x}_{n-1}\|}, \quad (n \geq 2).
$$

The factor δ is shown in Eq. (4.2), together with the residual reduction, for determining the current situation of $\mathbf{F}(\mathbf{x})$.

$$\delta = \log_{10}\left(ap + b\right), \tag{4.2}$$

where a and b are constant, and $a > 0$, $b \geq 1$. Thus, $\delta \geq 0$. The idea behind δ is illustrated in Fig. 4.2. We set $a = 9$ and $b = 1$ to obtain two important properties (the larger a and b increases the weight of δ),

Property 1: If $p \rightarrow 0$, which means the relative change of $\mathbf{x}$ increases rapidly, $\delta \rightarrow 0$ will stop the increment of h_{n+1}.

Property 2: If $p \rightarrow 1$, which means the relative change of $\mathbf{x}$ almost has no change, δ is approaching to 1.

At the beginning of DPTA ($n = 1, 2$), the simple iteration count method is used to update the time-step size, until we have $\mathbf{x}_1$ and $\mathbf{x}_2$. Note that, $\|\mathbf{x}_n\| = 0$ means all source values are set to be zero. It only happens in the initialization stage at t_0. If $\|\mathbf{x}_n - \mathbf{x}_{n-1}\| = 0$, the circuit achieves the steady state.

The factor δ mainly works at the searching phase since there is almost no change for the order of magnitude of $\mathbf{x}$ in converging phase. By using the log function, even p changes rapidly, the value of δ is still not too small or too large. Such small variation range is helpful for the smooth change of time-step size. The ideal tendency for the relative change of $\mathbf{x}$ is going to be smaller and smaller, so that the time-step size can be larger and larger. However, if the relative change of $\mathbf{x}$ is going to be larger, $\delta < 1$ limits the growth of time-step size to help the convergence
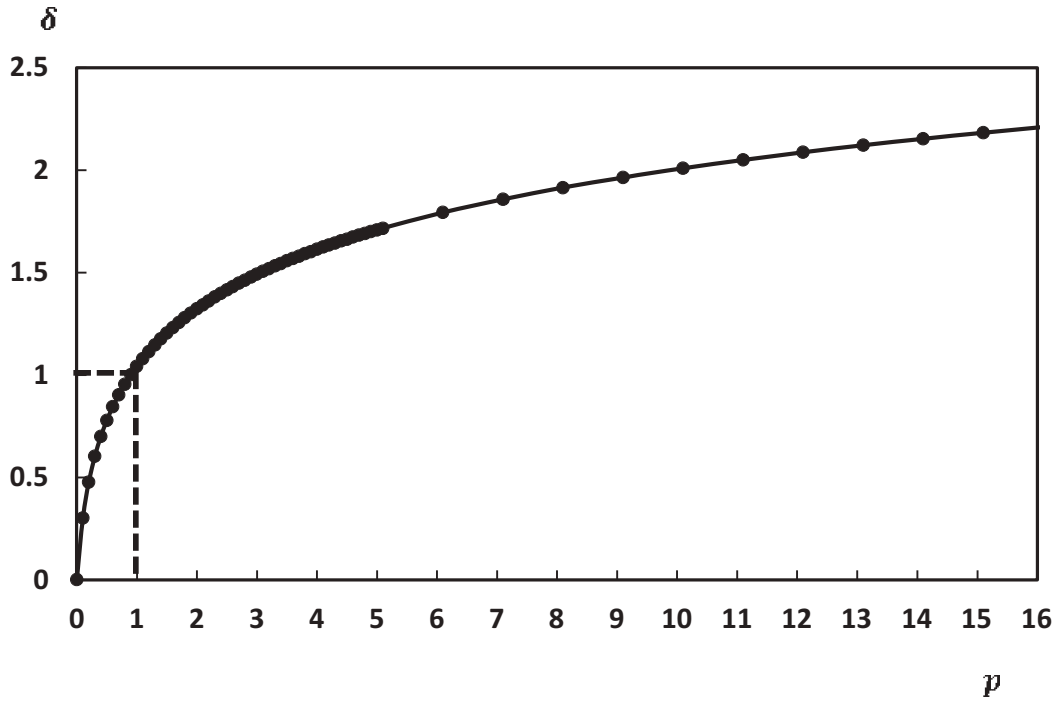
FIGURE 4.2: p and variable response of δ (a=9, b=1).

of NR. For the proposed method, the time-step size is based on the norm of the nonlinear residuals $\|\mathbf{F}(\mathbf{x}_n)\|$ rather than on the norm of $\Delta \mathbf{x}$, $\|\mathbf{x}_n - \mathbf{x}_{n-1}\|$, since that the small $\Delta \mathbf{x}$ does not imply the small residuals.

Here an example, shown in Fig. 4.3, is used to present the variable response of δ in different situations. There are 16 different combinations, and three of them are most important: oscillation (A1+B1), rapid change (A4+B1, A2+B1), and smooth change ((A1,A2,A4)+B2). The response of δ is shown in Table 4.1. If the relative change of $\mathbf{x}$ is going to be smaller, δ is larger than 1 to increase the time-step size. If oscillation or a rapid change occurs, $\delta < 1$ will limit the enlargement of time-step size.

The notation of γ is shown in Eq. (4.3),
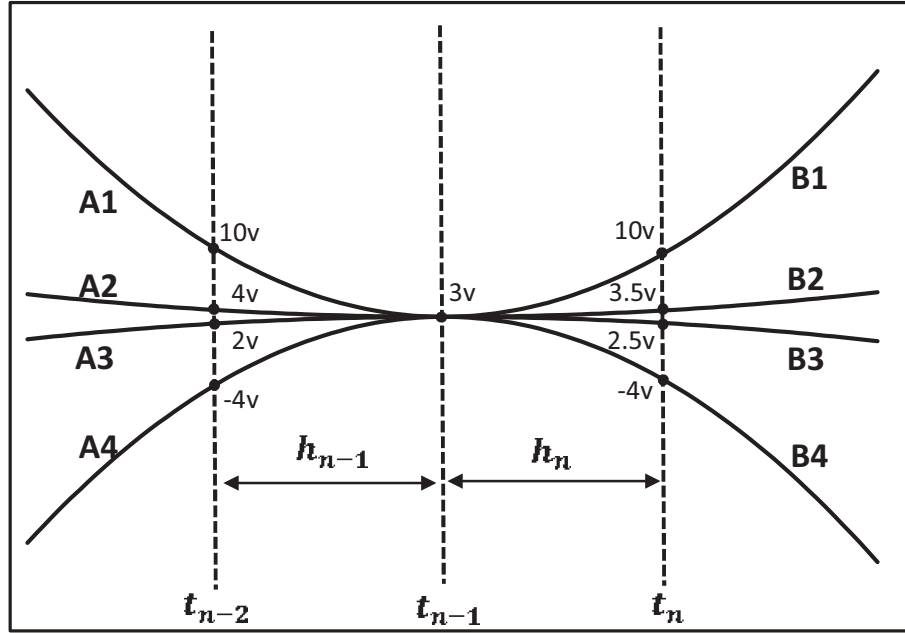
FIGURE 4.3: Example for showing the different conditions of a solution curve.

TABLE 4.1: The response of δ for different combinations (a=9, b=1).

	A1+B1	A1+B2	A2+B1	A2+B2	A4+B1	A4+B2
δ	0.602	1.633	0.316	1.204	0.929	2.025

$$\gamma = \frac{IMIN}{Nitr_n}, \tag{4.3}$$

where $Nitr_n$ is the number of iterations needed for NR at the step number n. If $Nitr_n$ is smaller than $IMIN$, which means that NR is easy to converge in the previous step, γ is larger than 1 and the proposed method tries to enlarge the time-step size.

In the proposed method, h_n is kept below a large enough bound h_{max}, which

can be considered as infinity, since the data types in C program have their own limitation. Therefore, I will allow for more generality in the formulation of h_n. For a given initial time-step h_0 and $n \geq 1$, the sequence h_n is

$$h_{n+1} = \phi\left(E(h_n, Nitr_n, \mathbf{x}, \mathbf{F}(\mathbf{x}))\right), \tag{4.4}$$

$$\phi(h) = \begin{cases} h_{min} & : & h \leq h_{min} \\ h & : & h_{min} < h \leq h_{max} \\ h_{max} & : & h > h_{max} \end{cases} . \tag{4.5}$$

This increment algorithm is aggressive. It always tries to enlarge the time-step size, even in some difficult situations. The larger time-step size enlarges the damping effect, which is useful for solving the oscillation problem.

4.2.2 Decrement Algorithm

For other continuation methods, a small step size just means the bad efficiency. However, for DPTA, it might cause the oscillation. The decrement of time-step size reduces the damping effect even to be negative. The negative damping effect is capable to convert a pseudo circuit into an oscillator. Therefore, the roll-back mechanism of DPTA should reduce the time-step size cautiously. As shown in Fig. 4.1, when NR fails to converge, the proposed roll-back mechanism works:

Step 0: $G = G_{default}$;

Step 1: set $h_{n+1} = \frac{G}{1+G} \cdot h_{n+1}$;

Step 2: solve the matrix by using NR;

Step 3: if NR gets the solution, go to Step 5. If NR fails again, go to Step 4;

Step 4: set $G = G/2$. If $G < 1$, $G = 1$. Go to Step 1;

Step 5: Set $G = G_{default}$. Resume work in the current pseudo-step.

The new roll-back mechanism is capable to get a larger time-step size, since it does not use a constant ratio to decrease the time-step size. The disadvantage of this method is that much more iterations are needed in some difficult situations. Here, the initial condition is $G_{default} = 10$ due to the comprehensive consideration of many test results. In general, this new method uses up to three extra pseudo-steps to reduce the time-step size in some really difficult situations. It is acceptable from the efficiency viewpoint.

4.3   Numerical Examples and Comparisons

The proposed time-step control method is implemented in Waseda SPICE (WSPICE) based on SPICE3f5. In order to verify the effectiveness of the proposed time-step control method used in DPTA, 51 benchmark circuits are chosen from [53], including 13 BIP circuits and 38 MOS circuits. Other benchmark circuits in [53] are used to verify other functions of circuit simulator, like netlist troubleshooting and model compatibility. Besides, there are 62 test circuits in INOUE laboratory. Thus, there are totally 113 test circuits (62 from INOUE Lab., 51 from [53]). The largest circuit is a digital circuit including 18816 MOSFETs. The smallest circuit has only one BJT or one MOSFET. All these circuits have been solved with the proposed method. However, most of them are very easy to be solved by using conventional DPTA (CPU time < 0.01s). Therefore, only 14 benchmark circuits and 4 circuits in INOUE Lab. are shown in this section.

Firstly, Table 4.2 shows the comparison between the conventional SER [46] method and the proposed method for the 14 typical benchmark circuits [53]. The circuits' name, size, and performance improvement are listed in this table. Some of these circuits are easy to oscillate due to the insertion of the pseudo-elements, which can verify the capability of the proposed time-step control method for overcoming the defects of PTA techniques. In Table 4.2, - means the conventional methods failed to converge. All tests shown in Table 4.2 use default parameters' value (capacitor value is 1E-4 F, initial time-step size is 1E-3s). The speedup ratio means that the CPU time of conventional method devided by the CPU time of proposed method. Comparing with the conventional SER method [46], the proposed method has $1.37X \sim 76.34X$ speedup of CPU time.

Secondly, four typical circuits are singled out to show the comparisons among the simple iteration count method (conventional DPTA proposed in Chapter 3),

TABLE 4.2: The list of test circuits, the circuit sizes, and the performance improvement(using default parameter values).

Circuit	Nodes	eqn	bjt	mosfets	sources	speedup
benchmark circuits[53]						
ring	18	19	0	34	11	-
g1310	66	97	28	14	3	4.21X
mux8	30	42	0	64	12	74.07X
schmitfast	5	19	0	8	2	1.74X
slowlatch	12	37	0	14	5	-
opampal	71	518	148	0	3	2.29X
optrans	270	1860	528	0	6	-
voter25	43	51	0	74	8	76.34X
voter	1708	1731	0	4243	23	-
ram2k	4849	32632	0	13880	23	1.37X

the original SER method (conventional SER) [46], and the proposed method. The first test circuit is a positive feedback circuit. The second one is an oscillator. The third one is combinational circuit. The last one is a MOS bandgap reference circuit. The simulation performance is compared by convergence performances, the number of total iterations (# of Iters), the number of pseudo-steps (# of Steps), the number of rejected pseudo-steps (# of Rejected Steps), and CPU times. The CPU time is determined mainly by the number of iterations and the number of steps. In order to simplify the comparison, the constant inductors are used, and only change the value of capacitors for all pseudo-elements. Besides, the initial time-step size is also constant. The comparison results are shown in the following sections.
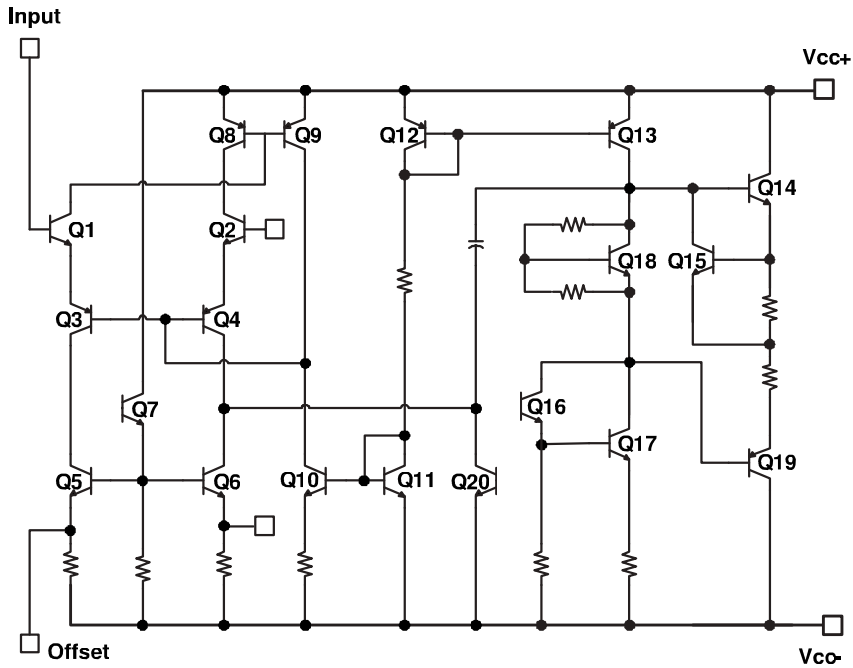
FIGURE 4.4: One stage UA741 operational amplifier.

4.3.1 Example 1: Positive Feedback Circuit

Firstly, a 5-stage positive feedback UA741 OP AMP circuit is considered. Figure 4.4 shows one stage UA 741 circuit. The UA 741 operational amplifier with a positive feedback is 5-stage connected in cascade configuration. The number of elements is 188 including 115 BJT's, and the total number of nodes is 234. The open-loop gain of the circuit is high. Because of the 5-stage connected, the circuit has multiple solutions. Part of this circuit is presented as a difficult example in [7]. Because of the positive feedback, the high loop gain and multiple solutions, the circuit is difficult that the SPICE3 and even the commercial simulators cannot easily converge to the solution.

Table 4.3 shows the simulation results of different time-step control methods. In the table, TRUE means that the algorithm successfully achieves the steady state,

and $*$ means the number of total iterations is larger than 10^8 which is unacceptable for our research. The number of steps is the number of pseudo-steps needed to converge to the final solution. The number of rejected steps shows the number of pseudo-steps when the NR method fails to converge. From the test results, for the simple iteration count method, (# of Iters) $\approx 2*$ (# of Steps), which means that in the most of pseudo-steps, the NR method only needs 2 iterations to get the solution. The NR method can easily get converged at each time point. However, the number of total iterations is much larger than the proposed method since a large number of pseudo-steps are needed. One of the reasons is that the maximum step size limits the growth of time-step size. It can be solved by changing a larger maximum time-step size, and then the new problem is how to choose a suitable value. Note that for the proposed method, even the value of capacitor changes in a wide range, the convergence efficiency is similar which means that users do not need to choose the value of pseudo-capacitor carefully by using the proposed method. For this circuit, it has been proved that the proposed time-step control method is capable to choose a larger and suitable time-step automatically.

In this case, the test circuit is not easy to oscillate especially for the small capacitor used in pseudo-elements. So the larger damping effect does not offset the additional requests of total iterations. In some conditions, the conventional SER [46] method uses less total iterations (little difference), but more pseudo-steps (almost 1.5 times). In each pseudo-step, the simulator updates the data of pseudo-circuits for doing transient analysis. This I/O function costs many CPU times especially for large-scale circuits. Although the proposed method fails to reduce the number of total iterations, it successfully reduces the CPU times.

Compared with conventional DPTA, new method has $0.94X \sim 1.24X$ speedup of CPU time. Compared with the best result of conventional SER [46], proposed method has $1.22X \sim 1.62X$ speedup of CPU time. Moreover, the proposed

method has a wider applicability to the pseudo-capacitor value

TABLE 4.3: Simulation performance comparison of UA741 5-stage PFB OP AMP.

Condition		Results					
Algorithm	Capacitor value (F)	Convergence Performance	# of Iters	# of Steps	CPU time (s)	# of Rejected Steps	speedup of CPU time
conventional DPTA	1E-6	TRUE	2986	1079	0.909	41	1X
	1E-4	*	-	-	-	-	-
	1E-2	*	-	-	-	-	-
	1	*	-	-	-	-	-
conventional SER ($\delta \cdot \gamma = 1$) [46]	1E-6	TRUE	1948	434	1.327	54	0.69X
	1E-4	TRUE	1788	402	1.186	56	0.77X(1X)
	1E-2	TRUE	2032	526	1.651	54	0.55X
	1	TRUE	3035	996	2.823	58	0.32X
proposed control method	1E-6	TRUE	1832	259	0.733	91	1.24X(1.62X)
	1E-4	TRUE	1884	272	0.786	96	1.16X(1.51X)
	1E-2	TRUE	2269	340	0.971	118	0.94X(1.22X)
	1	TRUE	1970	301	0.825	98	1.10X(1.44X)

4.3.2 Example 2: Inverter-Chain Circuit

Secondly, a fifteen stage CMOS inverter chain (also called ring oscillator) [44], as shown in Fig. 3.7, is used as an example. Because of the 15-stage negative feedback, the loop gain of the circuit is large. The test results are shown in Table 4.4. This circuit is easy to oscillate due to the insertion of the pseudo-elements. When the capacitor value is around 10^{-5}, the conventional DPTA method has good performance. The convergence efficiency of the conventional method decreases rapidly as the capacitor value increases. However, the proposed method still can get the good results. This feature is important for the proposed method since many complex circuits are composed of different kinds of sub-circuit, and each of them needs a specific capacitor value.

This case shows that the proposed method is powerful to decrease the oscillation, and the robustness of DPTA is improved. Compared with conventional DPTA, the proposed method has $13.64X \sim 104.82X$ speedup of CPU time, and it has a wider applicability to the pseudo-capacitor value.

The performance of conventional SER [46] method is too bad in this case. It uses several hundred times the CPU time than the proposed method. It is not a general performance, and will not be counted into the final conclusion.

TABLE 4.4: Simulation performance comparison of 15-stage CMOS inverter chain.

Condition			Results				
Algorithm	Capacitor value (F)	Convergence Performance	# of Iters	# of Steps	CPU time (s)	# of Rejected Steps	speedup of CPU time
conventional DPTA	1E-6	*	-	-	-	-	-
	1E-5	TRUE	296	65	0.039	8	59.13X
	1E-4	TRUE	25242	4604	2.306	842	1X
	1E-2	*	-	-	-	-	-
conventional SER ($\delta \cdot \gamma = 1$) [46]	1E-6	*	-	-	-	-	-
	1E-4	*	-	-	-	-	-
	1E-2	TRUE	29482	14468	11.825	45	0.20X
	1	*	-	-	-	-	-
proposed control method	1E-6	TRUE	937	103	0.169	65	13.65X
	1E-4	TRUE	71	20	0.022	1	104.82X
	1E-2	TRUE	159	30	0.055	9	41.93X
	1	TRUE	113	27	0.053	4	43.51X

4.3.3 Example 3: Combinational Circuit

Thirdly, the oscillation circuits, the circuits with multiple solutions and the practical circuits are combined together. In order to have a heavy oscillation, some oscillators are included in the combinational circuit. Moreover, this circuit combines the MOS FETs and BJT together. For each sub-circuit, the suitable pseudo control parameters, including the capacitor value, initial time-step size, maximum step-size, and so on, are quite different. For the simple iteration count method, it is difficult to choose the suitable parameter values. As shown in Table 4.5, compared with the iteration count method and the conventional SER [46] method, it is obvious that the proposed method has a wider applicability to different capacitor values. The robustness of DPTA is improved by using the proposed time-step control method.

Compared with conventional DPTA, the proposed method has $0.86X \sim 1.09X$ speedup of CPU time. Compared with conventional SER [46], the proposed method has $1.46X \sim 1.85X$ speedup of CPU time. It has a wider applicability to the pseudo-capacitor value compared with both conventional DPTA and conventional SER.

TABLE 4.5: Simulation performance comparison of combinational circuit.

| Condition			Results				
Algorithm	Capacitor value (F)	Convergence Performance	# of Iters	# of Steps	CPU time (s)	# of Rejected Steps	speedup of CPU time
conventional DPTA	1E-6	TRUE	1228	262	0.260	22	1X
	1E-4	*	-	-	-	-	-
	1E-2	*	-	-	-	-	-
	1	*	-	-	-	-	-
conventional SER ($\delta \cdot \gamma = 1$) [46]	1E-6	TRUE	1206	286	0.643	24	0.40X
	1E-4	TRUE	840	168	0.439	34	0.59X(1X)
	1E-2	*	-	-	-	-	-
	1	*	-	-	-	-	-
proposed control method	1E-6	TRUE	629	94	0.238	27	1.09X(1.85X)
	1E-4	TRUE	678	99	0.240	33	1.08X(1.83X)
	1E-2	TRUE	751	120	0.301	32	0.86X(1.46X)
	1	*	-	-	-	-	-
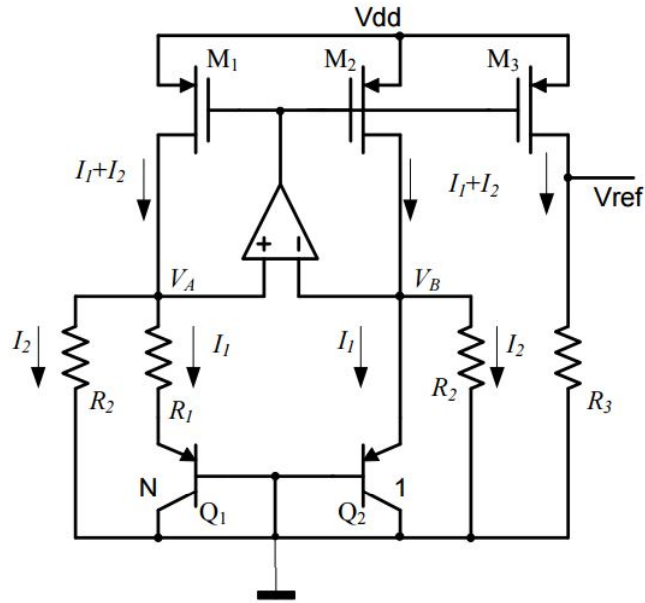
FIGURE 4.5: A MOS bandgap reference circuit [53].

4.3.4   Example 4: MOS Bandgap Circuit

A simple and practical MOS Bandgap reference, shown in Fig. 4.5, is used as the fourth example. This circuit is typical to show the advantages of the proposed method. Many test results show that the simulation efficiency of the simple iteration count method is affected by the maximum step size. This case will show the problem for the simple iteration count method without upper limit. The bandgap reference circuit has no electron states which also clarifies that there could be more than one solutions within a range.

Figure 4.6 shows the solution curve of a node voltage from t_0 to t_f by using the simple iteration count time-step control method when the maximum time-step size is a constant value. Even though the circuit finally converges to the steady state, too many pseudo-steps are needed in the converging phase because of the limited time-step size to the fixed constant maximum value. The simulation efficiency is
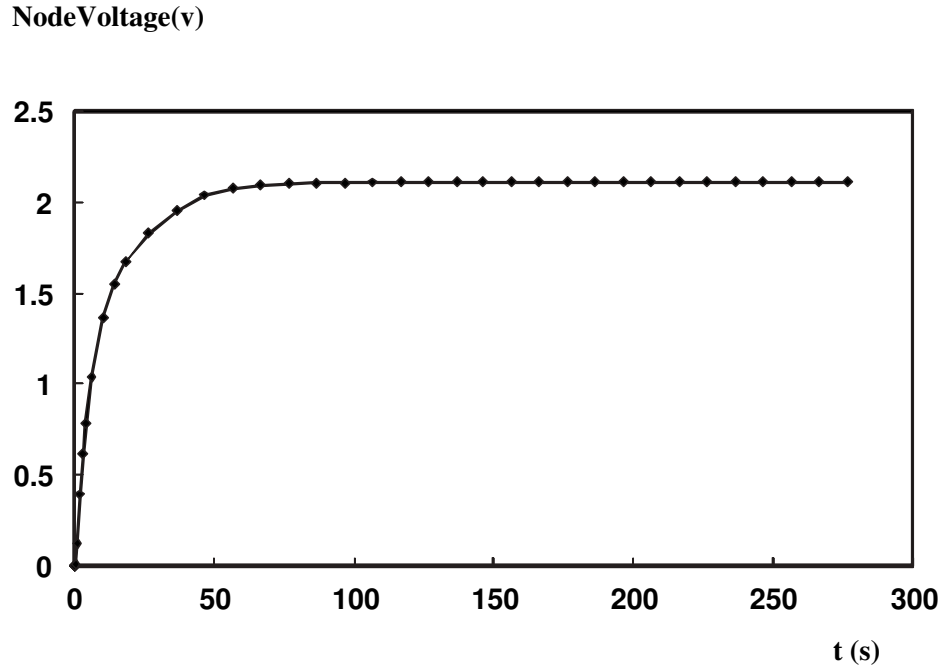
NodeVoltage(v)

FIGURE 4.6: The solution curve by using conventional method with a constant maximum time-step size for solving MOS Bandgap circuit.

not satisfactory. Figure 4.7 shows the solution curve by using the simple iteration count method without the upper limit, which is not converged. The time-step size changes periodically as shown in Fig. 4.8. This figure represents the time-step size h chosen for each pseudo-step. Note that, at the step number 21, the NR method converges easily with the time-step size around 33 second. Thus the time-step is doubled at the step number 22. However, the NR method fails to converge at the step number 22 with such a large time-step size. Then, the time-step size is divided by 8, which is smaller than 10 second. Such rapid change of the time-step size may lead to the change of damping effect. The solution curve might approach to a different solution. This kind of rapid change for the time-step size will occur in cycles and the solution curve will vary periodically as shown in Fig. 4.7. The steady state cannot be obtained finally.

For the proposed time-step control method, the growth rate of time-step size
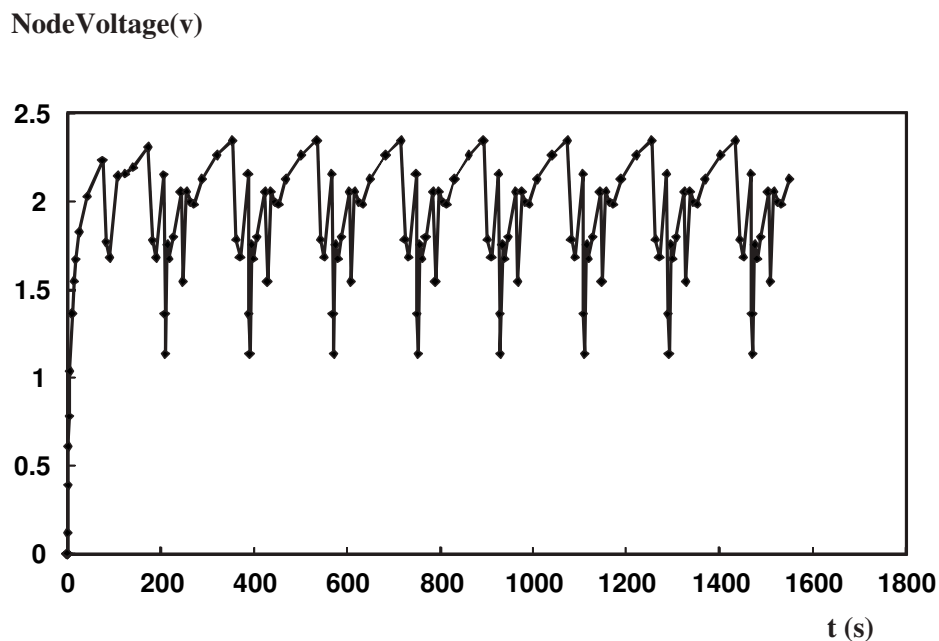
NodeVoltage(v)

FIGURE 4.7: The solution curve by using conventional method with infinity maximum time-step size for solving MOS Bandgap circuit.

is carefully chosen according to the circuit state at each time point. As shown in Fig. 4.9, the solution curve approaches the steady state around 2.77v easily. The new time-step control method not only considers the iteration count, but also the relative change of **x** and the change of residual reduction. Thus the time-step size is limited in the searching phase. Also note that in the converging phase, the solution in each pseudo-step is close to the final solution. Therefore, the proposed method increases the time-step size without any upper limit. Using this case, the proposed method is proven to improve simulation efficiency, and the convergence of DPTA.
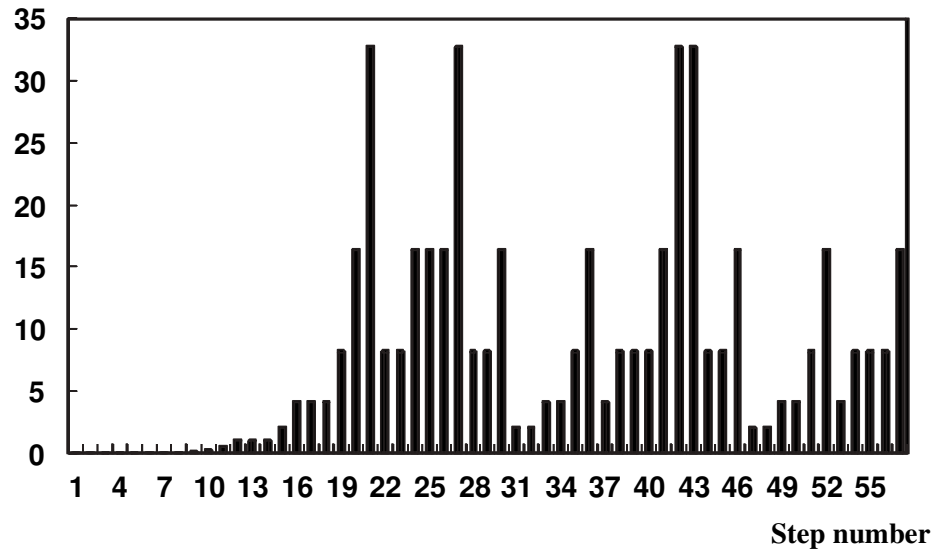
Time-step size (s)

FIGURE 4.8: The change of time-step size when the maximum time-step size is infinity for the conventional method.
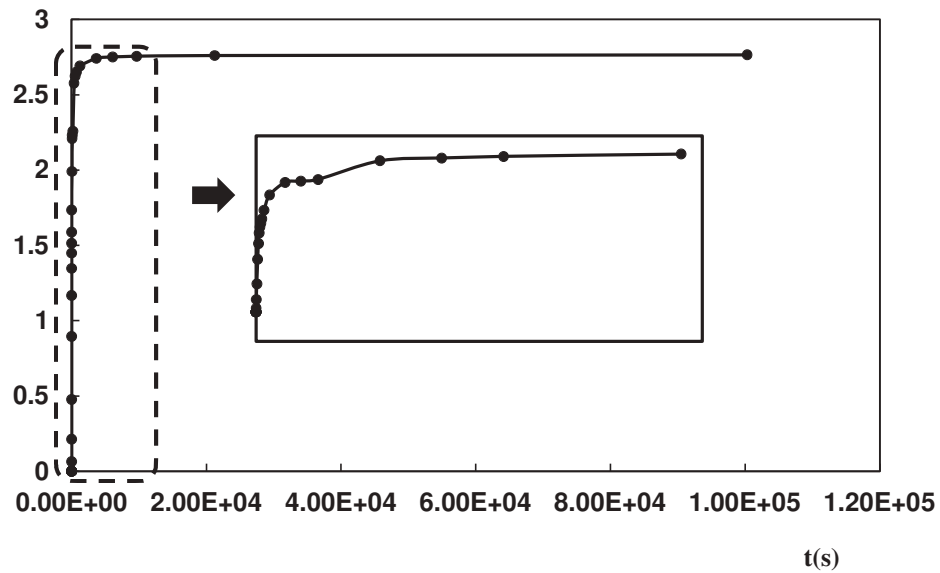
NodeVoltage(v)

FIGURE 4.9: The solution curve by using proposed method with infinity maximum time-step size for solving MOS Bandgap circuit.

4.4 Conclusions

In this work, a new time-step control method applied to DPTA for finding DC operating points of nonlinear circuits is proposed. This method is especially helpful when dealing with complex circuits combining several parts with different technology, where the requirement of parameter values is quite different. It has the ability to optimize the time-step size at each pseudo-step according to the circuit state.

Compared with conventional DPTA, the proposed method has $0.86X \sim 104.82X$ speedup of CPU time. Compared with conventional SER, the proposed method has $1.22X \sim 76.34X$ speedup of CPU time. It is also proved that, DPTA with the proposed time-step control method has the ability to 100% solve all test circuits in INOUE Lab. and the benchmark circuits (113/113). Moreover, the robustness of DPTA is enhanced. Compared with other time-step control methods, the proposed method can expand the range of capacitor value used in the pseudo-element.

Chapter 5

Conclusions

5.1   Conclusions

Solving the nonlinear DC equations and getting the DC operating point is the most fundamental and difficult part during the circuit simulation, since it is the base and prior to other analysis like transient analysis and AC analysis. Pseudo-transient analysis (PTA) is the most promising method to solve the nonlinear DC circuit equations. However, the most serious problem of this technique is that the oscillation problem and the discontinuity problem can not be solved simultaneously. A complete PTA method includes three major parts: the pseudo-elements, the numerical integration algorithms and the time-step control methods. All the former studies of PTA technique are from the pseudo-elements viewpoint. In this study, A different viewpoint is considered to improve the PTA technique. In this dissertation, a damped pseudo-transient analysis (DPTA) with adaptive time-step control method is proposed to solve these two problems. The proposed DPTA method uses new numerical integration algorithms with larger artificial damping effect to overcome the oscillation problem of PTA technique. Besides, a switching algorithm is proposed for the DPTA to further improve the efficiency by varying from different numerical integration methods. It can obtain various damping effect. The proposed time-step control method has the ability to optimize the time-step size at each pseudo-step according to the prediction of circuit state.

The organization of dissertation is concluded as follows.

In Chapter 1, the background and importance of this research are introduced. After that, the challenges in this study and the innovations are concluded. With the rapid progress of circuit design, the LSI analog circuits become complex and with mixed types of functions, circuit simulation is getting much more difficult

and important. The circuit simulation has three important components, including mathematical modelling of devices, formulation of nonlinear dc circuit equations and numerical algorithms to solve the equations. Pseudo-transient analysis (PTA) is the most promising method for solving the nonlinear dc circuit equations. However, all the conventional researches about PTA are from the pseudo-element viewpoint, and they are still not satisfactory for large-scale circuits.

In Chapter 2, the useful theories for the proposed methods are introduced. Firstly, the commonly used numerical integration algorithms are reviewed. Secondly, the numerical damping effect is introduced, which is used to solve the oscillation problem in PTA. After that, three conventional time-step control methods, including LTE, iteration count, and SER methods, are reviewed. Finally, the convergence of PTA techniques is introduced.

In Chapter 3, a PTA method using numerical integration algorithms with artificial damping is proposed. In section 3.1, the details of conventional PTA studies are presented. Conventional pure PTA methods limit to the oscillation problem caused by pure pseudo-elements, while CEPTA sometimes fails to find the DC solution due to the discontinuous problem. Moreover, all these methods sometimes fail to obtain the DC operating point for some large-scale and complex circuits and the efficiency such as CPU time, steps and iterations is still not satisfactory. All the previous studies are from the pseudo element viewpoint. Thus, in section 3.2, to address these issues from the different viewpoint (numerical integration algorithm viewpoint), a PTA method using the k-step damped differentiation formulas (DDF-k) with artificial damping effect is proposed. The proposed method artificially enlarges the damping effect in the numerical integration algorithms to weaken the oscillation. Besides, capacitors are used only as the pseudo-elements so that the proposed DPTA method has no discontinuous problem. Therefore, discontinuous problem and oscillation problem can be solved at the same time.

Moreover, the proposed numerical methods are proved to be convergent by considering the consistency and stability in section 3.2. Furthermore, an effective switching algorithm for the DPTA method is proposed to improve the convergence and efficiency. It can automatically change among the different numerical integration algorithms to obtain varying degrees of damping effect. The proposed methods are implemented in our Waseda Spice and verified by large-scale complex circuits. In section 3.3, numerical examples and result comparisons are shown. With the proposed DPTA method, 100% test circuits in INOUE Lab. are solved (62/62). Compared with conventional PTA methods, DPTA has $0.81X \sim 4.79X$ speedup of CPU time. Among them, using DPTA for the practical and large-scale circuit (1516 MOSFETs), the CPU time has 4.79X speedup, and the number of NR iterations is reduced to 18.03% of the iterations by using CEPTA.

In Chapter 4, the adaptive time-step control method applied to DPTA is proposed. The conventional time-step control method does not fully consider the convergence of NR. Besides, it does not try to take the time-step size as large as possible. These two features may have some fatal problems when the control parameters of the time-step control method are not chosen carefully. Therefore, in section 4.2, based on the idea of SER method, an enhanced time-step control method is proposed, which can improve the robustness of DPTA. The proposed method can automatically and intelligently adapt the time-step size according to the predict of circuit state at each step. The new control algorithm is capable to adapt the time-step size without constant upper limit, so that it can obtain the damping effect as large as possible. Moreover, the proposed method has a wider applicability to the pseudo-capacitor value, since it can automatically and effectively adapt the time-step size according to the circuit state during the simulation. In section 4.3, the numerical examples demonstrate the efficiency improvement of DPTA by using the proposed time-step control method. Compared with conventional DPTA, the proposed method has $0.86X \sim 104.82X$ speedup of CPU time.

Compared with conventional SER, the proposed method has $1.22X \sim 76.34X$ speedup of CPU time. It is also proved that, DPTA with the proposed time-step control method has the ability to 100% solve all test circuits in INOUE Lab. and the benchmark circuits (113/113). Moreover, the robustness of DPTA is enhanced. Compared with other time-step control methods, the proposed method can expand the range of capacitor value used in the pseudo-element.

In Chapter 5, the conclusions and future works are given.

With these two proposed methods, the oscillation problem of PTA technique is solved. Compared with other algorithms for solving nonlinear DC circuit equations, the DPTA method with the adaptive time-step control method can solve the complex and large-scale circuits efficiently. Moreover, the robustness of the proposed methods is better than other PTA methods. In this research, the goal of finding a practical algorithm to solve all challenges is achieved.

5.2   Future Works

As mentioned before, the PTA techniques are not globally convergent. There might be some other circuits, which cannot be solved by the proposed methods. Therefore, much more circuits will be tested to find the problems of two proposed methods.

Secondly, the robustness of PTA is still a big challenge. There are 20+ algorithm control parameters which need to be defined. The proposed time-step control method can automatically adapt the time-step size, which means that the users do not need to define the time-step control parameters. However, there are still 10+ parameters need to be considered. In the future, the large data analysis, data mining methods, and deep learning algorithms will be used to analyze the

connection between these parameters. In addition, more adaptive control methods will be proposed.

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