早稲田大学大学院情報生産システム研究科

博 士 論 文 概 要

論　文　題　目

Study on Low Voltage and Low Power CMOS Voltage Reference Circuits without Resistors

申　請　者
Jing WANG

情報生産システム工学専攻
ディペンダブル情報システム研究

2017 年　7　月

System on chip (SoC) is widely used in portable device markets nowadays. Voltage reference generators are ubiquitous in the SoC design areas, in which the output voltages exhibit little dependence on process and supply voltage variations. They are important parts for accurate working of various circuits like ADC (Analog-to-Digital Converter), DAC (Digital-to-Analog Converter), PLL's, DC-DC converters, and oscillators. Thus, a precision voltage reference forms an integral part of almost all circuit designs. There are mainly two kinds of voltage reference circuits: PTAT (Proportional to Absolute Temperature)/CTAT (Complementary to Absolute Temperature) voltage references, which are sometimes applied as temperature sensors; and voltage reference totally independent of temperature (famous for bandgap reference circuits), which is widely applied whenever an on-chip reference bias is needed.

Low power designs are required for portable device markets implementation. The scaling of complementary metal oxide-semiconductor (CMOS) process technology also increases the requirement for low voltage design. On the other hand, although resistor is available to be implemented in analog CMOS process, the area in standard digital process is greatly increased. The reason is that, the sheet resistance of the diffusion layers and polysilicon is reduced by using silicide. By applying resistors in digital process both increase the cost and circuit susceptibility to the substrate noise coupling. To overcome these problems, on way is to add an extra mask. Although it is capable to selectively block the silicide, the cost is also increased. In another way, to design circuits without resistors is becoming more and more popular to solve this problem nowadays. Therefore, ultra-low-power, low voltage and resistor-less have become key characteristics for circuit design but there are still challenges for high performance under different conditions. For PTAT/CTAT voltage generators which are widely used as temperature sensors, several dozens of them are placed on chip at different positions, the power consumptions themselves should be designed much smaller. For bandgap reference circuits, the minimum supply voltage limits the total supply voltage of the system on chip, which needs to be further reduced in this field.

For conventional PTAT/CTAT voltage reference generator design, one of the conventional V_{th} extractor in (S. Vlassis, ElectronLett2007) was proposed. This circuit extracts the unit output V_{th} voltage. However, power consumption is between 50 uW and 65 uW and resistors are also used. Another research in (G. Fikos, TCASII2001) reduced the power and designed without resistors.

However, the minimum power consumption is 1.14 uW, which still microwatt level. Moreover, both of these circuits above only generate unit output V_{th} voltages. A paper (Z. Wang, JSSC1992) proposed the circuits to generate the n times V_{th} output value. However, the output n should be an integer number, which is discrete. This limits the circuit application. Moreover, the circuit (Z. Wang, JSSC1992) is not low power or resistor-less design.

For conventional reference circuits independent of temperature, the famous classical bandgap reference circuits were proposed by Widlar in (R.J. Widlar, JSSC1971), and modified by Brokaw in (A.P. Brokaw, JSSC1974). After these classical circuits, the minimum supply voltage V_{DD} of the bandgap reference circuit is reduced firstly in (H. Banba, JSSC1999) to 0.84 V, using resistor dividers. However, all these works must use resistors. A CMOS bandgap reference circuit without resistors was firstly published in (A. Buck, ISSCC2000). However, the circuit has a very high supply voltage of 3.7 V, and the temperature coefficients is large (119.7 ppm/C°). The reduction of minimum supply voltage and improvement temperature accuracy have not been totally solved yet.

Based on the above considerations and limitations of previous researches, a nano-level power CTAT generator of V_{th} extractor and a high accuracy sub-1-V bandgap reference circuit that both without resistors are proposed in this dissertation, respectively. The ultra-low-power design for CTAT reference circuit is based on the technique of controlling the overdrive voltage which is only determined by the design parameter (*WL* sizes). The low voltage design for bandgap reference circuit is realized based on the principle of reducing the output voltage (usually around 1.2 V) using a CMOS voltage divider; and the output accuracy is improved by a new current source. To help verifying analog circuit performance, a simple and practical statistical analysis device model is proposed to simulate the process variation before chip design.

The dissertation is organized with five chapters as follows:

In chapter 1, the application backgrounds and requirements are briefly introduced. Then the motivations and objective of the dissertation and research approach are presented. Finally, contributions of this work and its organization are shown.

In chapter 2, a simple and practical statistical analysis device model for analog circuit design is proposed. A method is given combining global and local variations together using 4 model parameters. It is available in prediction of circuit performance considering process variation. This model is used for the circuits statistical variation simulation proposed in chapter 3 and chapter 4.

In chapter 3, an accurate nanowatt supply-insensitive CMOS unit V_{th} extractor and a low power α times V_{th} (αV_{th}) extractor with continuous variety (CTAT reference voltage circuits) are proposed by controlling the overdrive voltage. The technique is controlling the overdrive voltage V_{ov} by changing transistor sizes. With the αV_{th} extractors, both incremental and decremental αV_{th} voltages are obtained by simply adjusting the transistor size. For the simulation results of 0.18 um process, the power consumption is 265 nW and line regulation is 0.027%/V for the unit V_{th} extractor; for the αV_{th} extractor, the power consumption is realized from microwatt to nanowatt, and line regulation is 0.146%/V. The measurement results are also discussed in the end of this chapter. The line regulation is about 0.5%/V for unit V_{th} extractor, which is worse than simulation result, caused by large output impedance and unstable measurement environment. The minimum power consumption is 432 nW, which is same nano-level low power result. Besides being used as temperature sensors, the CTAT reference voltage circuit is capable to be applied as a part of bandgap reference circuit in chapter 4.

In chapter 4, an under 1 V CMOS only bandgap reference circuit without resistors is proposed. The improvements of the proposed circuit are shown as follows: Firstly, the performance of sub-1-V supply voltage is realized by utilizing a voltage divider. Secondly, the temperature coefficient is improved by a current source with approximately linear negative temperature dependence. Its temperature dependence is compensated by only adjusting the *W/L* ratios of the two differential pairs in the bandgap reference circuit.

Simulation results show that the output reference voltage is around 0.5 V with a minimum supply voltage of 0.85 V. Moreover, the temperature coefficient is only 3.5 ppm/ C° from 0 C° to 70 C°. In high accuracy resistor-less design area, the supply voltage of 0.85 V is the state-of-the-art performance. The measurement results are also discussed in the end of this chapter with the minimum supply voltage of 0.85 V and 4.9 ppm/ C° temperature coefficient, which have a good agreement with the simulation results. For chip variation distribution, the mean value of temperature coefficient variation between different chips is 7.37 ppm/C°, and deviation σ is 8.9 ppm/C°. The conclusion is that the proposed bandgap reference circuit has ability to work with high accuracy under 0.85 V supply voltage.

In chapter 5, the conclusions of this dissertation are given.