Waseda University Doctoral Dissertation

Study on Low Voltage and Low Power CMOS Voltage Reference Circuits without Resistors

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December 2017

Abstract

System on chip (SoC) is widely used in portable device markets nowadays. Voltage reference generators are ubiquitous in the SoC design areas, in which the output voltages exhibit little dependence on process and supply voltage variations. They are important parts for accurate working of various circuits like ADC (Analog-to-Digital Converter), DAC (Digital-to-Analog Converter), PLL (Phase Locked Loop), DC-DC converter, and oscillator. Thus, a precision reference voltage forms an important part of almost all circuit designs. There are mainly two kinds of voltage reference circuits: PTAT (Proportional to Absolute Temperature)/CTAT (Complementary to Absolute Temperature) voltage reference generators, which are sometimes applied as temperature sensors; and voltage reference generators totally independent of temperature (famous for bandgap reference circuits/BGR circuits), which is widely applied whenever an on-chip reference bias is needed.

Low power designs are required for portable device markets implementation. The scaling of complementary metal oxide-semiconductor (CMOS) process technology also increases the requirement for low voltage design. On the other hand, although resistors are available to be implemented in analog CMOS process, the area in standard digital process is greatly increased. The reason is that, the sheet resistance of the diffusion layers and polysilicon is reduced by using silicide. By applying resistors in digital process both increases the cost and circuit susceptibility to the substrate noise coupling. To overcome these problems, one way is to add an extra mask. Although it is capable to selectively block the silicide, the cost is also increased. In another way, to design circuits without resistors is becoming more and more popular to solve this problem nowadays. Therefore, ultra-low-power, low voltage and resistor-less have become key characteristics for circuit

design but there are still challenges for high performance under different conditions. For PTAT/CTAT voltage generators which are widely used as temperature sensors, several dozens of them are placed on chip at different positions, the power consumptions themselves should be designed much smaller. For bandgap voltage reference circuits, the minimum supply voltage limits the total supply voltage of the system on chip, which needs to be further reduced in this field.

For conventional PTAT/CTAT voltage reference generator design, one of the conventional V_{th} (threshold voltage) extractor in ElectronLett2007 [1] was proposed. This circuit extracts the unit output V_{th} voltage. However, power consumption is between 50 uW and 65 uW and resistors are also used. Another research in TCASII2001 [2] reduced the power and designed without resistors. However, the minimum power consumption is 1.14 uW, which is still microwatt level. Moreover, both of these circuits above only generate unit output V_{th} voltages. A paper published in JSSC1992 [3] proposed the circuits to generate the n times V_{th} output value. However, the output n should be an integer number, which is discrete. This limits the circuit application. Moreover, the JSSC1992 [3] circuit is not low power design.

For conventional reference circuits independent of temperature, the famous classical bandgap reference circuit was proposed by Widlar in JSSC1971 [4], and modified by Brokaw in JSSC1974 [5]. After these classical circuits, the minimum supply voltage V_{DD} of the bandgap reference circuit is firstly reduced to 0.84 V in JSSC1999 [6]. However, all these works use resistors. A CMOS bandgap reference circuit without resistors was firstly published in ISSCC2000 [7]. However, the circuit has a very high supply voltage of 3.7 V, and the temperature coefficients is large (119.7 ppm/C°). The reduction of minimum supply voltage and realization of low temperature coefficient have not been

totally solved yet.

Based on the above considerations and limitations of previous researches, a nanopower CTAT generator of V_{th} extractor and a low temperature coefficient sub-1-V bandgap reference circuit that both without resistors are proposed in this dissertation, respectively. The ultra-low-power design for CTAT reference circuit is based on the technique of controlling the overdrive voltage which is only determined by the design parameter (*WL* sizes). The low voltage design for bandgap reference circuit is realized based on the principle of reducing the output voltage (usually around 1.2 V) using a CMOS voltage divider; and the output temperature dependence is improved by a new current source. To help verifying analog circuit performance, a simple and practical statistical analysis device model is proposed to simulate the process variation before chip design.

The dissertation is organized with five chapters as follows:

In Chapter 1, the application backgrounds and requirements are briefly introduced. Then the motivations and objective of the dissertation together with the research approach are presented. Finally, contributions of this work and its organization are shown.

In Chapter 2, a simple and practical statistical analysis device model for analog circuit design is proposed. A method is given combining global and local variations together using 4 model parameters. It is capable in prediction of circuit performance considering process variation. This model is used for the circuits statistical variation simulation proposed in Chapter 3 and Chapter 4.

In Chapter 3, an accurate nano-Watt supply-insensitive CMOS unit V_{th} extractor and a low power α times V_{th} (αV_{th}) extractor with continuous variety (CTAT reference voltage circuits) are proposed. The proposed circuits are using only CMOS transistors

working in strong inversion region. The technique is controlling the overdrive voltage V_{ov} by changing transistor sizes. For the αV_{th} extractors, both incremental and decremental αV_{th} voltages are obtained by simply adjusting the transistor sizes. Both simulation and chip measurement are done based on a 0.18 um process. The simulation results show that, for the unit V_{th} extractor, the power consumption is 265 nW, which is approximately 1/5 of that in TCASII2001 [2] and 1/200 of that in ElectronLett2007 [1]. Supply voltage dependence is 0.027%/V, which is approximately 5 times smaller than the results in both ElectronLett2007 [1] and TCASII2001 [2]. For the αV_{th} extractor, the power consumption is realized from micro-Watt to nano-Watt, and supply voltage dependence is 0.146%/V. It realizes continuous α times V_{th} generation that JSSC1992 [3] is not capable to obtain. The measurement results are also discussed in the end of this chapter. The supply voltage dependence is about 1.57%/V for unit V_{th} extractor, which is worse than the simulation result, mainly caused by large output impedance and unstable measurement environment. The minimum power consumption is 432 nW, which is the same nano-level as the simulation result. Thus, the proposed V_{th} extractor circuits both realize nano-level power consumption and continuous varying.

In Chapter 4, a sub-1-V CMOS bandgap reference circuit without resistors is proposed. The proposed circuit is designed with only CMOS transistors. Comparing with previous design without resistors, the proposed circuit utilizes a CMOS voltage divider and a CTAT CMOS current source. The performance of sub-1-V supply voltage is realized by reducing the output voltage. The low temperature coefficient is realized by reducing the current source temperature dependence. Simulation results of 0.18 um process show that the output reference voltage is around 0.5 V with a minimum supply voltage of 0.85 V, which is smaller than that in ISSCC2000 [7]. Also, this 0.85 V supply voltage is

realized without resistors comparing with JSSC1999 [6]. Moreover, the temperature coefficient of the output voltage is only 3.5 ppm/°C from 0°C to 70°C. In low temperature coefficient resistor-less design area, the supply voltage of 0.85 V is the state-of-the-art performance. The measurement results are also discussed in the end of this chapter with the minimum supply voltage of 0.85 V and 4.9 ppm/°C temperature coefficient, which have a good agreement with the simulation results and smaller than the measurement results in ISSCC2000 [7]. For chip variation distribution, the mean value of temperature coefficient variation between different chips is 8.54 ppm/°C, and standard deviation σ is 8.9 ppm/°C. The conclusion is that the proposed bandgap reference circuit has ability to work with low temperature coefficient under 0.85 V supply voltage.

In Chapter 5, the conclusions of this dissertation are given.

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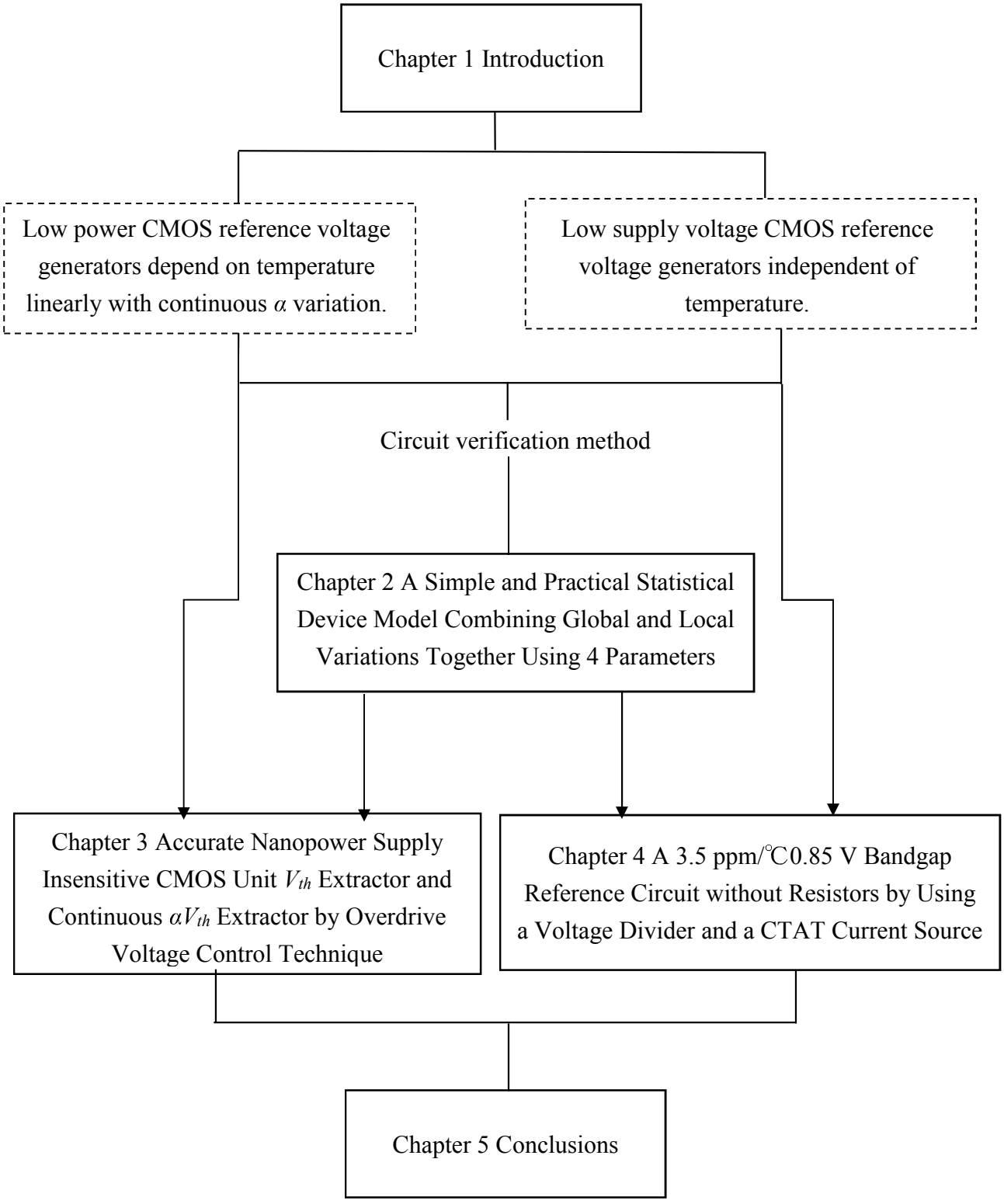


Dissertation Organization

1 Introduction

1.1 Backgrounds of voltage reference voltage generators

1.1.1 What are voltage reference generators?

Voltage reference generators are the circuits provide the voltage that is independent of PVT (process, supply voltage and temperature) characteristics, load and packaging stresses [4]. There are mainly two kinds of reference voltage generators [4][8], which are widely used.

One kind of the reference voltages is totally independent of temperature like bandgap reference circuits [4]. It is realized by two independent physical phenomena that have opposite temperature dependences. The other kind of reference voltages are dependent on the temperature linearly, like PTAT (Proportional to Absolute Temperature)/CTAT (Complementary to Absolute Temperature) voltage references, which are sometimes applied as temperature sensors [8]. Some are designed based on the principle of the thermal voltage temperature characteristics [9]; some are based on the threshold voltage temperature characteristics [1]-[3].

For the bandgap reference circuit, the output voltage temperature dependence should be minimized, while for the output voltage of temperature sensor, it should be maximized.

1.1.2 Applications and requirements

Integrated on-chip voltage reference is one of the fundamental blocks of electronic systems, and has been studied as an important topic in the past few years [4]-[21]. Voltage references are fundamental parts of most systems and electronic circuits.

They are widely used in analog, radio-frequency, mixed-signal and even digital circuits such as ADC (Analog-to-Digital Converter) a (Digital-to-Analog Converter), and the accuracy requirement varies across the different application domains [4]-[21].

The bandgap voltage reference generator is widely applied whenever a reference bias is needed intra-chip like SoC. For example, in a microprofessor integrated by a modern System on Chip (SoC), the bandgap voltage reference generator provides local references for comparators or biasing.

For the application of PTAT/CTAT voltage reference generators, temperature management circuits have also been used for many years in systems such as ovens, air conditioners and engines [9][22]-[24]. Today temperature sensors (based on PTAT/CTAT voltage references) a

.

1.1.3 Technology trend

The fully integrated complementary metal oxide-semiconductor (CMOS) technology is playing a more and more important role nowadays. In practical design, small size and low cost are needed [7][26].

1.1.4 Challenges

Low power design is becoming a critical demand in circuit designs, to continuously expand markets for devices such as portable devices, wireless sensor nodes, and implantable medical devices [22][23]. Due to the power saving, high density and low costs, CMOS has become the predominant technology in integrated circuit designs [7]. Moreover, although resistors are available to be implemented in analog CMOS process, the area in standard digital process is greatly increased. The reason is that, the sheet resistance of the diffusion layers and polysilicon is reduced by using silicide [7]. By applying resistors in digital process both increase the cost and circuit susceptibility of the reference operation to the substrate noise coupling [7]. To overcome these problems, one way is to add an extra mask [7]. Although it is capable to selectively block the silicide, the cost is also increased. In this case, to design circuits without resistors is becoming more and more popular to solve this problem nowadays [7][10].

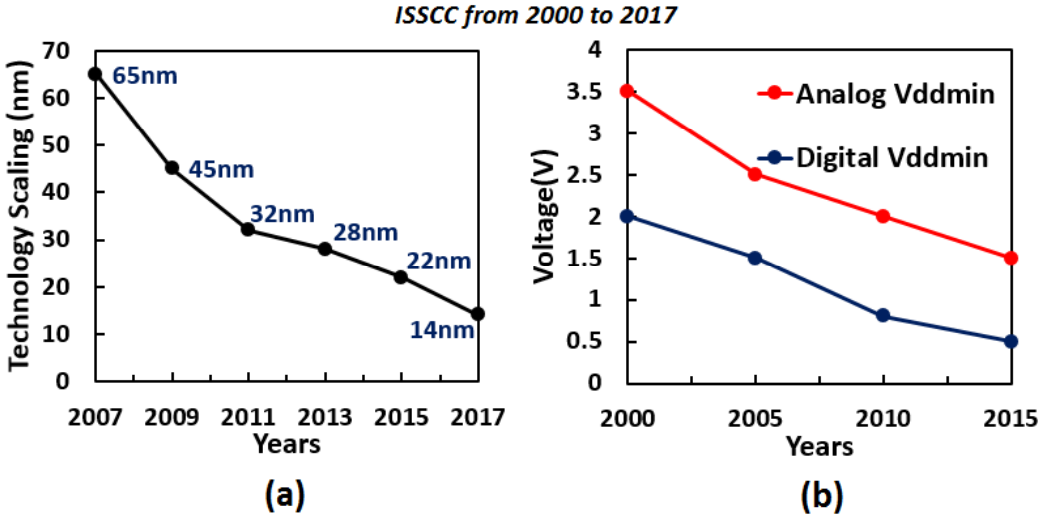


Fig. 1.1: (a) The scaling trend of CMOS technology. (b) Supply voltages trend of CMOS technology.

On the other hand, low voltage design requirement increases recently in Fig. 1.1 (b) . The main driving factor for low voltage operation is the scaling of process technologies as shown in Fig. 1.1 (a). Data in Fig. 1.1 are collected from ISSCC papers during 2000 to 2017.

Therefore, ultra-low-power and low voltage have become key characteristics for circuit designs. However, there are still challenges for high accuracy design in modern CMOS technologies under this condition. The traditional designs are not suitable, for the output bandgap reference voltages are above one volt. Moreover, to realize low power consumption, resistors with large resistance are required that occupy a huge silicon area. Recent advances have achieved low power consumption but with limited accuracy, large silicon area, and expensive calibration [20][21].

In addition, as scaling of CMOS technology, device parameter variations become larger. Both global and local variation influences increase [27].

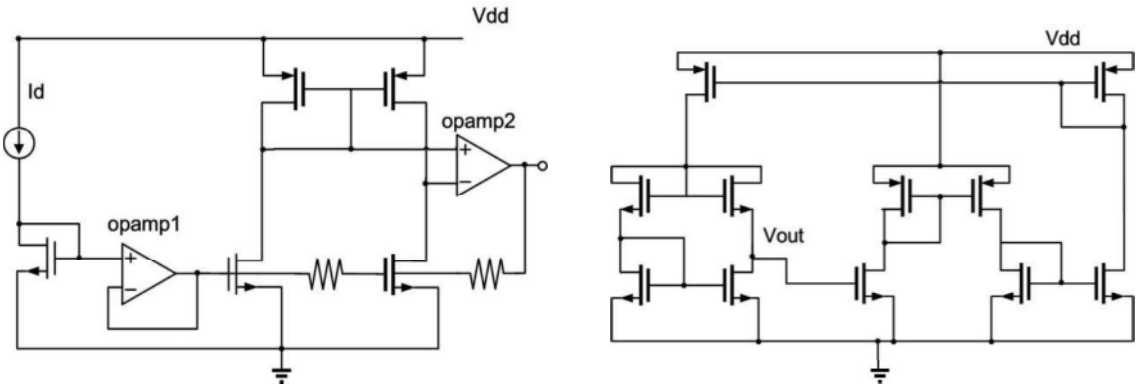
In this case, low supply voltage, low power design capable to achieve a small chip size with low temperature coefficient output becomes more and more important nowadays [6][8][11][16][20][21]. Therefore, the topics of this dissertation are focusing on improving low-supply voltage and low-power design techniques.

1.2 Conventional researches

1.2.1 Conventional PTAT/CTAT generators

PTAT/CTAT reference circuits usually generates linear temperature dependent output voltage by threshold voltage or thermal voltage [1][2]. For low power PTAT/CTAT generators design, one of the conventional V_{th} extractor is shown in Fig. 1.2

(a) [1]. The circuit is designed using resistors [1]. The current consumption is between 50 uA and 65 uA when the supply voltage is between 1 V and 3.6 V, respectively. Both the power consumption and supply voltage dependence are not small. Moreover, resistors are used that limits its application and costs large chip area.



(a) Low voltage unit V_{th} extractor [1].

(b) Low voltage and low power unit V_{th} extractor without resistors [2].

Fig. 1.2: Low power PTAT/CTAT generators without resistors.

Another circuit as shown in Fig. 1.2 (b) is realized by combining a simple low voltage V_{th} extracting block and novel feedback without resistors [2]. The power consumption is 1.14 uW, with the 0.1%/V supply voltage dependence at room temperature.

Even these two circuits are low power design, the power consumptions are still microwatt level. Moreover, both of the voltage outputs extract only unit V_{th} voltage.

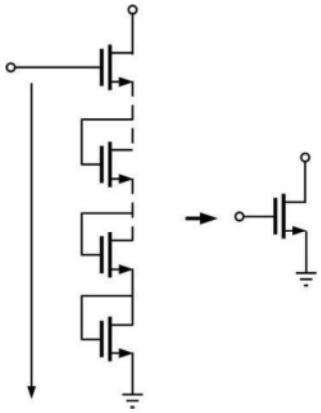


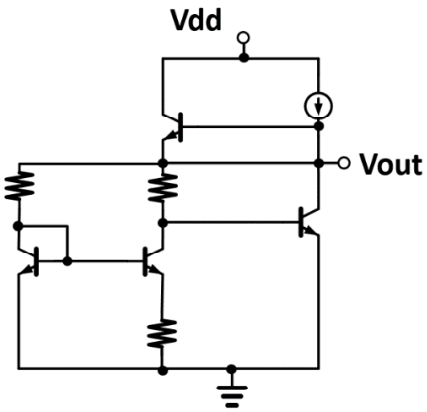
Fig. 1.3: N times V_{th} extractor circuit in [3].

In Fig. 1.3, the V_{th} extractor was proposed, which has the ability to generate N time output V_{th} voltage [3]. Two types of V_{th} extractors were presented: one is incremental and the other is decremental. An $n*n^2$ transistor array was presented to realize $V_{out}=NV_{th}$ [3]. Thus, the output voltage is easily used with a wide range of application, like level shifting, temperature compensation, and centigrade sensors for temperature measurement. The V_{th} value is changing by integer values. However, this integer changing limits the application. Moreover, in this circuit, low power design is not considered.

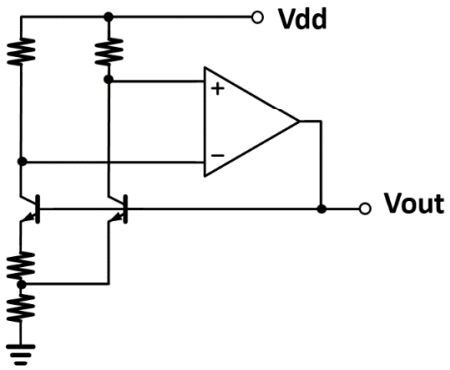
1.2.2 Conventional bandgap reference circuits

In the history of bandgap reference circuits design, one of the classical circuits is the Widlar bandgap reference circuit in Fig. 1.4 (a) in 1971 [4]. It uses the BJT (Bipolar Junction Transistors) to obtain the PVT independent output voltage (1.22 V). The limitation is that the output is not easy to control. To solve this problem, another classical bandgap reference circuit was proposed by Brokaw in 1974 shown in Fig 1.4 (b) [5]. The circuit contains two BJTs, where the collector current sensor is used to realize the bandgap reference output voltage. However, both of these classical circuits need high supply

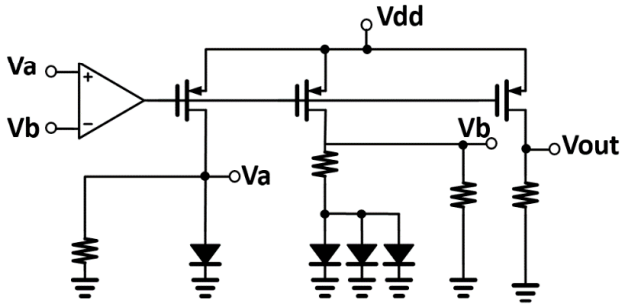
voltage. To meet the low supply voltage requirement, a sub-1-V bandgap reference circuit was proposed in Fig. 1.4 (c), by adjusting the output reference voltage value using resistors [6].



(a) W .



(b) Brokaw bandgap reference circuit [5].



(c) Sub-1-V bandgap reference circuit [6].

Fig. 1.4: The classical bandgap reference circuits with resistors.

On the other hand, the demand of resistor-less design is also increasing to meet today's requirements. A well-known CMOS bandgap reference circuit was proposed [7]

based on the similar bandgap reference principle [4][5]. Figure 1.5 shows the structure of the circuit in [7]. It is composed of two diodes, a current source, a voltage to current transconductor, a current to voltage transresistor and a current feedback. By this structure, this circuit successfully realized the bandgap reference circuit design without resistors. However, this circuit has a limitation of very high supply voltage (3.7 V), for the output voltage is around 1.2 V. Another limitation of this BGR circuit is that, the temperature dependence of the current source influences the reference voltage greatly. The output reference voltage temperature coefficient is reported 119.7 ppm/C°, which is not small enough for low temperature coefficient requirement.

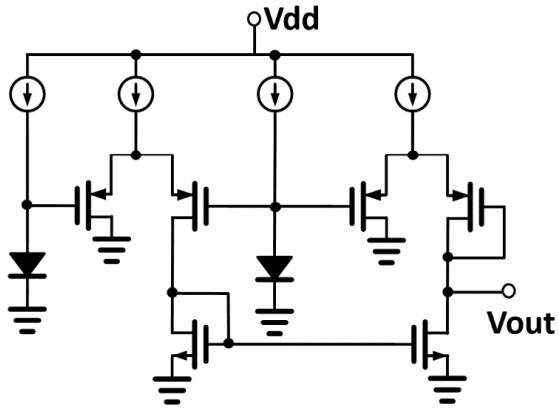


Fig. 1.5: The CMOS bandgap reference circuit without resistors in [7].

1.3 Motivation and research objective

Based on the motivation mentioned above, the research objectives are discussed. The aims are to solve the limitations of conventional works and to meet requirements of low power, and low supply voltage. The objectives are listed as below:

1. A CTAT voltage reference, which is based on the threshold voltage extractor of NMOS transistors is designed. The power consumption is nano-Watt without resistors,

and the supply voltage dependence is modified comparing with conventional works. Moreover, not only unit V_{th}, but also continuously changing V_{th} output value is generated. This output is capable to be applied directly to other circuits without Op-Amp.

2. A CMOS bandgap reference circuit without resistors is designed. The minimum supply voltage is reduced by using a CMOS voltage divider between two differential pairs. Moreover, both temperature coefficient and supply voltage dependence are reduced by a new current source, which has a negative temperature dependence. Its temperature coefficient is compensated by only adjusting *W/L* ratios of two differential pairs.

To design more accurately before making chips, a simple statistical model to simulate the process variation is also proposed.

1.4 Research approach

1.4.1 Common targets

As introduced before, on one hand, low power and low voltage design for voltage reference generators is required. For PTAT/CTAT voltage generators which were used as temperature sensors, several dozens of them are used on chip at different positions. The power consumptions itself should be designed much smaller. For bandgap reference circuits, the minimum supply voltage limits the total supply voltage of the system on chip. On the other hand, to reduce area and to integrate with digital ICs, design of CMOS reference voltage generators without resistors is also needed.

Based on these requirements, the targets of reference voltage generator designs are

shown below.

For the PTAT/CTAT voltage generator:

1. Use only CMOS technology without resistors.
2. Nano-Watt power consumption design.
3. Unit and α (continuously varying) times all-in-one without further Op-Amps.
4. Exactly follow temperature dependence of V_{th} parameter.
5. Supply voltage insensitive.

For the bandgap voltage reference generator:

1. Use only CMOS technology without resistors.
2. Reduce minimum supply voltage, for its supply voltage affects the minimum supply voltage of total SoC.
3. Low temperature coefficient by modifying current source temperature dependence.

These targets are realized in the proposed circuits in Chapter 3 and Chapter 4.

For designers to verify the performance variation due to the device parameter variations, the targets of the statistical device model are simple and practically accurate.

1.4.2 Methods

Both of the proposed circuits are designed without resistors. The design is based on the principle of transforming current to voltage and voltage to current using MOS transistors only.

To realize low power design for PTAT/CTAT voltage generators, the method of reducing overdrive voltage, which is controlled by the design parameter (WL sizes) of the

proposed circuit, is used. Also, long channel length transistors are applied. Based on this technique, the overdrive voltage model is proposed and careful tradeoff is discussed among mismatch, noise, power consumption and area.

To reduce the minimum supply voltage for bandgap reference circuit, the technique of reducing the output voltage is used. A new structure is designed to realize it.

To reduce the temperature coefficient, for the bandgap reference circuit, the method is reducing the current source temperature dependence influence. The aim is to use a CTAT current source instead of to use an ideal one. For CTAT voltage generator, the method is to make the circuit MOS transistors fit long channel model well, by controlling the overdrive voltage value. This method gives enough margin of overdrive voltage to make the temperature coefficient small even in high temperature range.

For the supply voltage dependence, both of the two proposed circuits are applying long channel MOS transistors to reduce DIBL (Drain-induced Barrier Lowering) so that the supply sensitivity is reduced. For CTAT voltage generator, another method to reduce it is to compensate the overdrive voltage mismatch of MOS transistors each other. Thus, the output voltage has small variation when the supply voltage changes.

A method to build statistical analysis device model is also proposed. Because that, the influence of CMOS process variation on analog circuit performance is more and more apparent. Therefore, modeling the process variation for analog circuits accurately is helpful to the circuit designers. The traditional worst-case analysis is too pessimistic to be widely used in analog circuits designs. Then a statistical analysis device model is given to do Monte Carlo analysis of the proposed reference voltage circuits, and the generated performance distribution reflects the influence of process variation well. The proposed statistical analysis model building is simple and practical. It only costs little time and

money.

1.5 Contributions of this work and its organization

As described above, reference voltage generators play a very important role in LSI circuit designs. The challenge nowadays is the low supply voltage and low power designs. On the other hand, to reduce the cost of large area, CMOS reference voltage generator without resistors is also required.

This dissertation includes two proposed reference voltage generators without resistors, which solve different issues. For CMOS V_{th} extractor., which is one kind of PTAT/CTAT reference voltage generators, the power consumption is several dozen to hundred microwatt level of conventional work. In this dissertation, the proposed V_{th} extractor is nanowatt level power consumption, with reduced supply voltage dependence. For CMOS bandgap reference circuits, the minimum supply voltages of previous researches are large. The reason is that the output reference voltage is around 1.25 V. Moreover, the conventional CMOS bandgap reference circuit without resistors has hundreds ppm/C° temperature coefficient, which is mainly caused by the temperature dependence of the current source used in the reference circuit. In this dissertation, the minimum supply voltage is reduced to 0.85 V by reducing the reference voltage. At the same time, the temperature coefficient is also reduced to 3.5 ppm/C°, by using a newly designed current source. Moreover, a simple and practical statistical analysis model is proposed in this dissertation. It is used for simulation the variation of the proposed reference voltage generators together with a circuit simulator.

The organization of this dissertation is shown as follows:

In Chapter 2, a simple and practical statistical analysis device model for circuit

design is proposed. The proposed simple statistical device model is capable to be used for analog circuit process variation simulation. It is also very simple so that easily to be applied for practical circuit designs. In this case, the cost of chip design is greatly reduced.

In Chapter 3, accurate nanopower supply-insensitive CMOS unit V_{th} extractor and αV_{th} extractor with continuous variety are proposed. The proposed threshold voltage extractor has the merits. Firstly, the circuits are designed without resistors. Secondly, the power consumption is reduced to nanowatt level. Thirdly, the circuit obtains not only V_{th} value but also αV_{th} value. Fourthly, the αV_{th} is capable to be changed continuously for different applications.

In Chapter 4, a 3.5 ppm/C° 0.85 V bandgap reference circuit without resistors is proposed. The proposed bandgap reference circuit has the merits. Firstly, the circuit is designed without resistors. Secondly, the minimum supply voltage is reduced to within 1 V. Thirdly, the temperature coefficient of the output reference voltage is greatly improved by reducing the temperature dependence of the current source.

2 A Simple and Practical Statistical Device Model for Analog LSI Designs

2.1 Introduction

As the feature size of CMOS devices scales down, the process variation imposed by each process step increases inversely [27][28]. As a result, this increasing process variation has become a critical factor in both analog integrated circuit (IC) design and manufacturing [29][30].

Process variation can be classified into two categories depending on their physical range on a chip or a wafer [31]:

- Global variation which is sometimes called inter-chip variation accounts for the total variation in the value of a component over different chips, wafers or batches.
- Local variation or mismatch which is sometimes called intra-chip variation reflects the variation in a component value with reference to an adjacent component on the same chip.

Presently, with the development of analog integrated circuits, CAD simulators with the SPICE as the core is not capable to do statistical analysis directly according to process variation and also not capable to predict the performance of analog LSI accurately. Therefore, building a statistical device model library and then using the Monte Carlo method to do statistical analysis for analog LSI are useful [32]-[34].

The typical viewpoint about mismatch was presented in Pelgrom's model [35] in which he gave a general mismatch law that the mismatch of pair transistors is inversely proportional to the square root of device area. However, without considering the global variation, the statistical device model is not capable to reflect the practical variation accurately. Some conventional complicated statistical device models including the global variation and the local variation are accurate. However, the construction of these models is not easy. For example, the references [36]-[38] need to extract all BSIM parameters which are difficult and time-consuming in practical applications. Nowadays, the commonly used BSIM3v3 model has more than 100 parameters [39]. If using the conventional complicated statistical device models, the extraction of all parameters will be horrible. Thus, some researchers proposed simple statistical analysis models which only contain a small number of parameters. A simple model in [40] was used to represent each main component by Gaussian distribution according to corner information. However, that simple model is not accurate enough to reflect variations of practical analog LSI.

Therefore, a simple and practical statistical device model for analog LSI designs is proposed in this chapter. In the proposed model, the global variation considering parameter correlations is specially researched and the local variation is also included. Based on practical chip measurement data, a simple method is introduced to extract a small number of model parameters. Meanwhile, the proposed model is applied to build statistical device model library and do statistical analysis of practical Op-Amp circuit using Monte Carlo analysis under HSPICE environment without additional software. The statistical analysis results have a good agreement with practical chip measurement results.

The rest of this chapter is composed of four parts as follows. Firstly, how to model the process variation is proposed in 2.2. Then model parameter extraction and

measurement results are shown in 2.3. In 2.4, the relationship with Chapter 3 and Chapter 4 is discussed. Finally, the paper is concluded in 2.5.

2.2 Model the process variations

In this section, how to construct the proposed statistical analysis device model is introduced.

2.2.1 The composition of the model parameter

Process variation is composed of two parts: global variation [Fig. 2.1 (a)] and local variation [Fig. 2.1 (b)]. Global variation affects all the devices on the same chip in the same way, e.g., causing the transistor gate lengths of devices on the same chip to be all la

.g., causing some devices have smaller transistor gate lengths and others larger transistor gate lengths than the nominal [41].

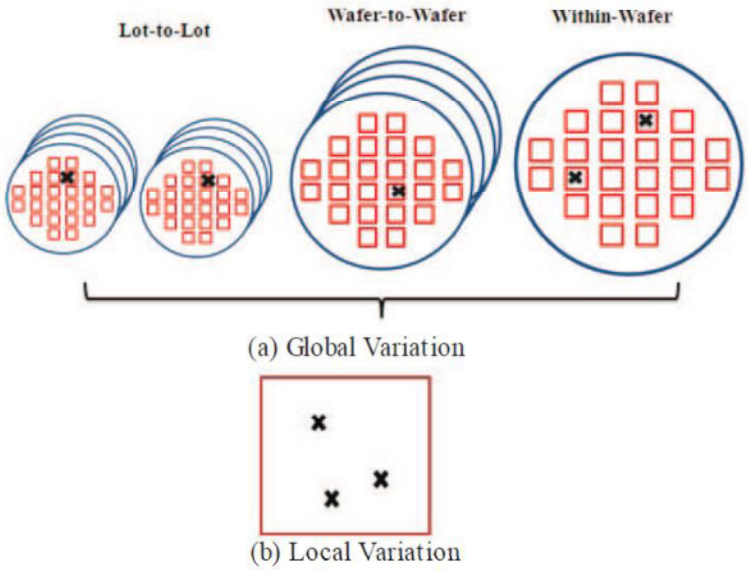


Fig. 2.1: Global and local variations of process variation.

The total value of parameters in the proposed model is composed of three parts: the typical value, the global variation and the local variation. Thus, the parameter P for a MOS transistor is expressed as blow:

$$P_{total} = P_{typ} + \Delta P_G + \Delta P_L, \quad (1)$$

where P_{total} is the total value of the parameter P, P_{typ} is the typical value of the parameter P, ΔP_G is the deviation imposed by global variation for the parameter P and ΔP_L is deviation imposed by the local variation for the parameter P.

In the proposed model, the deviation of global variation for MOS transistors is regarded as following the Gaussian distribution and the deviation of local variation for MOS transistors is also regarded as following the Gaussian distribution. Then the deviation of global and local variation in Eq. (1) is expressed specifically as:

$$\Delta P_G \sim N\left(o, \sigma(\Delta P_G)\right), \quad (2)$$

$$\Delta P_L \sim N\left(o, \sigma(\Delta P_L)\right), \quad (3)$$

where $\sigma(\Delta P_G)$ and $\sigma(\Delta P_L)$ are standard deviation of global variation and local variation, respectively.

2.2.2 Specific model parameter selection

MOS transistors have many relevant physical and electrical parameters. The commonly used BSIM3v3 model has more than 100 parameters [39]; however, only a small number of these change significantly due to process variation. Therefore, model parameter selection is significant for the construction of simple and practical statistical device model for analog LSI designs.

For analog circuits, drain current of a MOS transistor is very important, which is

paid much attention during circuit design and simulation. The variation of drain current will influence the performance of circuits directly. Therefore, in the proposed model for MOS transistors, the selection of model parameters is based on the drain current. That means some parameters which have much more significant effect on the drain current are chosen as the model parameters for MOS transistors.

The drain current for MOS transistors in saturation region is shown as [42]:

$$I_D = \frac{1}{2}\mu\frac{\varepsilon_{ox}}{t_{ox}}\frac{W}{L}(V_{GS} - V_{th})^2, \tag{4}$$

where μ is the carrier mobility, ε_{ox} is the permittivity of gate oxide, t_{ox} is the gate oxide thickness, L and W are the length and width of the channel for MOS transistors, V_{GS} is the gate-to-source voltage and V_{th} is the threshold voltage. In a constant process, μ and ε_{ox} are almost no change. Besides, for different conditions and it is not related with process variation. While, the parameters t_{ox}, V_{th}, L and W have physical meaning for circuit designers and their deviations due to process variation will affect the drain current of MOS transistors directly. Therefore, the parameters of the proposed model are shown in Table 1.

Table 1: Model parameters.

Gate Oxide Thickness	t_{ox}
Threshold Voltage	V_{th}
Gate Length	L
Gate Width	W

2.2.3 Global variation

For MOS transistors, due to internal relations of manufacturing process, some parameters have correlation relationships. For example, threshold voltage V_{th} has the

correlation with the doping concentration in the channel N_{CH} and the gate oxide thickness t_{ox}. If N_{CH} increases, V_{th} decreases. Conversely, if t_{ox} increases, V_{th} increases. In addition, some parameters between NMOS and PMOS also have correlation. Therefore, the global variation in the proposed model considers the correlation relationship. In the proposed model, a correlation matrix is used to make the global variation vary more reasonable. Equation (5) shows the correlation matrix of n parameters for both NMOS transistors and PMOS transistors.

$$R = \begin{array}{c} \\ N.P_{1G} \\ \vdots \\ N.P_{nG} \\ P.P_{1G} \\ \vdots \\ p.P_{nG} \end{array} \begin{array}{c} \begin{array}{cccccc} N.P_{1G} & \cdots & N.P_{nG} & P.P_{1G} & \cdots & P.P_{nG} \end{array} \\ \begin{bmatrix} 1 & \cdots & r_{1,n} & r_{1,n+1} & \cdots & r_{1,2n} \\ \vdots & 1 & \vdots & \vdots & \vdots & \vdots \\ r_{n,1} & \cdots & 1 & r_{n,n+1} & \cdots & r_{n,2n} \\ r_{n+1,1} & \cdots & r_{n+1,n} & 1 & \cdots & r_{n+1,2n} \\ \vdots & \vdots & \vdots & \vdots & 1 & \vdots \\ r_{2n,1} & \cdots & r_{2n,n} & r_{2n,n+1} & \cdots & 1 \end{bmatrix} \end{array} \tag{5}$$

In the correlation matrix, the correlation value is from -1 to 1. For two parameters, if the correlation value equals 0, it means that these two parameters have no correlation relationship. If the correlation value equals 1, it means these two parameters are positive correlated. Conversely, if the correlation value equals -1, it represents the negative correlation of these two parameters. Meanwhile, because correlation value can be any values from -1 to 1, larger absolute value of correlation value represents stronger correlation relationship.

After obtaining the standard deviation of global variation and the correlation matrix, the reverse calculation of Principal Component Analysis (PCA) is used to generate final specific deviations for global variation [43]. PCA is a mathematical procedure that uses an orthogonal transformation to convert a set of observations of possibly correlated variables into a set of values of uncorrelated variables called principal components. The

number of principal components is less than or equal to the number of original variables. The principal component *C* is expressed as [36]:

$$\mathrm{C} = \Lambda^{-0.5} U^{-1} S, \tag{6}$$

where *Λ* is the diagonal matrix containing the eigenvalues of the correlation matrix, *U* is the corresponding eigenvector of the correlation matrix. $S=(P-\mu)/\sigma$ is the parameter *P* after standardization, where μ and σ are the mean value and standard deviation of parameter *P*, respectively.

In the proposed model, the reverse calculation of Eq. (6) is done and the expression for *P* is obtained. Then the specific deviation value for global variation ΔP_G is expressed as:

$$\Delta P_G = \sigma U \Lambda^{0.5} C. \tag{7}$$

2.2.4 Local variation

Similar as the global variation, the distribution of local variation can be also regarded as following the Gaussian distribution as shown in Eq. (3). In the proposed model, the local variation is achieved based on Pelgrom's model [35]. That means the parameter *P* in the proposed model will have the standard deviation $\sigma(\Delta P_L)$, which is expressed as:

$$\sigma(\Delta P_L) = \frac{A_P}{\sqrt{L*W}}, \tag{8}$$

w

2.3 Model parameter extraction and measurement results

Experimental results are based on the measurement data of OP-Amp circuits using 0.65 um process technology on some wafers. These wafers belong to 19 different lots. Every lot includes 25 wafers and every wafer includes 3 chips. Each chip includes 3 same circuits at different positions. For every chip, the transistor parameters t_{ox}, V_{th}, L, W and current factor $\beta = \mu C_{ox}\frac{W}{L}$ of NMOS and PMOS transistors are measured.

Firstly, the local variation is extracted. For local variation in the proposed model, only two parameters A_{tox} and A_{vth} are needed to be obtained, where t_{ox} and V_{th} are two P parameters of A_P. A practical method to extract these local variation parameters is proposed.

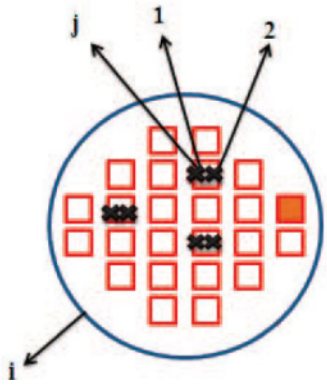


Fig. 2.2: Diagram of chip used for local parameter extraction.

As shown in Fig. 2.2, two MOS transistors on every chip are chosen. For all transistors marked 1 on every chip have the same size and all transistors marked 2 have another same size. Then the total value expression of one parameter for these two transistors on one chip is shown below:

$$P_{ij1} = P_{typ} + \Delta P_{Gij} + \Delta P_{Lij1}, \tag{9}$$

$$P_{ij2} = P_{typ} + \Delta P_{Gij} + \Delta P_{Lij2}, \tag{10}$$

where i is the wafer number, j is the chip number, P_{ij1} and P_{ij2} are the total value for MOS transistor 1 and 2. P_{typ} is the typical value, ΔP_{Gij} is the global variation, ΔP_{Lij1} and ΔP_{Lij2} are the local variation.

Because transistors 1 and 2 are on the same chip, the typical value and global variation are same. An equation is obtained through subtracting Eq. (9) by Eq. (10):

$$P_{ij1} - P_{ij2} = \Delta P_{Lij1} - \Delta P_{Lij2}, \tag{11}$$

then the standard deviations of both sides of Eq. (11) are calculated:

$$\sigma(P_{ij1} - P_{ij2}) = \sigma(\Delta P_{Lij1} - \Delta P_{Lij2}). \tag{12}$$

Because the local variations for transistors 1 and 2 are independent, the Eq. (12) is simplified as:

$$\sigma(P_{ij1} - P_{ij2}) = \sqrt{\sigma^2(\Delta P_{Lij1}) + \sigma^2(\Delta P_{Lij2})}. \tag{13}$$

Applying the standard deviation equation for local variation to Eq. (13) and getting the last equation:

$$\sigma(P_{ij1} - P_{ij2}) = \sqrt{(\frac{A_P}{L_{ij1} * W_{ij1}})^2 + (\frac{A_P}{L_{ij2} * W_{ij2}})^2}, \tag{14}$$

where A_P is the coefficient, L_{ij1} and L_{ij2} are the length of transistor 1 and 2, W_{ij1} and W_{ij2} are the width of transistors 1 and 2. Actually, the parameter P_{ij1} and P_{ij2} are easily measured, the length and width of MOS transistors are also easily obtained. Therefore, for Eq. (14), $\sigma(P_{ij1} - P_{ij2})$ is known, the length and width are also known, thus Eq. (14) is easily solved. After solving Eq. (14), the value of A_P is obtained. Finally, the standard deviation for local variation of MOS transistors is calculated using Eq. (8).

After obtaining the local variation for MOS transistors, the global variation is

calculated easily. Firstly, the variances of the both sides of Eq. (1) are calculated:

$$\sigma^2(P_{total}) = \sigma^2(P_{typ} + \Delta P_G + \Delta P_L). \tag{15}$$

Because P_{typ} is a constant value, the Eq. (15) is simplified as:

$$\sigma^2(P_{total}) = \sigma^2(\Delta P_G + \Delta P_L). \tag{16}$$

For a transistor, the global variation and local variation are independent, therefore Eq. (16) is further simplified as:

$$\sigma^2(P_{total}) = \sigma^2(\Delta P_G) + \sigma^2(\Delta P_L). \tag{17}$$

In Eq. (17), $\sigma(P_{total})$ is easily obtained through chip measurement, $\sigma(\Delta P_L)$ is calculated using A_P obtained before. Thus, Eq. (17) is solved and the standard deviation of global variation $\sigma(\Delta P_G)$ is expressed as:

$$\sigma(P_G) = \sqrt{\sigma^2(\Delta P_{total}) - \sigma^2(\Delta P_L)}. \tag{18}$$

The correlation matrix is an important component of the proposed model. An approximate method to extract the correlation matrix of global variation is proposed.

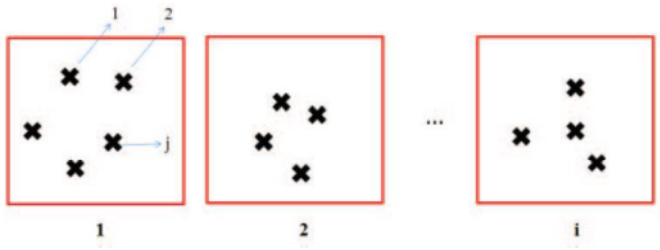


Fig. 2.3: Diagram of chips for correlation matrix extraction.

Some chips are chosen, every chip have some parameters as shown in Fig. 2.3. Firstly, calculating the mean value of parameter P for every chip as Eq. (19):

$$\overline{P_i} = \frac{P_{i1}+P_{i2}+\cdots P_{ij}}{j}, \tag{19}$$

where i is the chip number, j is the number of transistors on one chip, $\overline{P_i}$ is the mean value of parameter P for chip i, P_{ij} is the value of the parameter P for transistor j

on chip i.

Then the mean value of parameter $\overline{P_i}$ among different chips is calculated, and this mean value $\bar{P}$ is expressed as:

$$\bar{P} = \frac{\overline{P_1}+\overline{P_2}+\cdots\overline{P_i}}{i}. \tag{20}$$

Similarly, the two mean values of the other parameter Q is also expressed in the similar way:

$$\overline{Q_i} = \frac{Q_{i1}+Q_{i2}+\cdots Q_{ij}}{j}, \tag{21}$$

$$\bar{Q} = \frac{\overline{Q_1}+\overline{Q_2}+\cdots\overline{Q_i}}{i}. \tag{22}$$

Finally, the correlation value of global variation for parameter P and Q is expressed as:

$$r_{PQ} = \frac{\sum_{k=1}^{i}(\overline{P_k}-\bar{P})(\overline{Q_k}-\bar{Q})}{\sqrt{[\sum_{k=1}^{i}(\overline{P_k}-\bar{P})^2][\sum_{k=1}^{i}(\overline{Q_k}-\bar{Q})^2]}}. \tag{23}$$

The proposed method is used to obtain the model parameters. These model parameters include three parts whose real values are not shown due to the confidential contract:

- The standard deviation of global variation for 4 parameters about NMOS and PMOS (Table 2: $\sigma_G(t_{ox})_{NMOS}$, $\sigma_G(V_{th})_{NMOS}$, $\sigma_G(L)_{NMOS}$, $\sigma_G(W)_{NMOS}$ are the standard deviation of t_{ox}, V_{th}, L and W for NMOS; $\sigma_G(t_{ox})_{PMOS}$, $\sigma_G(V_{th})_{PMOS}$, $\sigma_G(L)_{PMOS}$, $\sigma_G(W)_{PMOS}$ are the standard deviation of t_{ox}, V_{th}, L and W for PMOS).

Table 2: Global variation parameter.

$\sigma_G(t_{ox})_{NMOS}$	$\sigma_G(t_{ox})_{PMOS}$
$\sigma_G(V_{th})_{NMOS}$	$\sigma_G(V_{th})_{PMOS}$
$\sigma_G(L)_{NMOS}$	$\sigma_G(L)_{PMOS}$
$\sigma_G(W)_{NMOS}$	$\sigma_G(W)_{PMOS}$

- The correlation matrix of global variation for 4 parameters about NMOS and PMOS as shown in Eq. (24):

$$R = \begin{array}{c} \\ N.W_G \\ N.Vth_G \\ N.L_G \\ N.W_G \\ P.tox_G \\ P.Vth_G \\ P.L_G \\ P.W_G \end{array} \begin{array}{c} \begin{array}{cccccccc} N.tox_G & N.Vth_G & N.L_G & N.W_G & P.tox_G & P.Vth_G & P.L_G & P.W_G \end{array} \\ \begin{pmatrix} 1 & r_{12} & r_{13} & r_{14} & r_{15} & r_{16} & r_{17} & r_{18} \\ r_{21} & 1 & r_{23} & r_{24} & r_{25} & r_{26} & r_{27} & r_{28} \\ r_{31} & r_{32} & 1 & r_{34} & r_{35} & r_{36} & r_{37} & r_{38} \\ r_{41} & r_{42} & r_{43} & 1 & r_{45} & r_{46} & r_{47} & r_{48} \\ r_{51} & r_{52} & r_{53} & r_{54} & 1 & r_{56} & r_{57} & r_{58} \\ r_{61} & r_{62} & r_{63} & r_{64} & r_{65} & 1 & r_{67} & r_{68} \\ r_{71} & r_{72} & r_{73} & r_{74} & r_{75} & r_{76} & 1 & r_{78} \\ r_{81} & r_{82} & r_{83} & r_{84} & r_{85} & r_{86} & r_{87} & 1 \end{pmatrix} \end{array} \tag{24}$$

- The coefficient of local variation for 2 parameters about NMOS and PMOS (Table 3: $A_{toxNMOS}$ and $A_{vthNMOS}$ are the coefficient of local variation about t_{ox} and V_{th} for NMOS; $A_{toxPMOS}$ and $A_{vthPMOS}$ are the coefficient of local variation about t_{ox} and V_{th} for NMOS). The coefficient of local variation for oxide thickness is obtained from the coefficient of local variation for current factor β.

Table 3: Local variation parameter.

$A_{toxNMOS}$	$A_{toxPMOS}$
$A_{VthNMOS}$	$A_{VthPMOS}$

Firstly, the coefficient $A_{\beta NMOS}$ and $A_{\beta PMOS}$ are extracted from the chip measurement data. Then the local variation percentages of β_{NMOS} and β_{PMOS} are calculated. After that, it is assumed that, the oxide thickness of NMOS and PMOS have the same local variation percentage as β_{NMOS} and β_{PMOS}, respectively. Finally, the value of $A_{toxNMOS}$ and $A_{toxPMOS}$ are obtained according to the local variation percentage.

After obtaining the model parameters, the proposed model is applied to do statistical analysis of Op-Amp using Monte Carlo analysis. The performance parameters of Op-Amp are also compared with practical measurement data.

The performance parameters of Op-Amp are voltage gain and current consumption. The distribution of these two performance parameters obtained from chip measurement and simulations using the proposed model are shown in Fig. 2.4 and Fig. 2.5, respectively.

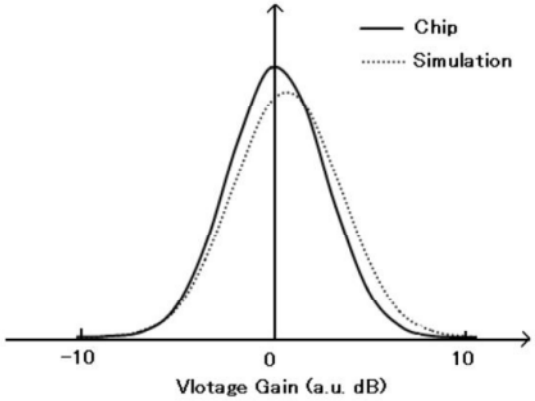


Fig. 2.4: The distribution of voltage gain obtained from chip measurement and simulation.

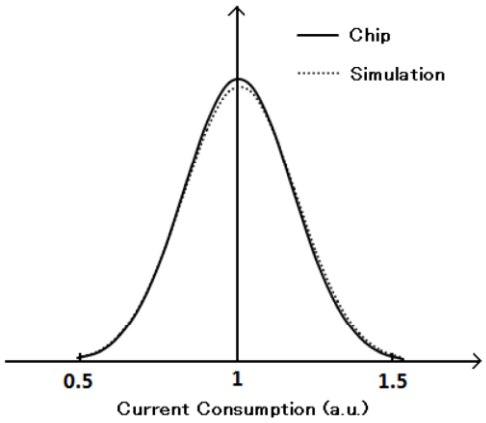


Fig. 2.5: The distribution of current consumption obtained from chip measurement and simulation.

From the statistical analysis results of these two performance parameters for Op-Amp circuit, it is found that the statistical simulation analysis based on the proposed model has a good agreement with practical chip measurement results. The errors of the mean value and the standard deviation for voltage gain obtained from simulations using the proposed model are 1 dB and 0.3 dB compared with the chip measurement results, respectively. While for performance parameter of current consumption, the errors are only 0.01% and 3.03%, respectively. Therefore, the proposed model, used to reflect the process variation of some key parameters for MOS transistors, is capable to predict the variation of some performance parameters about analog circuit accurately.

2.4 Circuits simulation applications for Chapter 3 and Chapter 4

In Chapters 3 and 4, the local model of the statistical analysis model presented in Chapter 2 is used. Meanwhile, how to do the Monte Carlo simulations in Chapter 3 and 4 are also same as Chapter 2.

2.5 Summary

In this chapter, a simple and practical device model for LSI design is proposed. The proposed model considers the global and local variation of MOS transistors with 4 parameters. In the global model of MOS transistors in this section, correlations of MOS transistors are specifically researched in calculating the global standard deviation of MOS transistors. Finally, the proposed model is applied to predict the variations of some

pa -Amp circuit. The error of the mean value and the standard deviation for voltage gain obtained from simulations using the proposed model are 1 dB and 0.3 dB compared with the chip measurement results. While for performance parameter current consumption, the error is only 0.01% and 3.03%. The statistical analysis results demonstrate that the proposed model is accurate compared with practical chip measurement results.

In the future, the model is considered to be improved based on much more practical data in different processes. The model parameters should be modified if used for other different process technology.

3 Accurate Nanopower Supply Insensitive CMOS Unit V_{th} Extractor and Continuous αV_{th} Extractor by Overdrive Voltage Control Technique

3.1 Introduction

The threshold voltage (V_{th}) is one of the most salient characteristics of the metal-oxide-semiconductor (MOS) transistor. Traditionally, V_{th} is extracted using graphical or numerical methods [44]; however, these methods are complicated, too expensive to implement on chips, and only applied for measuring MOS transistor characteristics.

A V_{th} extractor is a circuit that automatically extracts the V_{th} of a MOS transistor and generates the V_{th} value as an output voltage. The extractor is useful for process characterization, device modelling, temperature compensation and temperature measurement [3][22][24][45]-[47].

First-generation unit V_{th} extractors require a reference voltage for biasing [3][45][48]. To solve this problem, self-biased unit V_{th} extractors have been proposed [49]-[51]. A V_{th} extractor is also used to cancel out V_{th} voltage in several *V-I* and *I-V* conversion circuits or produce accurate bias conditions. For these uses, the V_{th} extractor sometimes needs battery operation; therefore, the power consumption of the V_{th} extractor is a factor that cannot be ignored. Thus, accurate low power consumption CMOS unit V_{th} extractors have been proposed [1][2], which consume several micro-Watts of power. However, circuits

with nano-level power consumption are required nowadays. With these issues in mind, an accurate nanopower supply-insensitive CMOS unit V_{th} extractor is needed.

Voltage extractors whose output voltages follow linearly to temperature are also required nowadays. Considering the applications of temperature independent reference voltage circuit and temperature sensor for portable devices, some researches have been done in the area of low power α times variable voltage extractors design. For the first application, a voltage generation circuit with positive temperature dependence and a negative temperature dependent V_{th} extractor are commonly used [24][47]. To compensate temperature dependence, careful design is needed. When continuous α times V_{th} extractor is applied, the adjustment of temperature dependence becomes much easier for optimized value generation. Both V_{th} extractor with Op-Amps and bipolar junction transistor (BJT) circuits realize continuous α times temperature dependent voltage extraction [22]-[24][47][52]. However, the power consumption is a problem. Moreover, BJT solution requires curvature correction because its temperature dependence is not linear. For low power CMOS circuit design, an α times V_{th} extractor (α is an integer) is proposed in [3]. Although the power consumption and cost is reduced, it does not have a merit of continuous α times V_{th} extractor.

In this paper, an accurate nanopower supply-insensitive CMOS unit V_{th} extractor and a low power α times V_{th} (αV_{th}) extractor with continuous variety are proposed by overdrive voltage control technique. With the αV_{th} extractors, both incremental and decremental αV_{th} voltages are obtained by simply adjusting the transistor sizes. The target is that, the power consumption be smaller than 1 uW (nanopower) and supply-sensitivity be less than 0.05%/V (half of conventional circuits) for unit V_{th} extractor. The power consumption realize from micro-Watt to nano-Watt, and supply-sensitivity be less

than 0.15%/V (close to conventional unit αV_{th} extractors) for αV_{th} extractor.

3.2 V_{th} extractor and continuous α times V_{th} extractors

In this section, a self-biased nanopower CMOS unit V_{th} extractor circuit is proposed. In 3.2.1, circuit and operation are introduced. In 3.2.2, output voltage stability is analyzed. In 3.2.3, overall tradeoff is shown. The αV_{th} extraction is discussed in 3.2.4. Finally, the layout discussion is shown in 3.2.5.

3.2.1 Schematic and work principle of unit V_{th} extractor

- **V_{th} extractor circuit**

Figure 3.1 shows the proposed circuit. It consists of a current source and the generate part. It is assumed that, the current mirror ratios have the relationship $S_{M1}: S_{M4}: S_{M5} =$ b: 1: a and $S_{M9}: S_{M7} = \left(\frac{b}{2}\right): a$, where S_M is the W/L ratio of each transistor. As the gate-source voltage $V_{gs7} = V_{gs9}$, following current relationships are obtained,

$$I_{M9}: I_{M7} = \left(\frac{b}{2}\right): a, \tag{25}$$

$$I \tag{26}$$

Thus, the transistor currents have the following relationship:

$$I_{M2}: I_{M3}: I_{M7}: I_{M8}: I_{M9} = \left(\frac{b}{2}\right): \left(\frac{b}{2}+1\right): a: \left(\frac{b}{2}\right): \left(\frac{b}{2}\right). \tag{27}$$

This relationship is used to the analysis of the operation point in the next subsection.

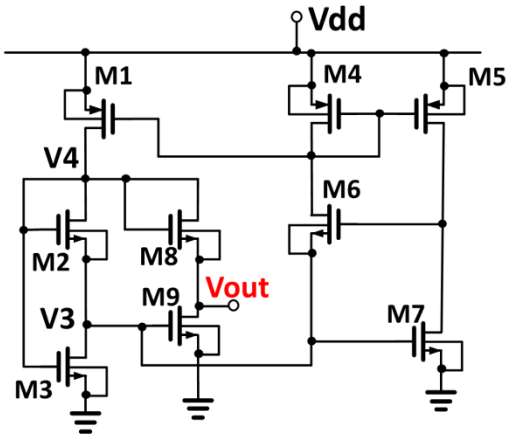


Fig. 3.1: The proposed nanopower unit complementary metal-oxide-semiconductor (CMOS) V_{th} extractor circuit.

- **Analysis of the operation point**

This part shows the analysis of the stable operation point and use the results later for the output voltage (V_{out}) value, nanopower, and minimum supply voltage. This analysis is based on the long channel model. The transistors M_3 operates in triode region and the transistor M_2, M_7, M_8 and M_9 operate in saturation region. The currents I_{M2}, I_{M3}, I_{M7}, I_{M8} and I_{M9} are expressed as follows,

$$I_{M2} = \frac{1}{2}\mu C_{ox} S_{M2}(V_4 - V_3 - V_{th})^2, \quad (28)$$

$$I_{M3} = \mu C_{ox} S_{M3}(V_4 - V_{th} - \frac{V_3}{2})V_3, \quad (29)$$

$$I \quad -\mu C_{ox} S_{M7}(V_3 - V_{th})^2, \quad (30)$$

$$I \quad -\mu C_{ox} S_{M8}(V_4 - V_{out} - V_{th})^2, \quad (31)$$

$$I \quad -\mu C_{ox} S_{M9}(V_3 - V_{th})^2, \quad (32)$$

w

If transistor sizes satisfy $S_{M2} = S_{M9}$, the following equation is obtained, as mentioned in [52]:

$$V_4 = 2V_3. \tag{33}$$

Then, considering Eqs. (27)-(29) and (33) together, the following is obtained:

$$\left(\frac{b}{2}+1\right)\frac{1}{2}\mu C_{ox}S_{M2}(V_3 - V_{th})^2 = \frac{b}{2}\,\mu C_{ox}S_{M3}\left(\frac{3V_3}{2} - V_{th}\right)V_3. \tag{34}$$

By taking a solution that meets the condition $V_3 > V_{th}$, the node voltage V_3 is obtained as:

$$V_3 = (1+\gamma)V_{th}, \tag{35}$$

$$\gamma = \frac{2bS_{M3} + \sqrt{b(b+2)S_{M2}S_{M3} + b^2S_{M3}^2}}{(b+2)S_{M2} - 3bS_{M3}}. \tag{36}$$

As γ is determined only by the CMOS transistor *W/L* ratios, the values of V_3 and V_4 are determined by the MOS transistor *W/L* ratios and the V_{th} value, which is the advantage of this work. Thus, the transistors, are self-biased to the voltages determined by the V_{th} and *W/L* ratios. Because V_3 is equal to the gate-source voltage V_{gs2} (as the value of V_3 is equal to that of $V_4 - V_3$) of transistor M_2, the overdrive voltage V_{ov2} and the drain current I_{M2} of transistor M_2 are expressed as follows:

$$V_{ov2} = V_3 - V_{th} = \gamma V_{th}, \tag{37}$$

$$I \quad -\mu C_{ox}S_{M2}\gamma^2 V_{th}^2. \tag{38}$$

In Fig. 3.2, the relationships between $\frac{V_{ov2}}{V_{th}}$ a — a

lows:

$$\frac{V_{ov2}}{V_{th}} = \gamma. \tag{39}$$

Here, the overdrive voltage of transistor M_2 is adjusted by the transistor size. The other transistors have a similar relationship are proved in the same way.

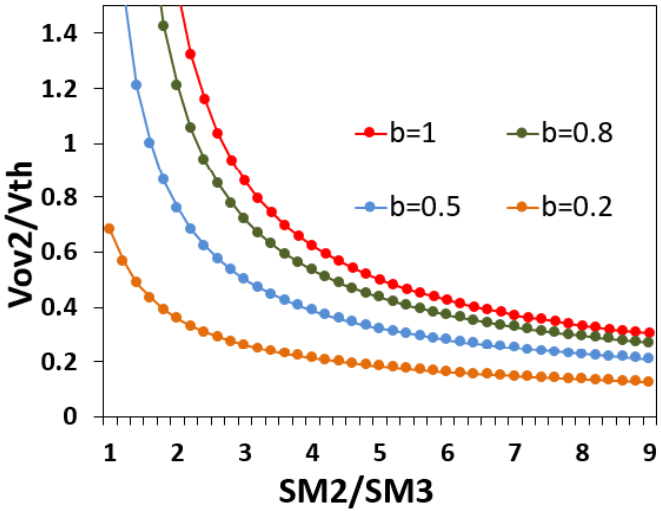


Fig. 3.2: The relationships between overdrive voltage V_{ov} over V_{th} and the transistor size ratio of S_{M2} over S_{M3}.

- **Unit V_{th} extraction**

To extract the V_{th} value, the technique is shown below. Output V_{th} is obtained by adding and subtracting V_{gs} of transistors M_2, M_8 and M_9. According to Kirchhoff's voltage laws, the output voltage of the proposed circuit is shown as follows:

$$\begin{aligned} V_{out} &= V_{gs9} + V_{gs2} - V_{gs8} \\ &= (V_{ov9} + V_{th}) + (V_{ov2} + V_{th}) - (V_{ov8} + V_{th}) \\ &= V_{th} + (V_{ov9} + V_{ov2} - V_{ov8}). \end{aligned} \tag{40}$$

The W/L ratios of transistors M_2, M_8 and M_9 are set to be $S_{M2} = S_{M9} = 4S_{M8}$. Since the saturation current of M_2, M_8 and M_9 are the same, $V_{ov8} = 2V_{ov9} = 2V_{ov2}$, the equation is obtained:

$$V_{out} = V_{th}. \tag{41}$$

The CMOS unit V_{th} extractor is realized by the proposed circuit. It should be noted that V_{ov} is cancelled and the output voltage is only expressed as V_{th}.

- **Power consumption**

All the transistors work in the strong inversion region. To reduce power consumption with the proposed structure, one method is to reduce the *W/L* ratio value, so that the current is reduced. The other method is to reduce the overdrive voltage of each transistor. Small V_{ov} is obtained by adjusting $\frac{S_{M2}}{S_{M3}}$. These two methods are applied together to obtain a reasonably small current. The limitations of the *W/L* ratio and V_{ov} are discussed later.

- **Minimum supply voltage**

The operation of the transistor in the strong inversion region enters the cutoff region, when the supply voltage decreases. The minimum supply voltage V_{DDmin} should satisfy the following:

$$V_{DDmin} > V_{ov1} + V_{gs2} + V_{gs9} = V_{ov1} + V_{ov2} + V_{ov9} + 2V_{th}, \quad (42)$$

w -to-source voltage of transistor M_2 and V_{gs9} is the gate-to-source voltage of transistor M_9.

The method to reduce the minimum supply voltage is to reduce the value of the overdrive voltages of the transistors. Considering the accuracy of the circuit, assuming $V_{th} = 0.5$ V, overdrive voltage is considered not smaller than 0.15 V for V_{ov1}, V_{ov2}, V_{ov9}. $V_{DDmin} > 1.45$ V is obtained.

3.2.2 Output voltage stability analysis of unit V_{th} extractor

In this part, the output voltage stability is analyzed together with some simulation. An HSPICE is used for simulation. The simulation model is BSIM3, and the ROHM 0.18 um CMOS technology is used.

- **Supply voltage dependence and drain-induced barrier lowering (DIBL)**

Ideally V_{out} is constant when the current I_M saturates completely, and I_M follows the Eqs. (29), and (30)-(32). But in reality, by short channel effect (or DIBL), the saturation current has V_{DD} dependence and then V_{out} has a V_{DD} dependence.

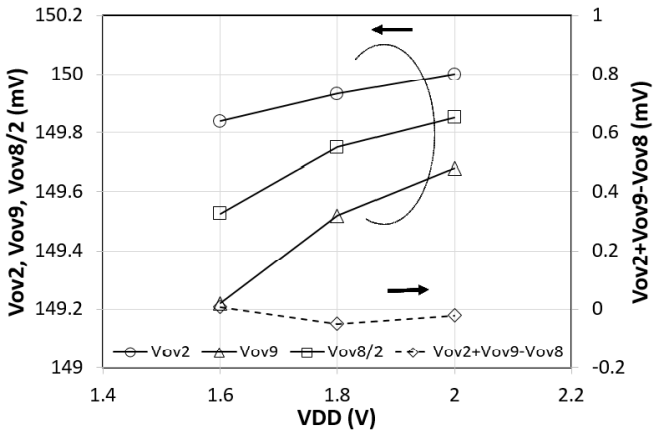


Fig. 3.3: Overdrive voltages V_{ov2}, V_{ov8}, and V_{ov9} for different supply voltages.

The second order effect is suppressed and cancelled in the following ways:

First, long channel length is applied to reduce the DIBL factor η, with which V_{th} is expressed as $V_{th} = V_{th0} - \eta V_{ds}$. The simulation results show that, for NMOS the minimum $\mathrm{L} = 120\mathrm{um}$, η is only approximately 0.00006; for PMOS the minimum $\mathrm{L} = 16\mathrm{um}$, η is only approximately 0.001. The overdrive voltage change ΔV_{ov} is reduced to 0.2 mV-0.5mV as shown in Fig. 3.3.

Second, the overdrive voltages V_{ov2}, V_{ov8}, and V_{ov9} increase as V_{DD} increase together. Small ΔV_{ov} at M_2, M_8, and M_9 are cancelled, where $\Delta V_{ov2} + \Delta V_{ov9} - \Delta V_{ov8} < 0.05$ mV. The broken line in Fig. 3.3 shows this.

Thus, the supply voltage dependence is greatly reduced.

- **Temperature sensitivity**

Temperature dependence is mainly caused by subthreshold current, because it is not included in Eqs. (29), and (30)-(32), and it has a different temperature dependence as compared with saturation current.

If V_{ov} is close to zero, the subthreshold current cannot be neglected. On the other hand, a too large value of V_{ov} increases the minimum supply voltage and power consumption. Thus, the V_{ov} value should not be too large either. The smallest V_{ov} is selected at which the subthreshold current is neglectable.

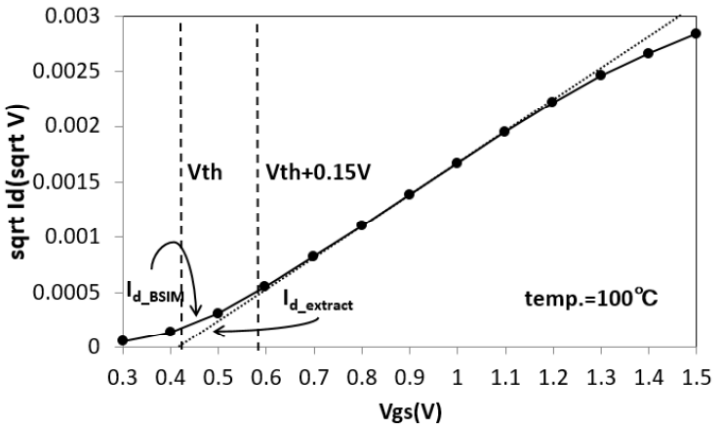


Fig. 3.4: The dependence of sqrt I_d on V_{ov} at high temperature (100C°).

Figure 3.4 shows the dependence of $\sqrt{I_d}$ on V_{ov} at high temperature (100C°). Where I_{d_BSIM} is the current consists of the subthreshold current and saturation current; and $I_{d\_extract}$ is the extracted saturation current from the Figure. When $V_{ov} = 0.15$ V, $V_{ov} = 0.1$ V, and $V_{ov} = 0.05$ V, the errors of the current function are 1%, 3.2%, and 15.9%, respectively (these errors are calculated using $\frac{I_{d\_BSIM} - I_{d\_etract}}{I_{d\_extract}}$).

Note that *W/L* ratios are adjusted to obtain different V_{ov} values. When $V_{ov} = 0.15$ V, $V_{ov} = 0.1$ V, and $V_{ov} = 0.05$ V, the temperature sensitivity errors of V_{out} calculated in

Eq. (43) a .02%, 0.03%, and 0.11% in the temperature range of $T_{min} =$ 0 ℃ and $T_{max} = 100$ C°, respectively. An overdrive voltage of $V_{ov} = 0.1$ V is acceptable, but $V_{ov} = 0.15$ V with 0.05 V margin is selected.

$$Sensitivity_{\_temp.} = \frac{\max(|V_{out}(T) - V_{thM2}(T)|)}{(T_{max} - T_{min}) average(V_{out})}. \quad (43)$$

The simulation results are compared with the V_{th} value of transistor M_2 (V_{thM2}) in the library, which is obtained by "DC .op" statement in the simulation. This is used as the real V_{th} value.

- **Mismatch effect**

Mismatch is considered by extracting key parameter related to the output voltage. To take care of mismatch, Different V_{th} are used for each transistor in Eq. (40). The expression is shown below,

$$V_{out} = V_{ov9} + V_{ov2} - V_{ov8} + V_{thn2} + V_{thn9} - V_{thn8}. \quad (44)$$

Therefore, the variation is expressed as follows:

$$\Delta V_{out} = -\frac{V_{ov9}}{2}\frac{\Delta K_9}{K_9} - \frac{V_{ov2}}{2}\frac{\Delta K_2}{K_2} - \frac{V_{ov8}}{2}\frac{\Delta K_8}{K_8} + \Delta V_{thn9} + \Delta V_{thn2} + \Delta V_{thn8}, \quad (45)$$

where $K_i = \mu C_{ox} S_{Mi}$. According to Pelgram's model, σK and σV_{th} are given as follows:

$$\sigma\frac{\Delta K}{K} = \frac{A_K}{\sqrt{WL}}, \quad (46)$$

$$\sigma\Delta V_{th} = \frac{A_{Vt}}{\sqrt{WL}}. \quad (47)$$

Both of them are inversely proportional to the transistor area (WL). Thus, by using a larger transistor size, $\frac{\Delta K}{K}$, ΔV_{th} and ΔV_{out} are reduced.

3.2.3 Overall tradeoff

Three cases are compared to discuss tradeoffs. Transistor sizes are summarized in the upper half of Table 4. Case 1 uses a minimum width of 0.18 um to reduce the gate area; The width is increased to 1 um in case 2 with nearly the same length, and the gate area is increased to reduce mismatch; The same width used in case 2 is maintained in case 3 while the length is reduced to obtain a smaller gate area.

In each case, local variation has been simulated using the model in [53]. The output voltages are compared with A_{vthM2}. For the local variation, both the random *Vth* variation, and the random *K* variation are considered. The A_k and A_{vth} are extracted from [54], where $A_{vthn} = 4.2$ mV*um, $A_{vthp} = 2.9$ mV*um and $A_{kn} = A_{kp} =$ 1.3%*um.

Noise simulation has also been done. Using a function of HSPICE. The noiMod flag 2 is selected for the BSIM3 noise model, so that both thermal noise and flicker noise are considered. The noise power spectral density (PSD) is accumulated with the bandwidth from 100 Hz to 100 KHz to calculate root mean square of noise voltage.

For the circuit design, one of the case is chosen considering the tradeoffs between supply voltage, mismatch, power, and noise shown in the lower half of Table 4. For case 1, the current, power consumption, and gate area are the smallest. However, the mismatch is 4.25% and the noise error is 0.46%. For case 3, the gate area is nearly the same as case 1 and the noise error is reduced to 0.05%. The mismatch is 2.82%, which is still more than 1 %. Moreover, the power consumption is close to 1 uW. For case 2, the power consumption is small and its each error is smaller than 1%. However, the area of case 2 is the largest. From the viewpoint of performance (noise, mismatch and power consumption), case 2 is chosen as this proposed unit V_{th} extractor circuit design.

Table 4: Comparison of V_{th} extractor characteristics by different transistor sizes.

	CASE 1		CASE 2		CASE 3	
MOS transistors	W_1 (um)	L_1 (um)	W_2 (um)	L_2 (um)	W_3 (um)	L_3 (um)
M_1	0.5	4	2	16	0.5	1
M_4	1	4	4	16	1	1
M_5	0.25	4	1	16	1	1
M_2	0.18	110	1	120	1	40
M_8	0.18	440	1	480	0.25	40
M_9	0.18	110	1	120	1	40
M_3	0.18	790	1	720	1	250
M_6	0.18	100	1	120	1	100
M_7	0.18	110	1	120	1	40
V_{ov} (V)	0.15		0.15		0.15	
I_d (nA)	2.25		24.2		62.5	
Power consumption (nW)	50		179.3		865.2	
Minimum V_{DD} (V)	1.6		1.6		1.6	
Noise (uV/sqrt Hz)	1.11		0.77		0.55	
Noise error	0.46%		0.12%		0.07%	
Mismatch	4.25%		0.55%		2.82%	
Gate area (um^2)	305.8		1792		461.5	

3.2.4 Realization of continuous α times V_{th} extractors

In this section, an αV_{th} extractor is proposed. Continuous αV_{th} extractors without op-amp have not been proposed in previous works. Its continuous varying is realized by changing the overdrive voltage, which is adjusted by the W/L ratios of the transistors.

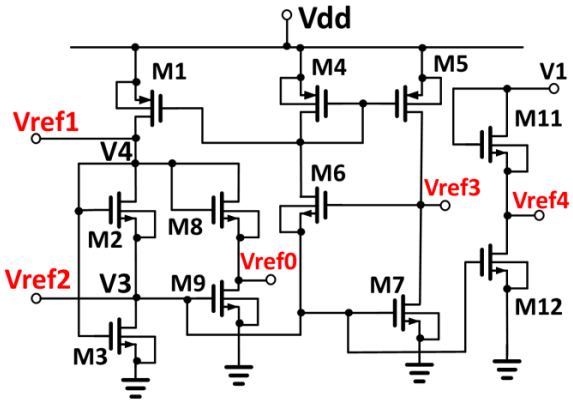


Fig. 3.5: The proposed continuous αV_{th} extractor circuit.

An incremental αV_{th} extractor and a decremental αV_{th} extractor are proposed. The incremental αV_{th} is a reference voltage that has a positive dependence on the threshold voltage and the output value is α times of unit V_{th} value of an NMOS transistor. The decremental αV_{th} is a reference voltage that has negative dependence on the threshold voltage and the output value is a constant voltage minus α times of the unit V_{th} value of an NMOS transistor.

Figure 3.5 shows the αV_{th} extractor circuit consists of both incremental and decremental parts. The incremental circuit is the same as the unit αV_{th} extractor circuit. For the decremental circuit, NMOS transistors M_{11} and M_{12} are added, and V_l is a constant bias voltage. The output voltage V_{ref0} is the same as the unit circuit. The output voltages of V_{ref1}, V_{ref2}, and V_{ref3} are incremental; the output voltage of V_{ref4} is decremental.

- **Incremental αV_{th} extractor**

In Fig. 3.5, three node voltages V_{ref1}, V_{ref2} and V_{ref3} are chosen as the output voltages of the incremental αV_{th} extractor.

According to Eqs. (33) and (35),

$$V_{ref1} = V_4 = 2V_3 = (2 + 2\gamma)V_{th} = \alpha_1 V_{th}, \tag{48}$$

$$V_{ref2} = \alpha_2 V_{th} = V_3 = (1 + \gamma)V_{th} = \frac{1}{2}\alpha_1 V_{th}. \tag{49}$$

Thus $\alpha_1 = 2 + 2\gamma$ and $\alpha_2 = 1 + \gamma$, V_{ref1} and V_{ref2} are incremental αV_{th} voltages, which are α_1 and α_2 times, respectively. As a result, γ is modified according to Eq. (36). For the range of γ is $0.2 < \gamma < 1.4$ in Fig.3.2, the range of the output voltages are as follows:

$$1.2V_{th} < V_{ref2} < 2.4V_{th}, \tag{50}$$

$$2.4V_{th} < V_{ref1} < 4.8V_{th}. \quad (51)$$

It must be noted that if γ increases then current becomes large. As the values of α_1 and α_2 are limited, a node voltage with a much larger α value should be designed. To obtain a larger output voltage range with small current, V_{ref3} is proposed. The drain currents of transistors M_6 and M_7 are as follows:

$$I_{M6} = \frac{1}{2}\mu C_{ox} S_{M6}(V_{ref3} - V_{ref2} - V_{th})^2, \quad (52)$$

$$I_{M7} = \frac{1}{2}\mu C_{ox} S_{M7}(V_{ref2} - V_{th})^2. \quad (53)$$

As the currents satisfy $I_{M6}: I_{M7} = 1: a$, the following relationship below is obtained,

$$V_{ref3} = \alpha_3 V_{th}, \quad (54)$$

where $\alpha_3 = \left(\sqrt{\frac{S_{M7}}{aS_{M6}}} + 1\right)\gamma + 2$, and with even small γ, the α_3 value is capable to still be large to realize low power design.

Therefore, the voltage V_{ref3} is applied as an incremental αV_{th} reference voltage with a much larger α value.

- **Decremental αV_{th} extractor**

Transistors M_{11}, and M_{12} and the constant bias voltage V_1 shown in Fig. 3.5 are used to generate a decremental αV_{th}. A bias voltage V_1 is given to the gate and drain of M_{11} and the gate of M_{12} is connected to V_{ref2} to make the circuit work. The equations are obtained as,

$$I_{M11} = \frac{1}{2}\mu C_{ox} S_{M11}(V_1 - V_{ref4} - V_{th})^2, \quad (55)$$

$$I_{M12} = \frac{1}{2}\mu C_{ox} S_{M12}(V_{ref2} - V_{th})^2. \quad (56)$$

From Eqs. (49), (55) and (56) the voltage V_{ref4} is obtained,

$$V_{ref4} = V_1 - \alpha_4 V_{th}, \tag{57}$$

where $\alpha_4 = 1 + \gamma\sqrt{\frac{S_{M12}}{S_{M11}}}$. The voltage V_{ref4} is obtained as the decremental αV_{th} voltage.

According to Fig. 3.2, the range of γ is $0.2<\gamma<1.4$. The range of α_4 is obtained below,

$$1 + 0.2\sqrt{\frac{S_{M12}}{S_{M11}}} < \alpha_4 < 1 + 1.4\sqrt{\frac{S_{M12}}{S_{M11}}}. \tag{58}$$

The range of V_{ref4} is obtained as follows:

$$V_1 - \left(1 + 1.4\sqrt{\frac{S_{M12}}{S_{M11}}}\right)V_{th} < V_{ref4} < V_1 - (1 + 0.2\sqrt{\frac{S_{M12}}{S_{M11}}})V_{th}. \tag{59}$$

Therefore, the voltage V_{ref4} is applied as a decremental αV_{th} reference voltage.

The important improvements of the αV_{th} extractors presented above are summarized below,

- ✧ An αV_{th} extractor, both incremental and decremental, is implemented with continuous variety.
- ✧ Both incremental and decremental αV_{th} extractors are realized using nano-Watts to several micro-Watts (depends on γ value) power consumption (transistors M_{11} and M_{12} have same level of transistor sizes as the unit αV_{th} extractor).
- ✧ Both incremental and decremental αV_{th} extractors are realized by self-biasing.
- ✧ The α value is adjusted by simply choosing suitable transistor sizes for the circuit transistors according to the function of the transistor overdrive voltage in Fig. 3.2.

3.2.5 Layout discussion

For the practical use of this circuit, decomposition technique and layout solution are shown in this section. The transistor channel decomposition technique [55] is applied to

the proposed circuit. Similar low-power circuits with long lengths or large widths are verified by a test chip and the results show that the error is capable to be ignored and that the transistor array design is applicable. In Fig. 3.6, series transistors with same length are gate connected. Fig. 3.7 shows that the transistors in Table 4: M_2, M_7, and M_9 are divided into 12 units, respectively, while M_8 is divided into 48 units and M_3 is divided into 72 units. Simulation results for the decomposition of the long length transistors into W=L=1 um/10 um transistors are shown in Fig. 3.8. Comparing L = 120 um and decomposed L = 10 um, with n = 12, the error of the saturation current is approximately 0.2%. Comparing L = 480 um and decomposed L = 10 um, with n = 48, the error is approximately 0.81%. As such, the relationship fits well with the long length transistors and the decomposition.

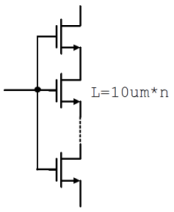


Fig. 3.6: Circuit of decomposition for large length.

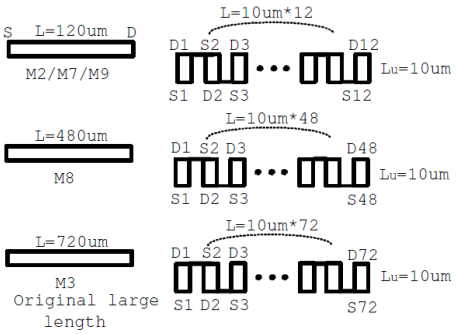


Fig. 3.7: Layout of decomposed transistors.

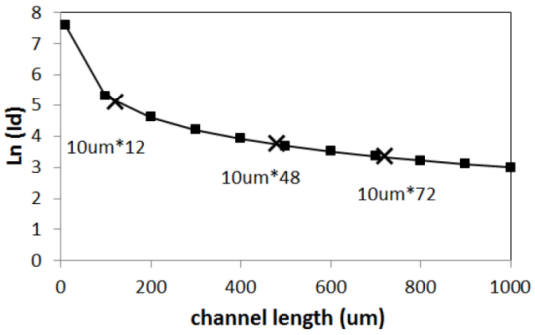


Fig. 3.8: Comparison of the decomposed and not-decomposed simulation results.

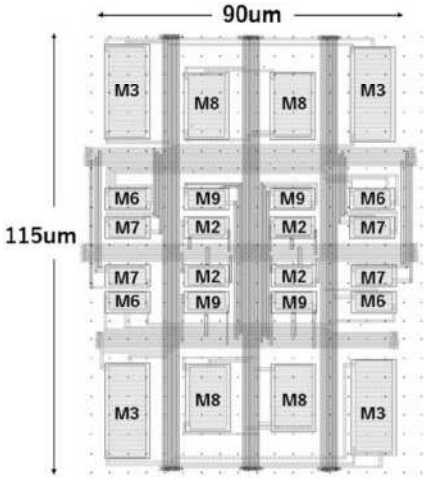


Fig. 3.9: The common centroid layout.

As shown in Fig. 3.9, common centroid technique [56] is used for the layout design of NMOS transistors, which reduces the influence of the systematic mismatch. All of M_2, M_3, M_7, M_8 and M_9 are composed with the same size unit transistors $W = L$ = 1 um/10 um, and furthermore, placed in a common centroid. This improves transistor matching and all five transistors have a similar threshold voltage.

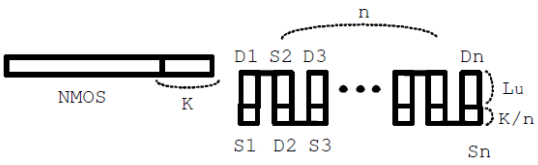


Fig. 3.10: Layout solution for the αV_{th} extractor.

For the αV_{th} extractor design, the technique to control the continuous α value is shown in Fig. 3.10. A transistor size of $L_u + K/n$ is used as a new unit transistor, where $L = nL_u + k,\ 0 < k < L_u$. Here, the change in unit transistor size is slight.

3.3 Simulation results

The proposed V_{th} extractor circuits shown in Figs. 3.1 and 3.5 have been designed using a standard CMOS 0.18 um technology and are verified by using the circuit simulator HSPICE. All the bodies of transistors are connected to their sources.

Case 2 is selected in Table 4 for the design of the unit αV_{th} extractor circuit. From these transistor sizes, the following parameter values are obtained by Eq. (39): a=0.25, b=0.5, $\frac{S_{M2}}{S_{M3}} = 6$ and $\frac{V_{ov2}}{V_{th}} = 0.285$. A post-layout simulation is done. The common centroid layout in Fig. 3.9 is used. Its area of NMOS transistors is 90 um*115 um, and the total layout area including PMOS transistors is about 110 um*115 um.

The simulation result of V_{ov2} for transistor M_2 is 0.149 V. According to Eq. (37) a

.

3.3.1 Unit V_{th} extractor simulation results

- **Comparison of V_{thM2} and the output value at temperature from 0 C° to 100 C°**

In Fig. 3.11, simulation results of the output reference voltage V_{out} versus the V_{thM2} for a temperature ranging from 0C° to 100C° is shown. The temperature sensitivity defined in Eq. (43) is 0.022%/C° in this range.

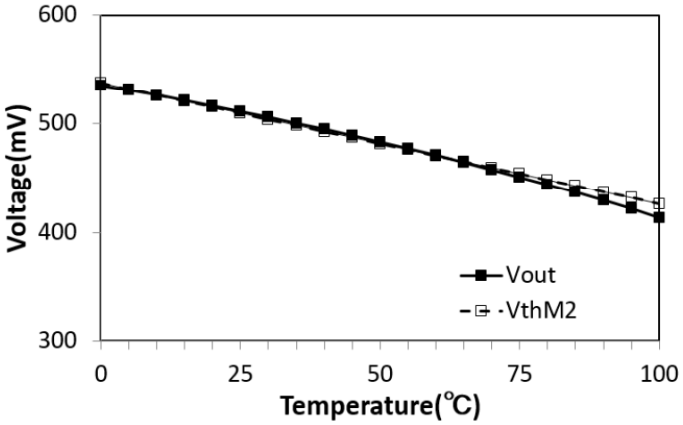
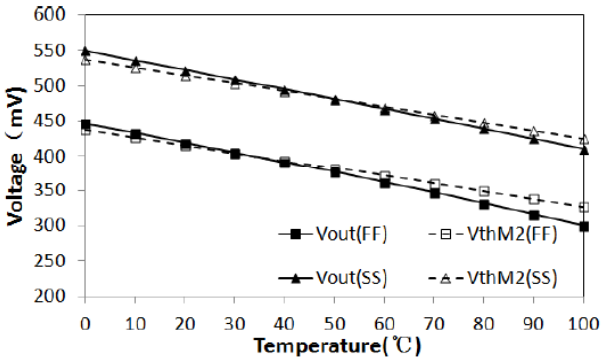


Fig. 3.11: Comparison of V_{thM2} and extracted unit V_{th} extractor output voltage (V_{out}) value at temperature range from 0C° to 100C°.

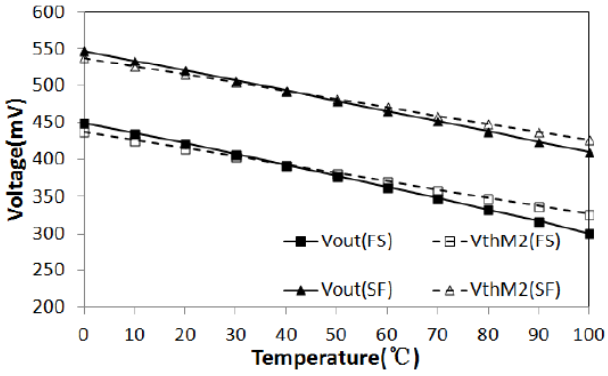
- **Comparison of TT, FF, SS value at different temperature**

The corner analysis errors have also been simulated. Fig. 3.12 shows a comparison of V_{out} and V_{thM2} at FF, SS, FS and SF values for a temperature range of 0C° to 100C°. Errors defined by Eq. (60) a lows. Compared with V_{thM2}, the errors are 0.03% (TT), 0.69% (FF), 0.6% (SS), 0.56% (FS) a .41% (SF) at room temperature. The worst case errors are, 4.76% (FF), 2.16% (SS), 4.64% (FS) a (SF) for a temperature ranging from 0C° to 100C°. These errors are caused by the influence of a leakage current. The calculation function is as follows:

$$\text{Error} = \frac{V_{out} - V_{thM2}}{average(V_{out})}. \quad (60)$$



(a)



(b)

Fig. 3.12: Comparison of the corner value of output voltages and V_{thM2} at temperature range from 0C° to 100C°, (a) FF and SS values, (b) FS and SF values.

- **Monte Carlo simulation for local variation**

To consider the influence of the mismatch, the local variation simulation has been done. The value of $\sigma(V_{out} - V_{thM2})$ was 0.41% for 1000 times Monte Carlo simulations, in which σ is the standard deviation of the output voltage V_{out} minus V_{thM2}.

- **Output voltage of different supply voltages at different temperature**

The output voltage of the proposed circuit versus the power supply voltage V_{DD} at

different temperatures is shown in Fig. 3.13. The minimum supply voltage for stable output voltage is 1.6 V. The unit threshold voltage of CMOS transistor is extracted with 0.027%/V supply sensitivity for power supply range of 1.6 V-2 V. To compare fairly with the other conventional results, the accuracy is also divided by the range of the available supply voltage. The calculation function is as follows:

$$Sensitivity_{\_V_{DD}} = \frac{\max(V_{out}) - \min(V_{out})}{average(V_{out})(V_{DD\_max} - V_{DD\_min})}. \quad (61)$$

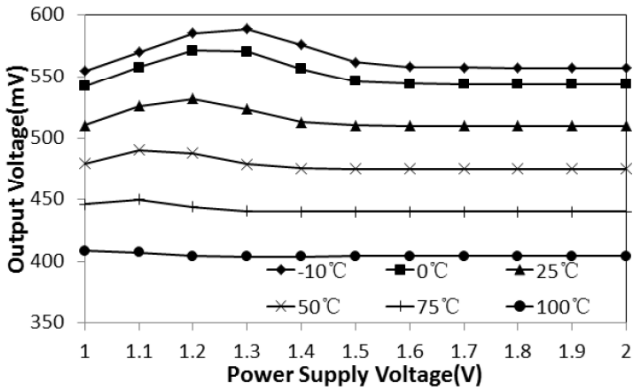


Fig. 3.13: Output voltages of different supply voltages at different temperatures.

- **Power consumption at different temperatures**

In Fig. 3.14, the power consumption at different supply voltages is simulated. The V_{th} extractor operates with 265 nW power consumption at $V_{DD} = 1.6$ V.

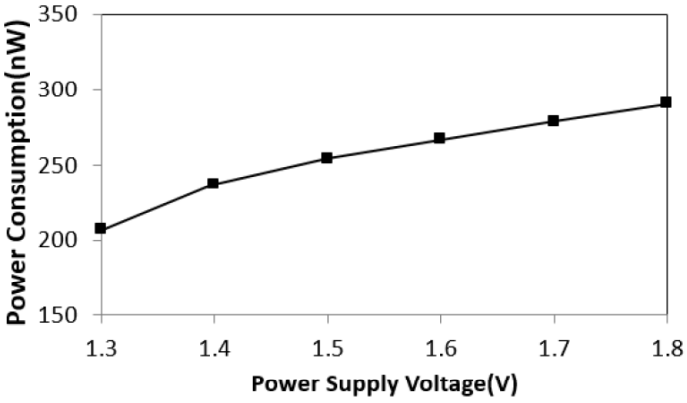


Fig. 3.14: Power consumption of different supply voltages.

- **Simulated noise spectrum**

Figure 3.15 shows the simulation results of the noise spectrum. The noise is 0.88 uV/sqrt Hz at 100 Hz with an error of 0.28%. This is smaller than the mismatch error. According to Table 4, the noise error increases when the *L*=*W* ratios become large. If the length is larger than that in case 2, the power consumption is reduced and the mismatch is smaller, however, noise increases and becomes a key influence. The sizes in case 2 is chosen to realize nanopower consumption and each error smaller than 1%.

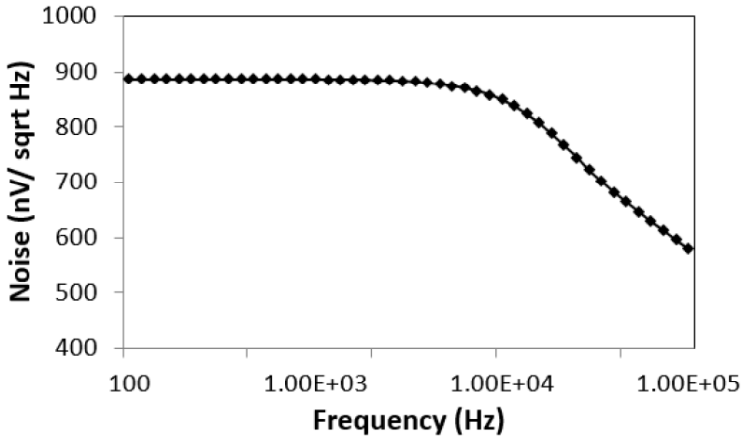


Fig. 3.15: Simulated noise spectrum.

3.3.2 αV_{th} extractor simulation results

The α values are calculated as follows: $\alpha_1 = 2.57$, $\alpha_2 = 1.285$, $\alpha_3 = 2.855$, $\alpha_4 = 1.285$. The dimension is same as unit V_{th}. The value of the bias voltage V_1 is equal to the supply voltage 1.8 V.

- **Comparison of V_{ref0}, V_{ref1}, V_{ref2}, V_{ref3} and V_{ref4} at different V_{thM2} values**

Figure 3.16 shows the dependence of the output voltages V_{ref0}, V_{ref1}, V_{ref2}, V_{ref3} and V_{ref4} on V_{thM2}. In the simulation, temperature is changed to sweep different V_{thM2}.

According to temperature dependence, the V_{thM2} values within the range from 0.35 V to 0.65 V are obtained together with the output voltages. Each variation is linear but with different slopes. Comparison with calculated α is as follows: The variation of V_{ref0} is almost the same as the variation of V_{thM2} value, that means V_{ref0} extracts a reasonable V_{th} value for the circuit. The output voltages V_{ref1}, V_{ref2} and V_{ref3} increase when V_{thM2} increases, and the slopes are different. They are determined by the value of α (α_1, α_2 for V_{ref1}, V_{ref2} and α_3 for V_{ref3}). The output voltage V_{ref4} decreases when V_{thM2} increases, because $V_{ref4} = V_1 - \alpha_4 V_{th}$. The errors of the slopes for V_{ref0}, V_{ref1}, V_{ref2}, V_{ref3} and V_{ref4} compared with calculated α values are 0.13%, 0.67%, 0.31%, 1.42%, and 2.82%, respectively.

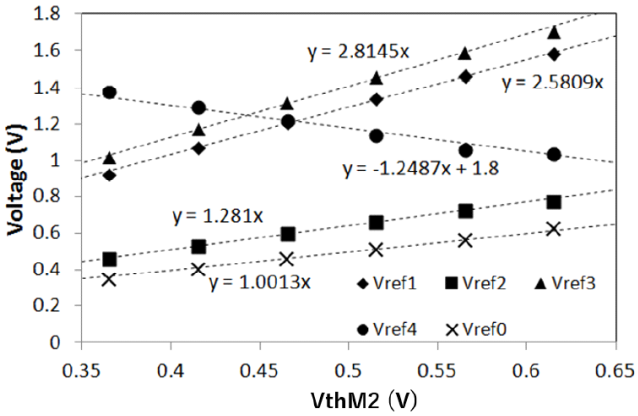


Fig. 3.16: Comparison of output voltages V_{ref0}, V_{ref1}, V_{ref2}, V_{ref3} and V_{ref4} at different V_{thM2} values.

- **Comparison of V_{ref0}, V_{ref1}, V_{ref2}, V_{ref3} and V_{ref4} at different S_{M2} over S_{M3} ratios**

Figure 3.17 is the simulation results of the output voltages V_{ref0}, V_{ref1}, V_{ref2}, V_{ref3} and V_{ref4} at different $\frac{S_{M2}}{S_{M3}}$ ratios. The unit V_{th} extractor output voltage V_{ref0} has almost no dependence on $\frac{S_{M2}}{S_{M3}}$. The αV_{th} extractor output voltages V_{ref1}, V_{ref2}, V_{ref3} and V_{ref4} are determined by the value of $\frac{S_{M2}}{S_{M3}}$, which means that the α value is controlled by adjusting

$\frac{S_{M2}}{S_{M3}}$.

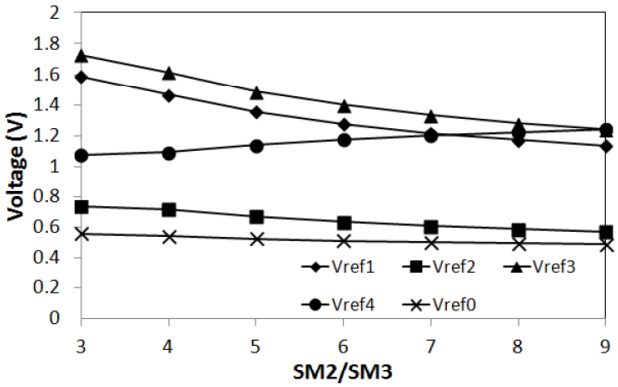


Fig. 3.17: Comparison of output voltages V_{ref0}, V_{ref1}, V_{ref2}, V_{ref3}, and V_{ref4} at different S_{M2}/S_{M3} ratios.

- **Comparison of simulation and theoretical output voltages of V_{ref3} and V_{ref4}**

Figure 3.18 shows V_{ref3}, which is incremental with the V_{th} temperature performance, and V_{ref4}, which is decremental with the V_{th} temperature performance. Both temperature variations of the two output voltages are linear. The calculated values of V_{ref3} and V_{ref4} are obtained according to the Eqs. (54) a (57), V_{thM2} value and the transistor sizes, respectively.

- **Output voltage of V_{ref3} at different supply voltages**

Fig. 3.19 shows the V_{ref3} versus the supply voltage V_{DD}. The minimum supply voltage is 1.6 V for V_{ref3}. The supply sensitivity is 0.146%/V. The accuracy is not as good as in the unit V_{th} extractor shown in Fig. 3.13, but similar level of conventional circuits. The reason is that the output voltage of the unit V_{th} extractor is not dependent on the overdrive voltage, while the α times V_{th} extractors are dependent both on the transistor V_{th} and the overdrive voltages.

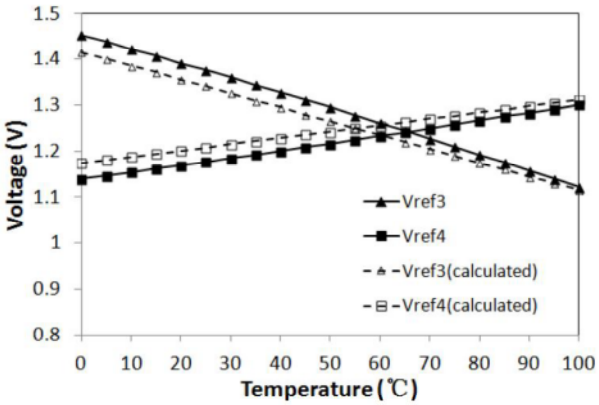


Fig. 3.18: Comparison of simulation and calculated output voltages of V_{ref3}, and V_{ref4} at temperature range from 0C° to 100C°.

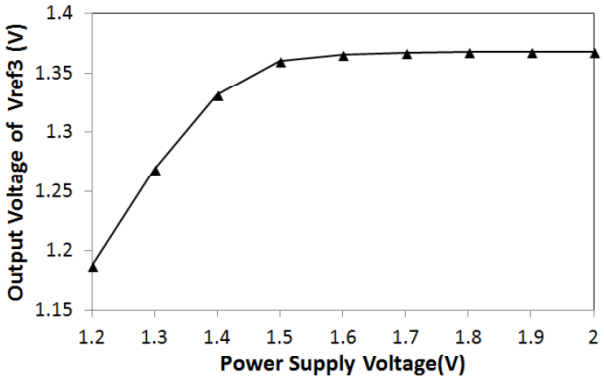


Fig. 3.19: Output voltage of V_{ref3} at different supply voltages.

3.3.3 Comparisons

The simulation results are compared with the results from conventional low power design unit V_{th} extractors [1][2] and an n times design V_{th} extractor [3].

Table 5 shows the comparison with the conventional unit V_{th} extractors [1][2]. It is inferred that the proposed circuit realizes an accurate output voltage V_{out} at the 265 nW consumption level, which is approximately 1/5 of that in [2] and 1/200 of that in [1]. Output voltage V_{out} sensitivity to V_{DD}, which is only 0.027%/V sensitivity, that is

approximately five times smaller than the results in both [1] and [2].

Table 5: Performance comparisons (unit V_{th} extractors).

	This work	[1]	[2]
Technology (um)	0.18	0.35	0.8
Supply voltage (V)	1.6-2	1-3.6	2-5
V_{out} sensitivity to V_{DD}	0.027%/V	0.12%/V	0.10%/V
V_{out} sensitivity to temp.	0.022%/℃	-	-
TT error (25℃)	0.03%	-	-
FF error (25℃)	0.69%	3.20%	-
SS error (25℃)	0.60%	-	-
FS error (25℃)	0.56%	-	-
SF error (25℃)	0.41%	-	-
Power Comsumption	265 nW	50 uW	1.14 uW
Noise (uV/sqrt Hz)	0.88	-	-

Table 6: Performance comparisons.

	This work	[3]
Technology (um)	0.18	3
Supply voltage (V)	1.6-2	5
V_{out} sensitivity to V_{DD}	0.146%/V (at α=2.855)	N/A
α times application	Continuous	Integer
Bias	Self-biased	Bias voltage needed

Table 6 shows the comparison with the conventional n times V_{th} extractor [3]. The merit of continuous α times V_{th} output voltage is achieved. The power consumption is greatly reduced to several nano-Watt or micro-Watt. Moreover, the αV_{th} extractor is self-biased while the circuit in [3] requires bias voltage.

3.4 Measurement results

The proposed circuit is designed under 0.18 um process technology. The chip

photograph of the proposed circuit without resistors is shown below in Fig. 3.20:

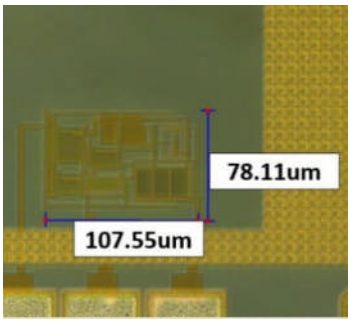


Fig. 3.20: The chip photograph of the proposed V_{th} extractor circuit without resistors.

Table 7: Transistor sizes of chip design.

MOS transistors	W (um)	L (um)
M_1	0.5	4
M_4	1	4
M_5	0.25	4
M_2	0.18	110
M_8	0.18	440
M_9	0.18	110
M_3	0.18	790
M_6	0.18	100
M_7	0.18	110

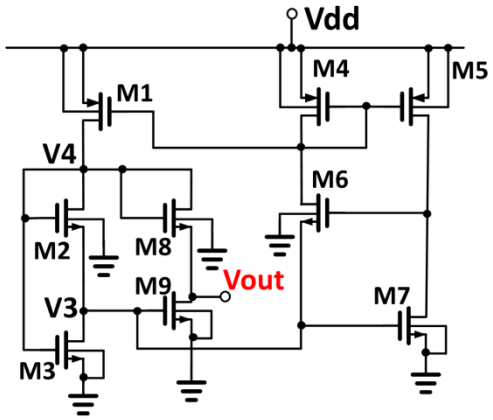


Fig. 3.21: Circuit structure of chip design with NMOS bodies connected to ground.

As shown in Fig. 3.20, the total chip area is about 0.008 mm^2. In this chip design, although case 2 is the best one considering the tradeoff of each performance, for the limitation of chip area, case 1 is chosen in practical design without common centroid layout. The transistor sizes are as shown in Table 7, similar as case 1 in Table 4, the area is small while the variation increases. In Fig. 3.21, for practical chip design, the bodies of each NMOS transistors are connected directly to the ground. In the simulation, NMOS bodies are connected to the source. In this case, the measurement results are influenced by the body effect.

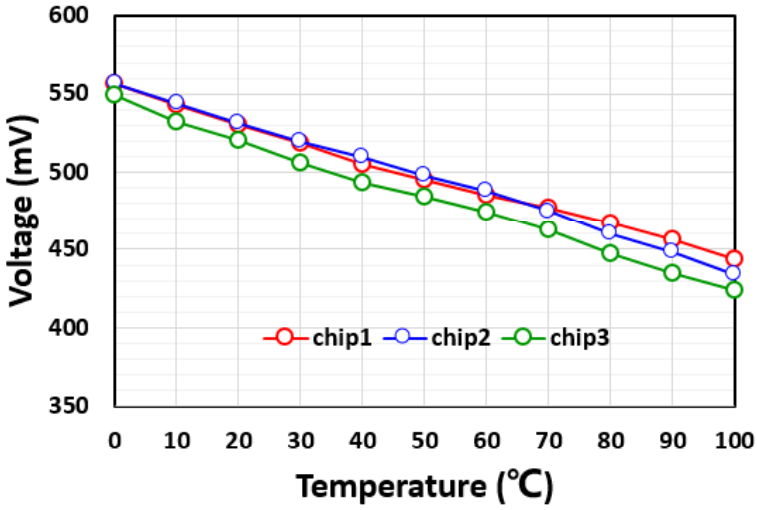


Fig. 3.22: Measurement results of extracted unit V_{th} output voltage (V_{out}) value for 3 different chips.

Figure 3.22 shows the measurement results of extracted unit V_{th} extractor output voltage (V_{out}) value at temperature range from 0C° to 100C° of 3 chips. The measured variation of output voltage is about 115 mV for average, and the simulation result is about 113 mV, which have a good agreement. The maximum variation between these 3 chips is about 15 mV at 100C°.

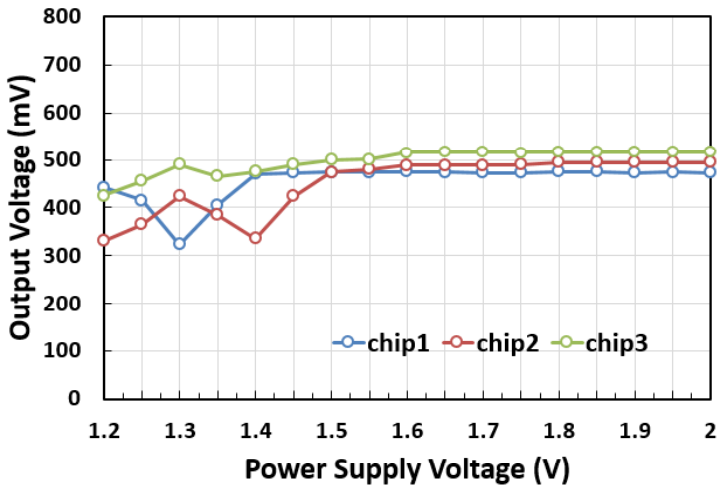


Fig. 3.23: Measurement results of output voltages of different supply voltages for 3 different chips.

The supply voltages dependences of output voltages are measured as shown in Fig. 3.23 from 3 different chips. The sensitivity is around 1.57%/V for the average performance of chip 3. Comparing with the simulation result of 0.027%/V, the measurement is worse than the simulation result.

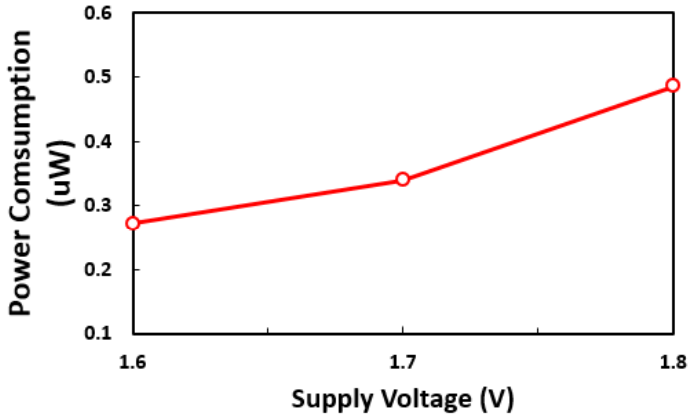


Fig. 3.24: Measure results of power consumption at different supply voltages.

Figure 3.24 shows the measurement results of power consumption at supply voltages from 1.6 V to 1.8 V. The power consumption is succeeded to realize nano-level. The

measured power consumption results are 432 nW at $V_{DD} = 1.6$ V. Comparing with the simulation results of 265 nW at $V_{DD} = 1.6$ V in Fig. 3.14, the measured power is a little increased caused by noise and leakage current.

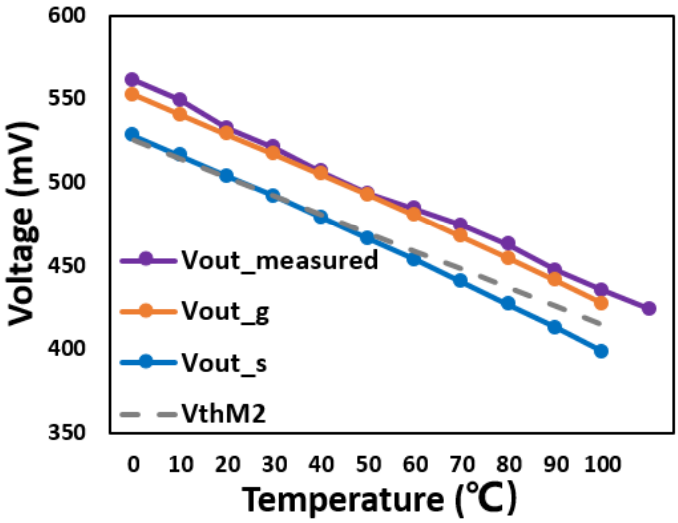


Fig. 3.25: Simulation and measurement comparison of temperature variation.

The influence of body effect is discussed using HSPICE simulation. The output V_{out_s} is shown in Fig. 3.1 with NMOS bodies connected to source, and output voltage V_{out_g} is shown in Fig. 3.21 with NMOS bodies connected to ground. Together with the measurement result $V_{out\_measured}$ and the typical V_{th} value V_{thM2}, the comparison of temperature is shown in Fig. 3.25. The applied transistor sizes of these two circuits are shown in case 1 from Table 4. V_{out_s} has small difference of only 0.036%/C° comparing with typical value V_{thM2}. When body connected to ground, both the V_{out_g} and $V_{out\_measured}$ value turns about 25.1 mV larger than V_{thM2} at room temperature, and the error is 0.087%/C° and 0.091%/C°, respectively. This is caused by body effect, for the source-to-body voltages are different from each transistor and their V_{th} value also different.

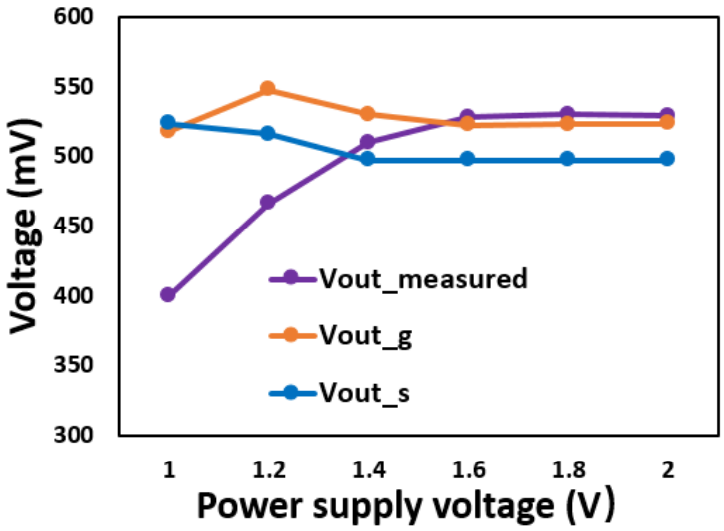


Fig. 3.26: Supply voltage dependence comparisons.

Figure 3.26 shows the comparison of supply voltage between V_{out_g}, V_{out_s} and $V_{out\_measured}$, respectively. As discussed, the V_{out_s} has a high accuracy of 0.027%/V. The measurement data $V_{out\_measured}$ shows that, the practical supply voltage dependence is large (around 1.57%/V). In this figure, the supply voltage dependence of V_{out_g} is 0.135%/V, which is 5 times larger than that of V_{out_s}. From these results, the body effect is one of the reason that make the measurement supply dependence large.

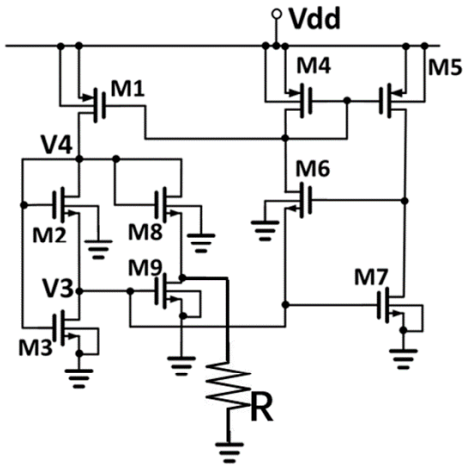


Fig. 3.27: Structure for loading effect simulation.

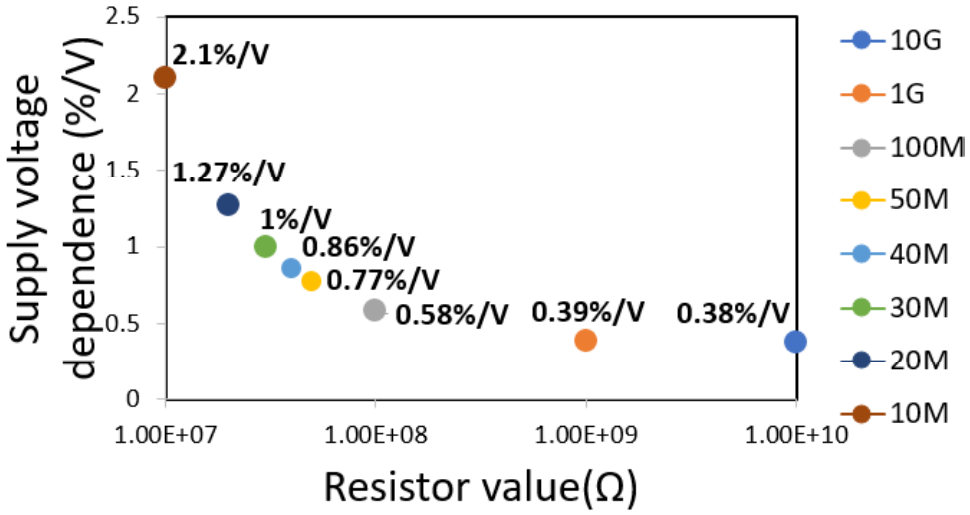


Fig. 3.28: Supply voltage dependence at different load resistances.

Although body effect has influence on the supply voltage dependence, the measured result still much larger than simulation. Considering the large output impedance, the load effect is also simulated. In Fig. 3.27, a resistor is connected to the output node, which is used to simulate the load input resistance. In Fig. 3.28, it is obvious that, the supply voltage becomes worse when resistor value becomes small. At R=10 MΩ, the supply voltage dependence is around 2.1%/V. At R=20 MΩ, the supply voltage dependence is around 1.27%/V. The measurement result of 1.57%/V is between these two results. This means the practical load resistance is between 10 MΩ and 20 MΩ. The voltage meter input resistance is 10 MΩ according to the manual, which agrees with the load effect simulation. Based on these results, the measurement result is greatly influenced by the loading effect.

3.5 Summary

In this chapter, unit and α times V_{th} extractors are proposed by overdrive voltage control technique.

For unit V_{th} extractor, the performance of nano-level power consumption and supply-insensitivity are achieved. Low power is realized by using long channel length transistors and optimized small V_{ov}. Supply voltage independence is realized by using long channel length and αV_{ov} compensation of NMOS transistor each other. According to post-layout simulation of unit V_{th} extractor based on a CMOS 0.18 um process, the threshold voltages of the CMOS transistors is extracted with 0.027%/V power supply sensitivity. For measurement results, the power supply sensitivity is 1.57%/V. The difference is mainly caused by the large output impedance of the circuit. Simultaneously, it operates with a nanopower consumption of 265 nW, comparing with 432 nW of measurement results.

For the αV_{th} extractor, both incremental and decremental V_{th} extractors are proposed. The continuous α is achieved by changing W/L ratios. This αV_{th} extractor operates from nano-Watts to several micro-Watts.

Overall, the obtained improvements meet the demand for portable devices operating with very low power consumption and large supply voltage variations.

4 A 3.5 ppm/C° 0.85 V Bandgap Reference Circuit without Resistors by Using a Voltage Divider and a CTAT Current Source

4.1 Introduction

The voltage reference is one of the important blocks, which is widely used in almost all LSI systems. The generated voltage is independent of variation caused by PVT (Process, Voltage, and Temperature) variation. The bandgap reference is one of the most popular reference voltage generators in analog and mixed digital systems [4][5]. In order to be implemented with the digital VLSI circuits, standard CMOS process becomes more and more popular for design this kind of circuit [6][12] - [19].

With the emergence of sub-micron CMOS process, low power consumption and low power supply voltage have become two important design topics in both digital and analog systems. In the near future, the system work under 1 V supply voltage is expected [6]. Moreover, the reduction of the minimum feature size of MOS transistors also reduces the supply voltage of VLSI. Thus, reducing supply voltage of BGR is strongly required. As a result, several BGR circuits working with supply voltages near or even below 1 V have been proposed in recent years [6][12] – [19] by using resistors.

However, BGR circuits with resistors in a standard CMOS process increases the chip area, which means the increase of cost. Especially in the low power designs, much larger

resistance is needed and the area of resistors increases significantly. Therefore, the BGR circuits without resistors become more attractive and many circuits have been proposed [7] [10][11] [19].

Although many BGR circuits without resistors have been proposed, some problems still exist. Due to the BGR value (1.25 V) a

. The large minimum supply voltage is a limit factor for low voltage applications. Therefore, in this paper, a sub-1-V CMOS bandgap voltage reference generator circuit without resistors is proposed. The improvements of the proposed circuit are below:

1. A CMOS only BGR circuit which is implemented without resistors, is capable to operate under 1 V supply voltage. The 0.85 V supply voltage is achieved by utilizing a voltage divider.
2. The temperature coefficient is improved. Original BGR circuits with resistors have small temperature dependence. However, the BGR circuit without resistors [7] has much larger temperature dependence caused by that of current source. This improvement is realized by a current source with approximately linear negative temperature variation. Its temperature dependence is compensated by only adjusting the *W/L* ratios of the two differential pairs in the BGR circuit. Thus, the temperature coefficient is reduce to about 3.5 ppm/C°.

Simulation results show that the output reference voltage V_{ref} is achieved around 0.5 V with a minimum supply voltage of 0.85 V. Moreover, the temperature coefficient of the output voltage is only 3.5 ppm/C° from 0C° to 70C°.

4.2 Principle of conventional CMOS bandgap reference circuits

A bandgap voltage reference generator is a circuit that independent of the PVT variation. The output voltage is commonly 1.25 V without special technical design (close to the value 1.22 eV of the bandgap of silicon at temperature 0 K). The concept of this circuit is firstly designed by David Hilbiber in 1964 [57]. Other researchers like Bob Widlar and Paul Brokaw continued the work to improve the performance [4][5].

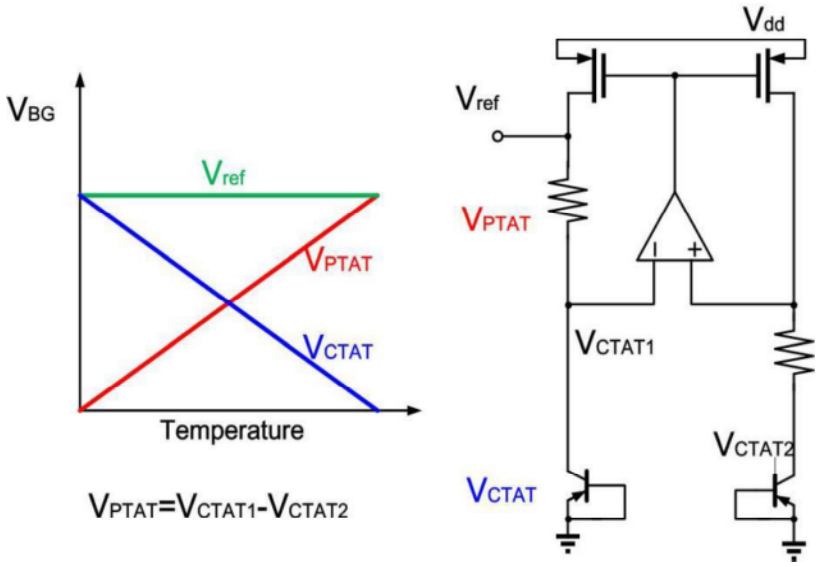


Fig. 4.1: The principle of bandgap reference circuit [5].

Bandgap reference voltage is realized by a proportional to absolute temperature voltage *Vptat* and a complementary to absolute temperature voltage *Vctat* to compensate temperature dependence each other as shown in Fig. 4.1. The CTAT voltage is generated by the *p*-*n* junctions (e.g. diodes). The PTAT voltage is generated using voltage difference between the two *p*-*n* junctions, which operated at different current densities.

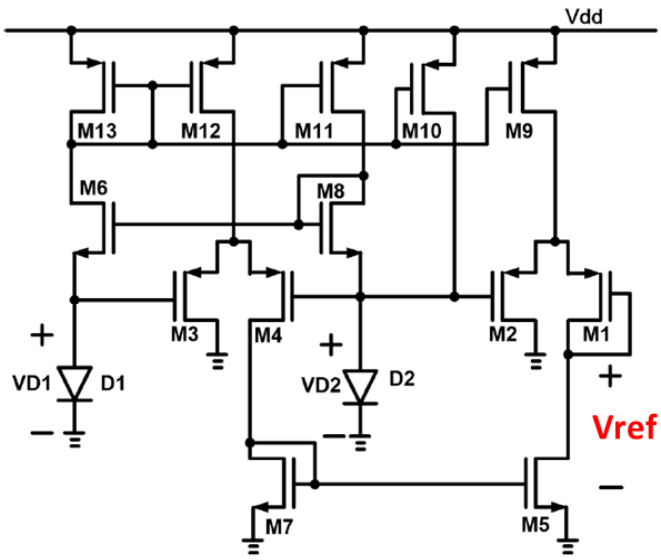


Fig. 4.2: The conventional bandgap reference circuit without resistors in [7].

A well-known BGR circuit without resistors was proposed [7] based on the similar bandgap reference principle [4]. Figure 4.2 shows the structure of the circuit in [7]. The current source together with current mirrors is composed of transistors M_6, M_8, M_9, M_{10}, M_{11}, M_{12} and M_{13}. The voltage to current transconductor and the current to voltage transresistor are realized by the differential pairs M_3-M_4 and M_1-M_2, respectively. The current feedback is composed of transistors M_5-M_7.

According to the principle of the BGR, the voltage $V_{D2} - V_{D1}$ has the relationship,

$$V_{D2} - V_{D1} = \theta V_T, \tag{62}$$

w

—). Then it

is delivered to the current to voltage transresistor. According to Fig. 4.2, the output reference voltage V_{ref} is expressed in the principle equation,

$$V_{ref}(conv.) = V_{D2} + \alpha(V_{D2} - V_{D1}). \tag{63}$$

Assuming infinite output impedance and the simple square-law model for a MOS device, the value of α is equal to $\sqrt{AG}$ (A is determined by the transistors M_1, M_2, M_3 and M_4, where $A = \frac{S_{M3}}{S_{M2}} = \frac{S_{M4}}{S_{M1}}$). This results into,

$$V_{ref}(conv.) = V_{D2} + \sqrt{AG}(V_{D2} - V_{D1}). \quad (64)$$

According to the transistor sizes in [7], $AG = 49$ is obtained, which is not very small. Thus, the transistor sizes need to be large, which makes the circuits area and the mismatch large.

This circuit has a limitation of very high supply voltage (3.7 V). In order to reduce the supply voltage, there are two methods. One method is to reduce the output voltage V_{ref} (To pull up V_{ref}, the minimum supply voltage should be larger than it.). The other one is to reduce the gate-to-source voltage value of each transistor. Based on the second method, the supply voltage is reduced to about 1.4 V with small current [11]. However, it is hard to reduce the minimum supply voltage below 1 V, because the output reference voltage value is around 1.25 V. In this paper, the first method is applied, which is capable to break the bottleneck of 1.4 V minimum supply voltage.

Another limitation of the conventional BGR circuit is that, the temperature dependence of the current source influences the reference voltage greatly. The output reference voltage temperature coefficient is reported 119.7 ppm/C°. The current value from the structure varies with the temperature irregularly, and this influences the accuracy of the output reference voltage.

In this paper, a CMOS BGR circuit is proposed by adding a CMOS voltage divider and an improved current source. The circuit is capable to work under sub-1-V supply voltage with small temperature coefficient.

4.3 The proposed low supply voltage CMOS bandgap reference circuit

A low temperature coefficient sub-1-V BGR circuit without resistors is proposed in this section. Subsection 4.3.1 introduces the principle of the BGR circuit without resistors working under sub-1-V supply voltage. Subsection 4.3.2 describes the circuit of BGR core and current source.

4.3.1 Principle of reducing the supply voltage

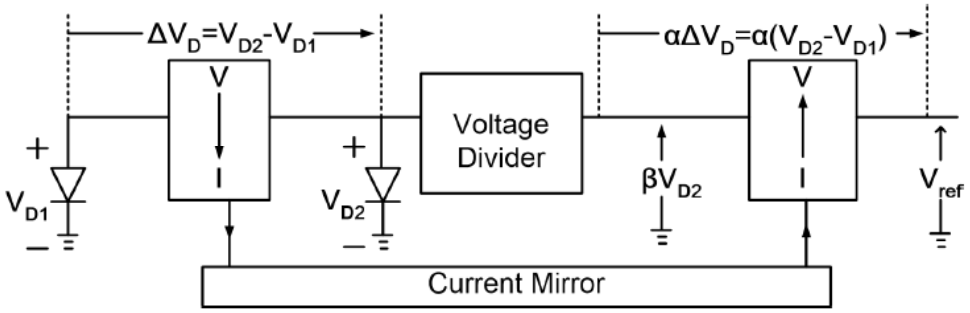


Fig. 4.3: The principle of the proposed BGR circuit without resistors.

To reduce the minimum supply voltage, a voltage divider is inserted between voltage to current transconductor and the current to voltage transresistor as shown in Fig. 4.3. By using this structure, following relationship is obtained,

$$V_{ref}(prop.) = \beta V_{D2} + \beta\alpha(V_{D2} - V_{D1}), \tag{65}$$

w

, as to be mentioned later by Eq. (73). Then, Eq. (65) is also presented as,

$$V_{ref}(prop.) = \beta V_{D2} + \sqrt{AG}(V_{D2} - V_{D1}). \tag{66}$$

Because V_{D2} in the conventional BGR circuit [7] is a constant value, the output voltages of the conventional BGR circuits are about 1.25 V, which limit the value of power supply voltage. The value of V_{D2} is much larger than the value of $V_{D2} - V_{D1}$, and V_{D2} cannot be adjusted by the MOS transistor *W/L* ratios. In the proposed circuit, β is a variable factor and is capable to be designed such as 1/2 according to requirements. The βV_{D2} is adjusted close to the value of $V_{D2} - V_{D1}$, so that $\beta\alpha$ in Eq. (65) or $\sqrt{AG}$ in Eq. (66) to compensate the temperature dependence is reduced from $\sqrt{AG}$ in Eq. (64). The total output reference voltage is reduced. According to the value of V_{D2} and $V_{D2} - V_{D1}$ in the conventional BGR, the value of *AG* is equal to 49 in [7]. After adding the parameter β ($\beta = 1/2$ in the proposed circuit), the *AG* value is reduced to about 12.

As the output reference voltage value in the proposed circuit has ability to be adjusted much smaller, the output reference voltage is reduced greatly and the minimum supply voltage is reduced to sub-1-V.

Since the value $\sqrt{AG}$ in the proposed circuit is reduced, the ratios of transistor sizes of the two differential pairs and current mirrors turn small. In this case, the circuit area is much smaller than the conventional circuit. Moreover, the ratios of *W/L* sizes of the two differential pairs and current mirrors become much close to each other. The main branch current ratio of diodes D_1 and D_2 is 1:1 (chosen to reduce the current mirror mismatch), and the diodes area ratio of D_1 and D_2 is 10:1. Thus, the mismatch is reduced. In this way, the performance is improved.

When $\beta = 1$, Eq. (66) is same as Eq. (65). Therefore, it is said that the conventional circuit structure [7] is just a special case of the proposed circuits.

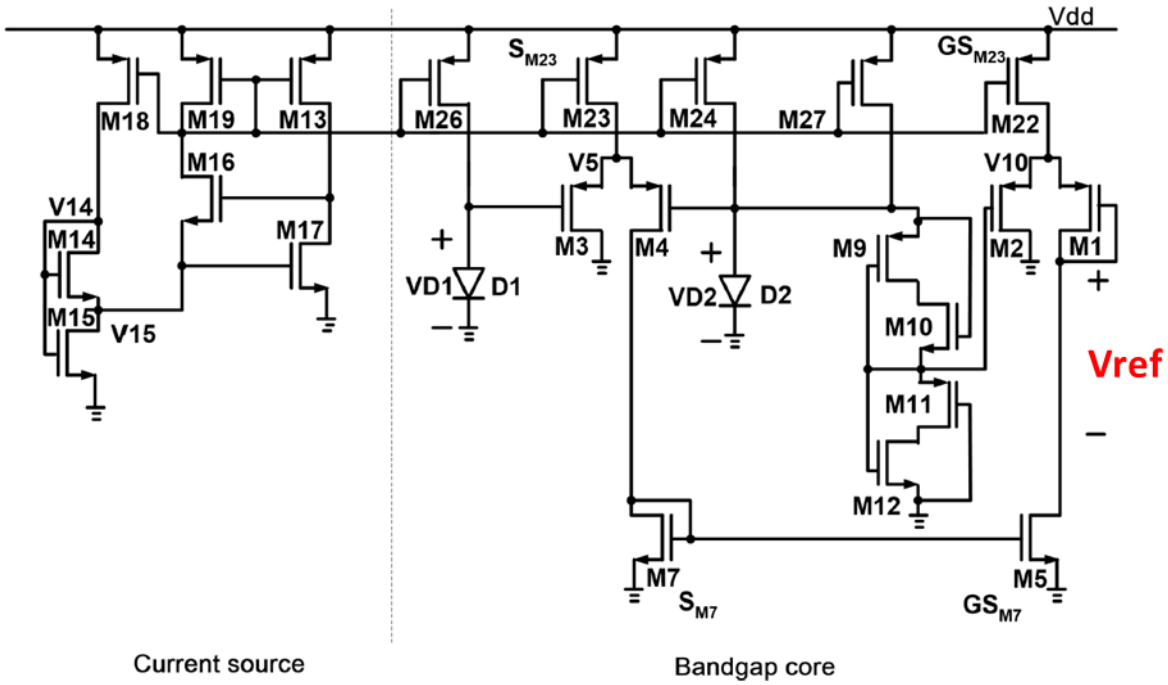


Fig. 4.4: The structure using all CMOS transistors in chip design.

Based on this principle, the voltage divider is applied and the constant AG and β in Fig. 4.4 are determined by the following analysis.

4.3.2 Circuit structure

A new BGR circuit is proposed in this section. BGR core with the voltage divider is expressed in the first part, and a new current source circuit that is capable to adjust the temperature dependence of BGR circuit is explained in the second part.

- **BGR core**

Figure 4.4 shows a proposed BGR circuit without resistors. The transconductor and transresistor of the proposed circuit are realized by two differential pairs. The parameter A and G are the same as previous section. For the two current mirrors, the W/L ratio of

transistor M_{22} (marked as GS_{M23} in Fig. 4.4) is G times larger than the W/L ratio of the transistor M_{23}; the W/L ratio of transistor M_5 (marked as GS_{M7} in Fig. 4.4) is G times larger than the W/L ratio of the transistor M_7.

The voltage divider includes a string of CMOS pairs of transistors (M_9, M_{10}) a (M_{11}, M_{12}), connecting their source-drain in series [58]. For each pair, the PMOS gate is connected to the NMOS source and the NMOS gate is connected to the PMOS source as shown in Fig. 4.4. The body of the CMOS transistors are connected to their sources. In this case, the I-V characteristics of CMOS pairs are identical. Thus, accurate tracking of the given source voltage V_{s9} of transistor M_9 is realized.

By using this voltage divider structure, the β is equal to $\frac{1}{2}$. For the current flowing through M_9 is only several pico Ampares, it can be totally ignored. In this case the currents flowing through transistors M_1, M_2, M_3 and M_4 have relationships below:

$$I_{M1} = GI_{M4}, \tag{67}$$

$$I_{M2} = GI_{M3}. \tag{68}$$

All the transistors M_1, M_2, M_3 and M_4 are operating in saturation region, thus the current functions are,

$$I_{M1} = \frac{1}{2}B\mu_P C_{ox} S_{M1}(V_{10} - V_{ref} - |V_{thP}|)^2, \tag{69}$$

$$I_{M2} = \frac{1}{2}B\mu_P C_{ox} S_{M2}(V_{10} - \frac{1}{2}V_{D2} - |V_{thP}|)^2, \tag{70}$$

$$I \quad -B\mu_P C_{ox} S_{M3}(V_5 - V_{D1} - |V_{thP}|)^2, \tag{71}$$

$$I_{M4} = \frac{1}{2}B\mu_P C_{ox} S_{M4}(V_5 - V_{D2} - |V_{thP}|)^2, \tag{72}$$

w -oxide capacitance, and S_{M1}, S_{M2}, S_{M3} and S_{M4} are the W/L ratios of transistors M_1, M_2, M_3

and M_4, respectively. The parameter B is the W/L ratio of the two differential pairs M_1-M_2 and M_3-M_4 (w $\frac{}{} = \frac{S_{M4}}{S_{M3}}$). Also, V_5 and V_{10} are the source voltages of the transistors M_3-M_4 and M_1-M_2 shown in Fig. 4.4.

According to Eqs. (67)-(72), the output reference voltage is finally obtained as,

$$V_{ref} = \frac{1}{2}V_{D2} + \sqrt{AG}(V_{D2} - V_{D1}). \quad (73)$$

The value of $\frac{1}{2}V_{D2}$ is half of the conventional one. To make the mismatch smaller, the parameter A is set to 1. To compensate the temperature dependence, $\sqrt{G}$ is also reduced for one half of $\sqrt{AG}$ in Eq. (66).

The approximated relationship between the proposed BGR circuit and the conventional BGR circuit is shown below,

$$V_{ref}(prop.) = \frac{1}{2}V_{ref}(conv.). \quad (74)$$

Thus, the minimum supply voltage for the proposed BGR is greatly reduced.

- **Current source**

A new current source circuit without resistors that is capable to adjust the temperature dependence of BGR circuit is developed. It also improves PSRR (Power Supply Rejection Ratio).

The assumption for the BGR circuit without resistors is to use the ideal current source. However, the current source applied in [7] varies with the temperature irregularly, which has great influence to the BGR voltage temperature dependence.

Also, a current source circuit satisfying both temperature coefficient $T_C = 0$ and high PSRR is complicated in general. Such current source is not necessarily needed. Because if the temperature coefficient of a current source $T_C = \emptyset$ ($\emptyset$ is a constant), its

effect on temperature dependence of the output voltage is compensated by tuning *G* value. This also make the design simple.

A linearly temperature dependent current source is shown in the left part of Fig. 4.4, which consists of transistors M_{13}, M_{14}, M_{15}, M_{16}, M_{17}, M_{18} and M_{19}. The transistors M_{14} and M_{17} are in saturation region, and M_{15} in linear region. They have the current functions:

$$I_{M14} = \frac{1}{2}\mu_N C_{ox} S_{M14}(V_{14} - V_{15} - V_{th})^2, \tag{75}$$

$$I \qquad\qquad - V_{th} - \frac{1}{2}V_{15})V_{15}, \tag{76}$$

$$I \qquad -\mu_N C_{ox} S_{M17}(V_{15} - V_{th})^2, \tag{77}$$

w

. 4.4.

It is assumed that $S_{M18} = S_{M19} = S_{M13}$, and $S_{M14} = S_{M17}$ to simplify the analysis of the proposed circuit. Then the current I_{M14} is equal to I_{M17} and,

$$V_{14} = 2V_{15}. \tag{78}$$

According to Eqs. (76)-(78),

$$V_{15} = \left[\frac{1-\lambda}{1-3\lambda} + \sqrt{\left(\frac{1-\lambda}{1-3\lambda}\right)^2 - \frac{1}{1-3\lambda}}\right] V_{th} = \gamma V_{th}, \tag{79}$$

w $\frac{S_{M15}}{+S_{M19}\,S_{M17}}$. The parameters λ and γ are constants determined by transistor sizes and are independent of process parameters. The output reference current is expressed as:

$$I_{ref} = I_{M17} = \frac{1}{2}\mu_N C_{ox} S_{M17}[(\gamma - 1)V_{th}]^2. \tag{80}$$

In Eq. (80), the mobility μ_N and the threshold voltage V_{th} have the temperature dependence:

$$\mu_N = K_u T^{-m}, \tag{81}$$

$$V_{th} = V_{th}(T_0) - a'(T - T_0), \tag{82}$$

w) a

. The diode branch voltage V_{DD}

is expressed in the diode equation shown as:

$$V_D = V_T \ln(\frac{I_{ref}}{I_S}), \tag{83}$$

w .

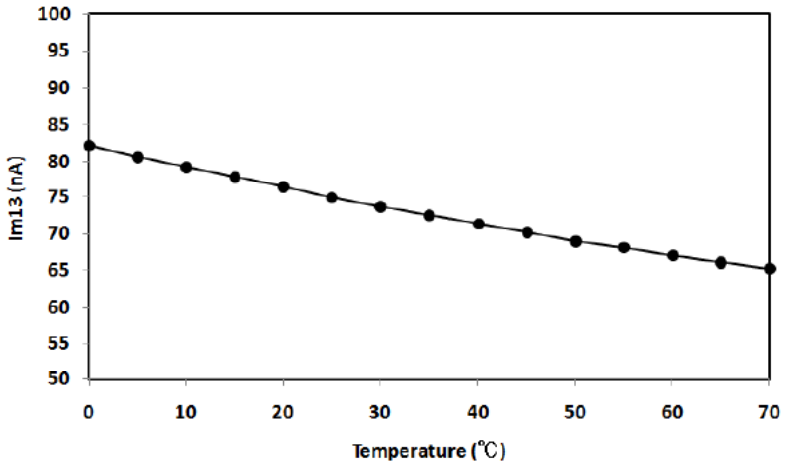


Fig. 4.5: The temperature variation of the proposed current source.

Figure 4.5 shows the temperature variation of the proposed current source. The current I_{m13}, which is applied as I_{ref} is simulated using the current flowing through the transistor M_{13}. The current I_{m13} has the negative temperature dependence, which is approximately linear.

According to Eq. (83), the negative temperature dependence of the current I_{m13} influences the value of the diode voltage V_D. Considering this temperature variation, the

V_D derivation of the temperature is shown below:

$$(\text{prop.})\frac{\partial V_D}{\partial T} = \frac{\partial V_T}{\partial T} ln \frac{I_{ref}}{I_S} - \frac{V_T}{I_S}\frac{\partial I_S}{\partial T} + \frac{V_T}{I_{ref}}\frac{\partial I_{ref}}{\partial T}, \tag{84}$$

$$\frac{V_T}{I_{ref}}\frac{\partial I_{ref}}{\partial T} = \frac{k}{q}\frac{3a'^2T^2-4a'\gamma'T+\gamma'^2}{(a'T-\gamma')^2}, \tag{85}$$

where q is the magnitude of the electrical charge on the electron, k is the Boltzmann's constant and $\gamma' = V_{th}(T_0) + a'T_0$. In (85), as $\frac{\partial V_T}{\partial T} ln \frac{I_{ref}}{I_S} - \frac{V_T}{I_S}\frac{\partial I_S}{\partial T} < 0$ (w

) and $\frac{k}{q}\frac{3a'^2T^2-4a'\gamma'T+\gamma'^2}{(a'T-\gamma')^2} < 0$,

so $(\text{prop.})\frac{\partial V_D}{\partial T}$ is still negative to the temperature variation.

The voltage difference $V_{D2} - V_{D1}$ is the positive temperature variation part in the BGR function, shown as,

$$V_{D2} - V_{D1} = V_T \ln(\frac{I_{S2}}{I_{S1}}). \tag{86}$$

The current source temperature variation has no influence to $V_{D2} - V_{D1}$ in the theory, so:

$$(\text{prop.})(V_{D2} - V_{D1}) = (\text{ideal})(V_{D2} - V_{D1}). \tag{87}$$

According to Eq. (84) a (87), the temperature dependence of the current source to the output reference voltage is compensated by adjusting the *W/L* ratios of the differential pairs (M_1, M_2) a (M_3, M_4), which satisfies the BGR relationship:

$$(\text{prop.})V_{ref} = \beta V_{D2} + \beta\alpha(V_{D2} - V_{D1}). \tag{88}$$

In this case, the current source temperature dependence is ignored, working as an ideal current source.

Current source constructed with M_{13}, M_{16}, M_{17} and M_{19} generally has good PSRR. Comparing with the reference current source in [7], the influence of the supply voltage variation to the output reference voltage is greatly reduced.

In the chip design, the transistors M_3 and M_4 are considered to be trimmed using a string of transistors with different W/L sizes, respectively. This technique is used to compensate the process variation especially for the parameter V_{th}.

Thus, the problem of current source temperature dependence is solved and the supply voltage dependence is reduced together, which greatly improves the accuracy of the output reference voltage.

4.4 Simulation results

Simulation has been done using a standard CMOS 0.18 um process. The two diodes D_1 and D_2 are actually formed with the PMOS transistors whose combined drain-gate-source act as anodes [7]. All the bodies of NMOS transistors are connected to ground, and PMOS transistors connected to V_{DD}. Firstly, the current flowing through the voltage divider structure is simulated. In the proposed circuit, it is designed very small comparing with the total current, so that the current is ignored. In Table 8, the simulation results of current I_{M9} flowing through transistor M_9 and the main branch (diode D_2) current I_{D2} are compared. The current I_{M9} is only several pico Ampere under different temperatures, while the current I_{D2} is several dozen nano Ampere level. Therefore, the current I_{M9} is negligibly small. That means there is almost no influence by ignoring the temperature dependence of the voltage divider structure current.

Table 8: The simulation results of current I_{M9} flowing through transistor M_9 and the main branch (diode D_2) current I_{D2}.

Temperature (℃)	ID2(nA)	IM9(pA)
0	82	77
25	75	94
70	65	126

The Monte Carlo simulation of the output voltage versus temperature for 100 times has been done. The Monte Carlo simulation includes both the global and local variation models in [53]. The shape of each line is similar for the 100 times Monte Carlo simulation. The average reference voltage at the room temperature is about 500 mV. Furthermore, the average value of V_{ref} temperature coefficient in the temperature range 0C° and 70C° is 3.76 ppm/C° and the standard deviation is 1.11 ppm/C° (3σ is 3.33 ppm/C°).

4.4.1 Minimum supply voltage

Figure 4.6 presents the simulated $V_{ref} - V_{DD}$ characteristics of the conventional and proposed circuits, respectively. In the conventional BGR circuit illustrated in Fig. 4.2, output reference voltage is 1.115 V, and the minimum supply voltage is 2.2 V. For the proposed BGR, the output reference voltage is 0.5 V. The simulated minimum supply voltage is 0.85 V. Comparing the simulation results of the proposed circuit and the conventional circuit, the minimum supply voltage is reduced of about 50%.

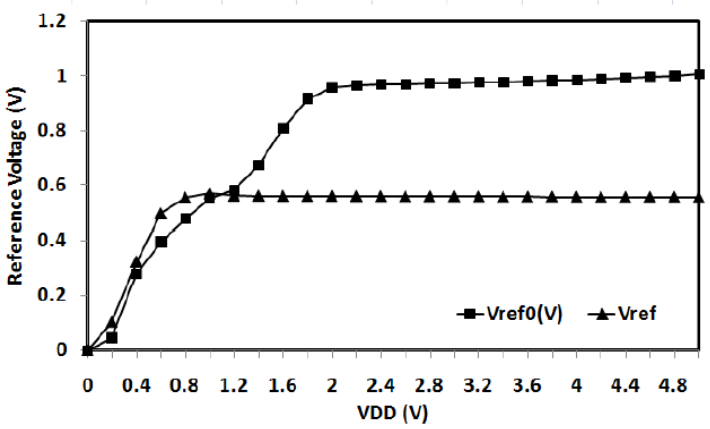


Fig. 4.6: Comparison of V_{DD} dependence: Conventional circuit (Fig. 4.2) and proposed circuit (Fig.4.4).

4.4.2 Temperature coefficient of reference voltage

Figure 4.7 shows the output voltage versus temperature with the temperature variation from 0C° to 70 C°. The average reference voltage is 0.5 V, which is almost half of the conventional BGR circuit in [7]. The temperature coefficient of the proposed circuit is improved to 3.5 ppm/ C°, compared with the 119.7 ppm/ C° temperature coefficient in [7].

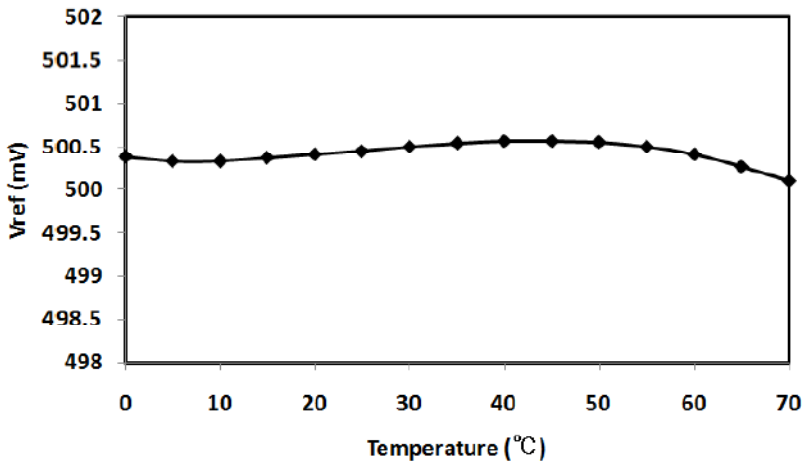


Fig. 4.7: The simulation results of the proposed circuit output reference voltage V_{ref} versus temperature.

4.5 Measurement results

The chip photograph of the proposed bandgap reference circuit without resistors is shown below in Fig. 4.8. All the bodies of NMOS transistors are connected to ground, and PMOS transistors connected to V_{DD}. The total chip area is about 0.026mm^2.

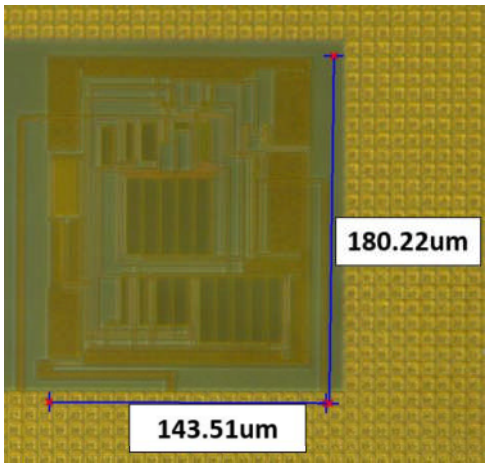


Fig. 4.8: The chip photograph of the proposed bandgap reference circuit without resistors.

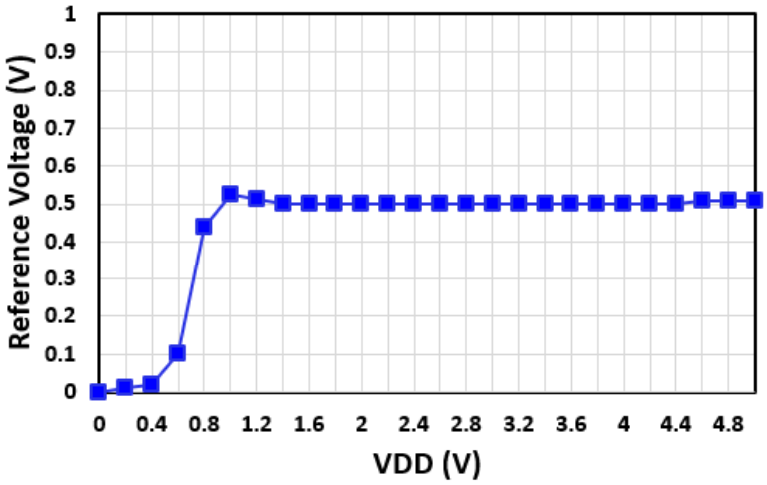


Fig. 4.9: The measurement results of the proposed circuit output reference voltage V_{ref} versus supply voltage.

Figure 4.9 presents the measurement $V_{ref} - V_{DD}$ characteristics of proposed circuit at room temperature. The output reference voltage is 0.5 V. Although the V_{DD} dependence is not very small during the V_{DD} range from 0.85 V to 1.2 V, the circuit is still under operation situation. The measured minimum supply voltage is 0.85 V, which

has a good agreement with the simulation results in Figure 4.6. The unstable range (V_{DD} from 0.85 V to 1.2 V) is caused by that, this range is closed to the minimum supply voltage of the CTAT current source.

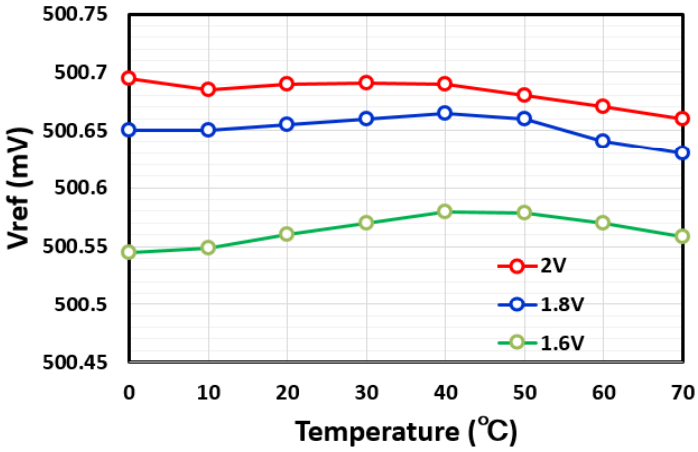


Fig. 4.10: The measurement results of the proposed circuit output reference voltage V_{ref} versus temperature (0C°-70C°).

Figure 4.10 shows the measurement results of the proposed circuit output reference voltage V_{ref} from temperature range of 0C°-70C°. The average reference voltage is 0.5 V, which has a good agreement with the simulation results in Fig. 4.7. The measured temperature coefficient of the proposed circuit is about 4.9 ppm/C°, compared with the 3.5 ppm/C° temperature coefficient of simulation results. This difference is caused by the variation that the middle points of temperature compensation moves in Fig. 4.10.

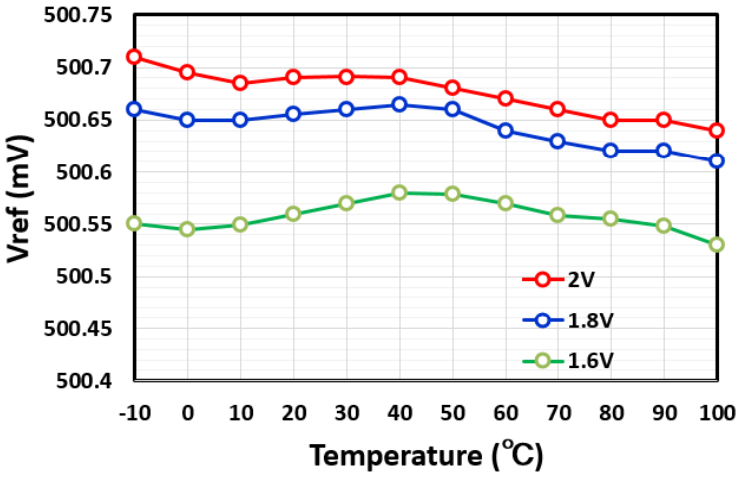


Fig. 4.11: The measurement results of the proposed circuit output reference voltage V_{ref} versus temperature (-10C°-100C°).

Wider temperature range performance is also measured. Figure 4.11 shows the measurement output voltage versus temperature with the temperature variation from -10C° to 100 C°. The average reference voltage is 0.5 V. The measurement temperature coefficient of the proposed circuit is only 8.6 ppm/C°. The circuit has a small temperature coefficient even in wider temperature range comparing with the conventional circuit in [7].

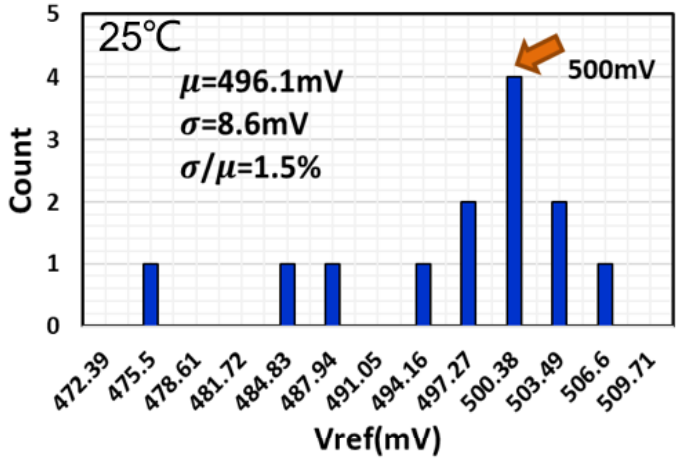


Fig. 4.12: Measured reference voltage distribution from 13 chips at 25C°.

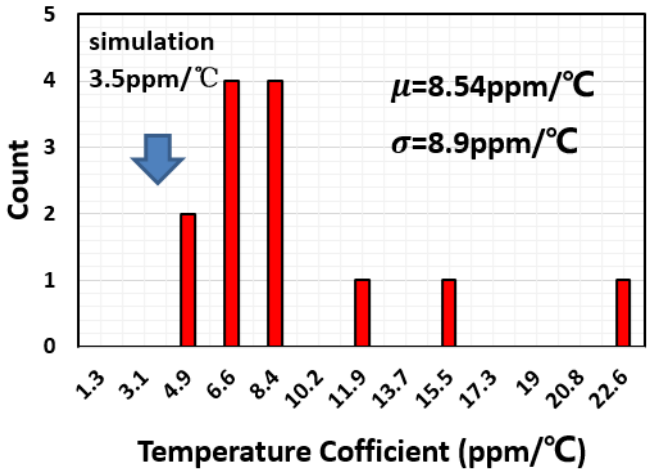


Fig. 4.13: Measured temperature coefficient distribution from 13 chips at 25C°.

Figure 4.12 shows the measured reference voltage distribution from 13 chips at 25C°. The average output reference voltage value is 496.1 mV, and the standard deviation σ is 8.6 mV. The variation of different chips is around 1.5%. The median value of output voltage is closed to the simulation typical value 500 mV.

Figure 4.13 is the measurement results of temperature coefficient distribution from 13 chips at 25C°. The average temperature coefficient from these 13 chips is 8.54 ppm/C°. The minimum temperature coefficient 4.9 ppm/C° is closed to the simulation typical value 3.5 ppm/C°.

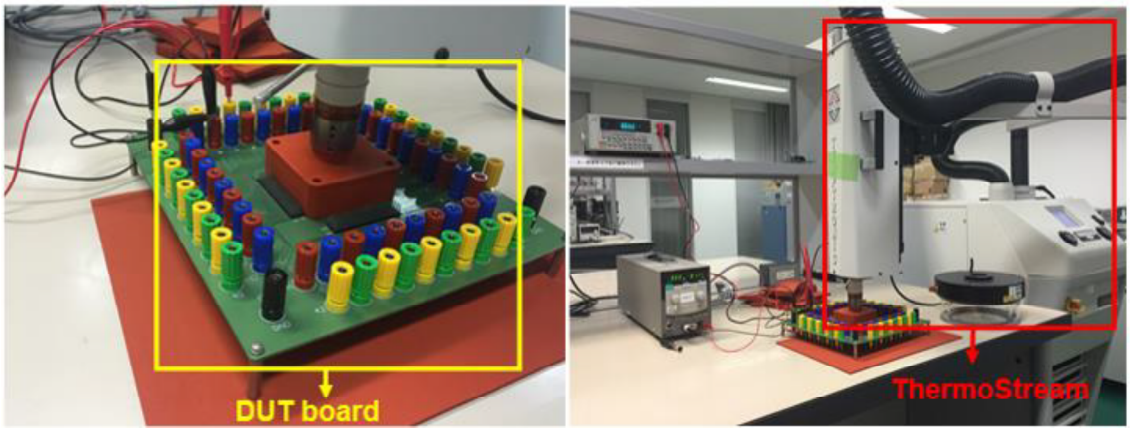


Fig. 4.14: Chip temperature coefficient measurement environment.

Figure 4.14 shows the chip temperature coefficient measurement environment of the bandgap reference output voltage. The chip temperature coefficient measurement uses the machine of ThermoSream, which is approximately exclude the wire influence.

4.6 Performance comparisons

Table 9 is the comparison of the proposed circuit with the conventional circuits in [7][10][11] and [19]. The performances of the circuits in [10], [11] are the simulation results. The performances of the circuits in [7] and [19] are the chip measurement results. For the proposed circuit, both simulation and measurement results are shown. In [7] [10] and [19], the minimum supply voltages are larger than 3 V, which is caused by the circuit structures and the process technologies. In [11], the minimum supply voltage is 1.4 V. However, the limitation of the output reference voltage (1.25 V) in [11] makes the circuit impossible to realize the minimum supply voltage smaller than 1 V. The proposed circuit solves the problem by adding a voltage divider to adjust the output reference voltage value. The minimum supply voltage is achieved to 0.85 V for both simulation and measurement results, which is smaller than 1 V. Moreover, the temperature coefficient of the proposed circuit is 3.5 ppm/C° for simulation and 4.9 ppm/C° for measurement results, which is much smaller compared with the conventional BGR circuits in [7][10][19]. To compare with [11], when the temperature range is 0C° to 100C°, the temperature coefficient of the proposed circuit is 5 ppm/C°. Compared with [19], when the temperature range is -40C° to 130C°, the temperature coefficient of the proposed circuit is about 9.8 ppm/C°.

Table 9: Performance comparisons.

	This work	This work	ISSCC2000[7]	DCAS2010[10]	TCASII2008[11]	TACAII2010[19]
Technology (um)	0.18	0.18	0.5	0.6	0.18	0.5
Supply voltage (V)	0.85	0.85	3.7	3	1.4	3.6
Reference voltage V_{ref} (V)	0.5	0.5	1.115	1	1.012	1.23
Temp. coefficient T_C (ppm/°C)	3.5	4.9	119.7	25	4	11.8
V_{ref} variation with supply from 1.2V-2V(mV)	0.1	0.15	-	-	0.5	-
Temp. range (°C)	0 to 70	0 to 70	0 to 70	0 to 70	0 to 100	-40 to 130
PSRR (dB)@25°C	-75 dB@DC	-51 dB@DC	-45.1 dB@10Hz	-53 dB@60Hz	-75 dB@100Hz	-31.8 dB@10Hz
Power Comsumption (uW)	0.3	0.34	-	-	21	-
Area (mm^2)	-	0.026	0.4	-	-	0.1
Results	Simulation	Measurement	Measurement	Simulation	Simulation	Measurement

4.7 Summary

A CMOS transistors BGR, which operates with sub-1-V supply voltage with the small temperature coefficient has been proposed and verified. It is generated by adding a CMOS voltage divider and a CTAT current source. The simulated minimum supply voltage of 0.85 V and the temperature coefficient of 3.5 ppm/C° (0C°-70C°) have been achieved. The measured minimum supply voltage is also around 0.85 V. Temperature coefficients are 4.9 ppm/C° (0C°-70C°), and 8.6 ppm/C° (-10C°-100C°), respectively. For the temperature coefficient variation results of 13 chips, the mean value of temperature coefficient variation is 8.54 ppm/C°, and deviation σ is 8.9 ppm/C°. The proposed BGR circuit is capable to solve the low voltage problems for the CMOS bandgap reference circuit.

5 Conclusions and Future Works

5.1 Conclusions

SoC is becoming more and more important in portable device design. Thus, low power, low voltage and resistor-less demands increases greatly. In this dissertation, a CMOS CTAT reference voltage generator (V_{th} extractor) a -1-V low temperature coefficient bandgap reference circuit without resistors are proposed, together with a simple and practical statistical model to verify the chip variation. The conclusions are summarized as follows.

In Chapter 2, a simple and practical statistical device model for analog LSI design is presented. The proposed model considers the global variation with the correlation matrix and local variation together. It only needs to extract 4 parameters for MOS transistors. It is applied to predict the variations of some parameters for 0.65 um Op-Amp. The errors of the mean value and the standard deviation for voltage gain obtained from simulations using the proposed model are 1 dB and 0.3 dB compared with the chip measurement results, respectively. While for current consumption, the errors are only 0.01% and 3.03%, respectively. The statistical analysis results using the proposed model are close to practical chip measurement results. This model is used for statistical variation simulation of the proposed circuit in Chapter 3 and Chapter 4.

In Chapter 3, unit and α times V_{th} extractors without resistors are proposed. They are usually applied to the temperature sensor, which distributed at different positions on one chip. As dozens of them are used, low power consumption requirement increases. The

proposed V_{th} extractors realize nano-level power consumption with high accuracy and supply insensitive performance. The key technique is V_{ov} controlling by changing the design parameters. Optimized small V_{ov} and long channel length are the solutions for low power design; ΔV_{ov} compensation and long channel length are the solutions for supply insensitive design. For circuit simulation of 0.18 um process, channel decomposition technique and common centroid layout (post-layout simulation) a

-Watt to microwatt level.

Practical design is also based on the 0.18 um process. However, for technical limitation, all NMOS transistor bodies are connected to ground. The accuracy is worse than simulation results. Active chip area is 0.008 mm^2, and power consumption is still nano-level of 432 nW. The low power design meets the demands for portable device markets.

In Chapter 4, A sub-1-V ultra-low temperature coefficient CMOS bandgap reference circuit is proposed. This solves the problem of total SoC supply voltage limitation. The key technique is using a CMOS voltage divider and a CTAT current source. The output voltage is reduced by reducing the output voltage with the voltage divider. This low temperature coefficient design is realized by making the current source temperature influence smaller using a new CTAT current source. The simulation is based on 0.18 um process. Minimum supply voltage is 0.85 V and temperature coefficient is 3.5 ppm/C°. The measurement results also have a good agreement with the simulation results. The minimum supply voltage is also around 0.85 V. Temperature coefficients are 4.9 ppm/C° from 0 C° to 70 C°, a -10 C° to 100 C°, respectively. For

measured reference voltage distribution from 13 chips, deviation σ is 8.6 mV. For measured temperature coefficient distribution, the mean value is 8.54 ppm/C° and σ is 8.9 ppm/C°, respectively. These measured performances confirm the effectiveness of the proposed low supply voltage and ultra-low temperature coefficient bandgap reference circuit.

In general, voltage reference generators mainly contain two types. The proposed two circuits in Chapter 3 and Chapter 4 cover both requirements for low power and low supply voltage SoC.

5.2 Future works

For the V_{th} extractor circuit in the Chapter 3, the measurement results are worse than simulation results. The possible reason is the unstable measurement environment, body effect and transistor variation. For the next step research, reducing the influence of body effect should be considered. Moreover, some work will be done to improve the measurement environment of this kind of large output impedance circuit. On the other hand, the common centroid layout technique and transistor sizes in CASE 2 will also be used to reduce variation influence in the next chip design.

For the bandgap reference circuit in the Chapter 4, on one hand, the chip-to-chip variation is large. In the next step study, reducing the variation is one topic to consider. On the other hand, the proposed bandgap circuit without resistors has a very low temperature coefficient. This performance is considered not only because that, the proposed current source with negative temperature dependence is approximately applied as an ideal current source, but also the current is capable to dramatically give a curvature correction for second order or even high order compensation when flowing through the

p-n junction (diode). According to this analysis, much more optimized combinations of transistor sizes are chosen, and the simulation results for the bandgap reference output voltage temperature coefficient are also further more improved. Based on this, the author's another next step research will focus on ultra-low temperature coefficient curvature correction bandgap reference circuit without resistors study and make chips to verify this theory. The aim is to reduce both the output voltage chip variation and temperature coefficient chip variation. In this case, the cost of trimming technique is excluded.

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Acknowledgements

Firstly, the author would like to express the deepest gratitude to the advisors. Thanks to Prof Yasuaki INOUE, who has taught me how to do research; and thanks to Professor Hirofumi SHINOHARA, my professor after the retirement of Professor Yasuaki INOUE, who gives the author many professional and helpful suggestions. The dissertation could not have reached its present form without their impressive patience, kindness and constant encouragement. The author is proud of becoming one of their students for their profound knowledge in academic and rich experience in society. Their academic observations would enlighten the author in the future works.

Second, the author would like to thank Professor Toshihiko YOSHIMASU and Professor Takahiro WATANABE for their kind helps and instructions.

Thirdly, the author would like to show her heartfelt thanks to the co-advisor. Thank them for reviewing the researches and giving so many suggestions, which are very important to the improvement of the study.

Fourthly, the author would also like to thank the past and present members of Professor INOUE's group and Professor SHINOHARA's group. They are Zhangcai Huang, Qiang Li, Li Ding, Zhou Jin, Xiao Wu, Dan Niu, Kunyang Liu, etc. The author appreciated the many happy hours spent with them and she will cherish the friendship with them forever.

Last but not least, the author is forever grateful to her family for being supportive and patient during the past several years. Thank you very much to her father, mother, lovely little brother and boyfriend.