Graduate School of Fundamental Science and Engineering
Waseda University

博 士 論 文 概 要
Doctoral Thesis Synopsis

論 文 題 目
Thesis Theme

VLSI Architecture of Intra-Prediction and SAO Estimation in HEVC and its Extension to Compressed Sensing

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People have always wanted better visual experiences. From Ultra High Definition Television (UHDTV), 3D video to Virtual Reality (VR), the pursuit of overwhelming visual experiences is unlimited. For such visual experience, the higher resolution and frame rate are important. For instance, the 8K UHD (7680*4320 resolution) with 120 frames per second (fps) is considered for the video application of the next decade. It is reported the sports broadcasting and the perfect VR require even higher resolution and frame rate, which sets technical challenges, such as the huge data volume and high processing throughput (frame resolution * frame rate).

Such huge data are impossible to store or transfer without encoding. The video data to encode have two types, the pixels and measurements (linear combinations of pixels). Pixels are generated from traditional CMOS image sensor, and measurements from Compressed Sensing (CS) based CMOS image sensor. The pixel encoding has a long history since 1968. High Efficient Video Coding (HEVC) is the most advanced one achieving a high compression ratio at the expense of high computational complexity contributed by the new features. Hence, designing high performance VLSI architecture to support UHD video application are challenging and necessary. Among all components in HEVC, the VLSI architecture of Intra prediction and Sample Adaptive Offset (SAO) are chosen. Since they are the most different components in function comparing with H.264. The different requires new and efficient VLSI architecture to support the UHD video encoding. They are discussed and proposed in Chapter 2 and 3 respectively.

As the resolution and frame rate increase, the traditional image sensor has power consumption problem and higher frame rate is hard to achieve. These problems could be solved by new type of image sensor using CS. It could recover the whole image by capturing only few measurements in the image sensor. Capturing much less data instead of every pixel, the power consumption in the image sensor could be reduced, hence it provides a promising future for the increasing resolution and frame rate in video application. Measurements coming from CS image sensor still required encoding before the transfer. However, measurements don't have the obvious spatial similarity that provides spaces for intra prediction in HEVC. To better encode the measurements, the intra prediction algorithm and VLSI architecture for CS is explored in Chapter 4 and 5.

VLSI architecture supporting high parallel degree (amount of pixels/measurements process per cycle) is necessary to processing the huge data. However, the higher parallel degree results into larger circuit area thus reducing the performance (Throughput / circuit area). This dissertation mainly targets on the high-performance VLSI architecture of HEVC SAO Estimation, intra prediction for encoder and its exploration in Compressed Sensing, by using the proposed concept "reduced video data". Only by taking the necessary video data, including pixels and measurements, it is possible to reduce the parallel degree in hardware while keeping the performance during the data processing. The summary of each chapter is introduced as follows.

Chapter 1 [Introduction] introduces the big picture of video acquisition process, including the traditional imaging and the CS imaging. Next, HEVC intra prediction and SAO are introduced. Furthermore, the motivation to explore the intra prediction in CS is introduced. At last, proposed concepts of this dissertation are shown.

Chapter 2 [VLSI architecture of HEVC Intra prediction using reduced loaded-pixels] presents the high-performance VLSI architecture for HEVC intra prediction. Intra prediction uses neighboring pixels from

different directions to predict pixels of a block (4x4~32x32). As the block size increases from 16 to 32 in HEVC, it takes 3x more neighboring pixels for prediction. Instead of loading all neighboring pixels as previous work, only the necessary pixels are loaded. This proposed idea reduces the two-third of reference pixels, thus reducing the area and increasing the throughput. It is achieved by LUT (Look Up Table) generated by software to tell which pixels are demanded in each prediction mode and location. Another proposal is the Hybrid Block Reordering and Data Forwarding, minimizing the idle time and eliminating the dependency between blocks by creating three Data Forwarding paths. It achieves the hardware utilization of 94%. The proposed VLSI architecture has a gate count of 217.8K, and is able to support 4320p@120fps HEVC intra prediction.

Chapter 3 [Dual-clock VLSI architecture of HEVC Sample Adaptive Offset Estimation] presents a high-performance VLSI design for SAO estimation. SAO is a process to find out optimal offsets to reduce ringing noises in an image. It consists of two steps, Statistics Collection (SC) and Parameter Decision (PD), each of them has totally different nature in calculation. SC has huge but simple calculations while PD has few but complex calculations. After studying such nature, it is discovered that reducing pixels to process per clock cycle in SC significantly reduces the area. Thus, a dual-clock architecture is proposed, where SC works under high frequency and PD under low frequency, so that SC could process few pixels each cycle. Such proposal reduces the overall area by 56%. To further improve the area and power efficiency, algorithm-architecture co-optimizations are applied including a coarse range selection (CRS) and an accumulator bit width reduction (ABR). CRS shrinks the range of fine processed bands for the band offset estimation. ABR further reduces the area by narrowing the accumulators of SC. They together achieve another 25% area reduction. The proposed VLSI design is capable of processing 8K@120fps encoding. It occupies 51K logic gates, only one-third of the circuit area of the state-of-the-art design.

Chapter 4 [Algorithm and VLSI architecture of intra prediction in Compressed Sensing using reduced measurements] presents a measurement intra prediction framework. Instead of using all measurements for prediction, measurements for prediction are reduced to two. These two measurements embed the block boundary information of closest area. They are obtained by modifying two rows in the random 0/1 measurement matrix. Furthermore, a low-cost VLSI architecture is implemented for the proposed framework, by substituting the matrix multiplication with shared adders and shifters. The experimental results show that our proposed framework can compress the measurements and increase coding efficiency, with 34.9% BD-rate reduction compared to the direct output of CS-based sensors. The VLSI architecture of the proposed framework is 9.1K in area, and achieves the 83% reduction in size of memory bandwidth and storage for the line buffer. This could significantly reduce both the energy consumption and bandwidth in communication of wireless camera systems.

Chapter 5 [Row-Operation-Based Intra prediction under Approximate-DCT measurement matrices and its VLSI Architecture implementation] presents the row-operation to perform the intra prediction on the proposed approximate-DCT measurement matrices. Deterministic measurements matrices derived from approximated-DCT are proposed, significantly increasing the coding efficiency comparing with the random binary matrix in Chapter 4. However, the intra prediction using two measurements in the last chapter could not

work on proposed matrices. Instead of using all measurements for prediction, the row-operation using three measurements are proposed. It achieves intra prediction as Chapter 4, without modifying the measurement matrix. Lastly, the VLSI architecture design for the intra prediction is proposed. Experiment results show the proposed matrix improve the coding efficiency by BD-PSNR increase of 4.2 dB. The proposed row operations increase the coding efficiency by 0.24 dB BD-PSNR. The VLSI architecture is only 4.3 K gates in area and 0.3 mW in power consumption, which is only half of the area and the power consumption in previous work.

Chapter 6 [Conclusion and future work] concludes the contributions of this dissertation. The solved and remaining problems are left for the future works.

早稲田大学　博士（工学）　学位申請　研究業績書

(List of research achievements for application of doctorate (Dr. of Engineering), Waseda University)

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学術誌原著論文	○ 1. Jianbin Zhou, Dajiang Zhou, Takeshi Yoshimura and Satoshi Goto “Approximate-DCT-Derived Measurement Matrices with Row-Operation-Based Measurement Compression and its VLSI Architecture for Compressed Sensing”, IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, Vol.E101-C, No.4, pp.263-272, Apr. 2018 ○ 2. Jianbin Zhou, Dajiang Zhou, Li Guo, Takeshi Yoshimura and Satoshi Goto “Framework and VLSI Architecture of Measurement-Domain Intra Prediction for Compressively Sensed Visual Contents”, IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, Vol.E100-A, No.12, pp.2869-2877, Dec. 2017 ○ 3. Jianbin Zhou, Dajiang Zhou, Shihao Wang, Shuping Zhang, Takeshi Yoshimura and Satoshi Goto, ″A Dual-Clock VLSI Design of H.265 Sample Adaptive Offset Estimation for 8k Ultra-HD TV Encoding,″ in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 2, pp. 714-724, Feb. 2017. 4. Dajiang Zhou, Shihao Wang, Heming Sun, Jianbin Zhou, Jiayi Zhu, Yijin Zhao, Jinjia Zhou, Shuping Zhang, Shinji Kimura, Takeshi Yoshimura, and Satoshi Goto; ″An 8K H.265/HEVC Video Decoder Chip With a New System Pipeline Design,″ in IEEE Journal of Solid-State Circuits (JSSC), vol. 52, no. 1, pp. 113-126, Jan. 2017. 5. Shihao Wang, Dajiang Zhou, Jianbin Zhou, Takeshi Yoshimura, and Satoshi Goto, VLSI implementation of HEVC motion compensation with distance biased direct cache mapping for 8K UHDTV applications, IEEE Transactions on Circuits and Systems for Video Technology (TCSVT), vol. 27, no. 2, pp. 380-393, Feb. 2017. ○ 6. Jianbin Zhou; Dajiang Zhou; Shihao Wang; Takeshi Yoshimura and Satoshi Goto. “High performance VLSI architecture of H. 265/HEVC intra prediction for 8K UHDTV video decoder”, IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, Vol. E98.A (2015) No. 12 pp. 2519-2527, Dec. 2015.

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