Graduate School of Fundamental Science and Engineering
Waseda University

博 士 論 文 概 要
Doctoral Thesis Synopsis

論 文 題 目
Thesis Theme

RADIATION-INDUCED SOFT ERROR HARDENED LATCH DESIGN TECHNIQUES FOR RELIABILITY AND ENERGY-EFFICIENCY IMPROVEMENTS

申 請 者
(Applicant Name)

Saki	TAJIMA
田島	咲季

Department of Electronic and Physical Systems,
Research on Integrated system design

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With Complementary Metal-Oxide Semiconductor (CMOS) technology shrinking and power supply voltage dropping greatly, the reliability issue has become much more critical than ever before. In general, reliability failures include systematic issues such as process/voltage/temperature (PVT) variations and aging effects (e.g. hot carrier injection (HCI) and Bias Temperature Instability (BTI)), and random failures such as soft errors caused by radiation. Among these reliability failures, radiation-induced soft errors are becoming one of the most critical concerns in state-of-the-art Very Large-Scale Integration (VLSI) designs. Soft error is a temporary error caused by collision of radiation particle like alpha particle and high energetic neutron on a circuit. When radiation particle strikes on a circuit, the electron-hole pairs are generated and collected to PMOS and NMOS diffusions, respectively. If the collected charge is beyond the critical charge, the stored data of PMOS transistor will be temporarily changed from logical from '0' to '1' and the data of NMOS transistor is changed from logical from '1' to '0'. As process technology continues scaling down, the critical charge of internal nodes is reduced due to the reduced capacitance, which results in the increased soft error rate (SER) in modern integrated circuits (ICs), and the influence of charge sharing would cause multiple-node-upsets (MNUs). Furthermore, soft errors are generally caused in-field, and due to the temporary property, they can be recovered automatically if given some additional time or through reset operations. However, the unpredictable occurrence of soft errors might lead to severe system failures in critical designs such as medical devices, aircraft and high-performance supercomputers. Consequently, radiation-induced soft error hardened design techniques have become essential to guarantee systems' reliability.

In literature, several design techniques such as hardware redundancy methods (e.g. Triple-Modular-Redundancy (TMR)), Error-correcting code (ECC)-based memory, soft error aware physical designs, soft error tolerant designs, and error-detection-based methods have been proposed to guarantee the reliability of ICs. Since most of existing works are based on hardware redundancy for error recovery or error tolerance, the corresponding soft error resilience usually comes at the price of increased area, power, and/or delay penalties, which becomes the challenge for next generation energy-efficient MNU-tolerant designs. In addition, soft errors occurring in a latch can lead to an upset at the latch output, which may propagate through the succeeding combinational logic and is captured by the next-stage storage element; however, this issue was often neglected in previous works. Therefore, it is desired to develop architecture-level reliable radiation-hardened latch designs.

In this dissertation, three soft error hardened latch designs are proposed for architecture-level reliability and energy efficiency improvement. Firstly, a low-cost soft error hardened latch (SHC) design using a novel Schmitt-Trigger-based C-element (STC) is proposed in Chapter 3, which features small area overhead and low power consumption for single node upset (SNU) tolerance. Unlike state-of-the-art soft error tolerant latches that are usually based on hardware redundancy or transistor upsizing, the proposed latch is implemented through double-sampling and node-checking by using a novel Schmitt-Trigger-based C-element for soft error tolerance improvement. To sample the latch input data twice is to protect storage cells from Single Event Transients (SETs) which is soft error occurring in combination circuits. If SETs are loaded into the storage cell, they can result in data corruption in the corresponding storage cell. To mitigating the effect of SETs, the latch input is sampled at different time in the proposed SHC latch. The Schmitt-Trigger-based C-element in the proposed SHC latch is used

for internal node checking and filtering single-bit-error. The proposed Schmitt-Trigger-based C-element consists of 8 transistors and can be viewed as two C-elements, one of which is used for single-bit-error filtering, and the other is used for input-output node checking. The proposed SHC latch has been simulated in ROHM 180nm CMOS process technology with Vdd=1.8V and the clock frequency to be 125 MHz. The implementation results show that the total number of transistors of the proposed SHC latch is only increased by 2 when compared to the conventional unhardened C^2MOS latch, and up to 20.35% and 82.96% power reduction can be achieved when compared to the conventional unhardened C^2MOS latch and the existing soft error tolerant HiPeR design, respectively.

The second proposed latch design as shown in Chapter 4 is a power-efficient single node upset hardened latch with in-situ error detection capability (EDSL) for reliability improvements against SNUs. As explained above, it is desired to develop architecture-level reliable radiation-hardened latch designs. Therefore, EDSL is proposed by incorporating SNU self-recover ability with in-situ error detection capability for reliability improvement against soft error. The proposed EDSL can not only recover from any incurred single event upset, but also provide in-situ error detection capability when the latch output is upset. EDSL design consists of the error tolerant part and the error detector part which detect transition caused by soft error on the output. EDSL latch has four main nodes such as PDH, NDH, BQ and the output Q. In particular, PDH and NDH are adopted the soft error occurrence mechanism that soft error changes the data of node consisted only PMOS or NMOS transistors in one direction, low-to high and high-to-low, respectively. Because EDSL uses this occurrence mechanism and limit the occurrence so that it makes detector part simple configuration. The detector part generates the error signal only when the output Q is flipped. On the other hand, Q and BQ are driven by both of transistors so that it will be flipped in both directions. In normal mode, EDSL can operate as normal latch and will not generate the warning signal. When soft error effects on PDH or NDH, it can self-recover with the data on internal nodes and will not propagate the fault data to other nodes and will not generate the error signal because Q keeps the correct data. In the situation when BQ or Q is flipped by soft error, the output must be flipped temporarily, and the error warning signal is generated. Furthermore, it can recover from soft error referring to the data of other nodes immediately. From above description, the proposed EDSL cannot only recover from SNUs, but also provide in-situ error detection capability when the output data is flipped. The proposed EDSL latch has also been designed by using ROHM 180nm CMOS process technology with Vdd=1.8V and the clock frequency to be 125 MHz. The implementation results show that, when compared with state-of-the-art error-detection based and SNU resilient designs, the proposed EDSL latch can achieve up to 72.25% and 79.74% reduction of power-delay product respectively, which clearly shows the effectiveness of the proposed EDSL method.

The third design is an output transition detector-based radiation-hardened latch (TDRHL) for power efficiency and reliability improvement of critical designs against both single- and multiple-node upsets, which is presented in Chapter 5. The proposed TDRHL design contains a baseline latch, an error recovery assistant logic (ERAL) and an output transition detector (QTD), in which the error recovery assistant logic is optimized from the existing single-event-induced-double-node upset-tolerant latch (SEID) for performance improvement and power reduction and the output transition detector is proposed to provide architecture-level recovering capability. TDRHL

has main 6 critical nodes, LP1 and LP2 are driven only by PMOS transistors and LN1 and LN2 are driven only by NMOS transistors, LQ and Q are driven by both of transistors so that LP1, LP2, LN1 and LN2 will flip in one direction, respectively, and the data on LQ and Q will be changed in both directions. In normal mode, TDRHL can operate as normal latch. In the situation when one or two data are flipped by soft error, it can self-recovery referring to other node data. When the flipping nodes including Q, it can not only self-recover but also generate the error alert signal by QTD. In addition, triple-node-upsets (TNUs) occur on TDRHL, it can generate the alert signal, but it cannot self-recover. Therefore, the proposed TDRHL can 1) recover from any SNUs and DNUs to its correct state, and 2) generate a warning signal for architecture-level recovery only when the latch output is flipped. The proposed TDRHL latch is designed and simulated by using ROHM 180nm CMOS process technology and the 32nm Predictive Technology Model (PTM), and timing variations at various process corners (SS: 0.8V/125◦C, TT: 0.9V/25◦C, FF: 1.0V/-40◦C) are also considered in the modern 32nm PTM model. The evaluation results show that, the proposed TDRHL outperforms state-of-the-art DNU tolerant designs with addition error detection capability, and up to 5.0X PDP improvement can be achieved. On the other hand, when compared with the existing detection-based design, self-recovery capability of SNUs and DNUs is provided at the cost of only 4.4% more power consumption. For the timing variations at different process corners, the existing SEID shows the greatest fluctuations and SHST is the next, while the timing variations of HRDNUT and the proposed TDRHL are the most consistent. Specifically, the proposed TDRHL outperformed existing works, which is partially due to the short path introduced in TDRHL. As for power efficiency, the PDP improvements at TT corner of TDRHL over SEID, HRDNUT and SHST are 1.9X, 2.5X and 5.0X, respectively. It should be noted that TDRHL is the only latch that can recover from any SNUs and DNUs, and provide architecture-level resiliency, therefore the PDP results clearly illustrate the power efficiency of TDRHL.

Conclusion and future research are presented in Chapter 6. In this dissertation, three radiation-induced soft error hardened latch designs are proposed for reliability and energy-efficiency improvements, which can be viewed as i) SNU hardened design, ii) SNU hardened and detection-based design, and iii) MNU hardened and detection-based design. As process technology continues scaling down, soft errors are becoming one of the most critical concerns in state-of-the-art ICs. Due to the transient property of soft errors, architecture-level design techniques should be developed to guarantee systems' reliability. Therefore, one of the future works involves the improvement of the proposed designs for architecture level applications. Furthermore, it is observed that more and more research work on the next generation non-volatile memories (NVMs) have been proposed. Therefore, another direction of the future work involves developing soft-error tolerant NVMs such as phase change memory (PCM) and spin transfer torque RAM (STT-RAM) for reliability improvement of future memory systems.

早稲田大学　博士（工学）　学位申請　研究業績書

(List of research achievements for application of doctorate (Dr. of Engineering), Waseda University)

氏 名(Full Name)　田島咲季（Saki, TAJIMA）　印(seal or signature　　)

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