High-Performance Normally-off 2DHG Diamond MOSFET for High Voltage Switching Application

高性能ノーマリオフ 2DHG ダイヤモンド MOSFET を用いた高電圧スイッチングアプリケーション

Te BI

畢 特

Waseda University

Graduate School of Fundamental Science and Engineering

Department of Electronic and Physical Systems

Research on Nanodevices

Supervisor: Hiroshi Kawarada

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Abstract

Chapter 1. This chapter begins with an overview of WBG semiconductor materials and their applications in power devices. The SiC high-voltage power devices and GaN-based high electron mobility transistor (HEMT) n-type devices and their circuit applications are also introduced in this chapter. However, these materials are very difficult to be utilized as p-type devices. Diamond, owing to its unique physical and electrical properties and a bandgap of 5.5 eV, has become the most promising new generation semiconductor material for p-type power devices, as compared to SiC and GaN. The diamond surface exhibits negative electron affinity (NEA) by hydrogen-termination. Thus, the C–H diamond surface is an NEA of about 1.3 eV; hence, diamonds with hydrogen-terminated bonds exhibit unique surface conductivity. Energy band bending caused by negative charge adsorption on the C-H suface induce two-dimensional hole gas (2DHG) under the diamond surface, and the C–H diamond exhibits very high p-type conductivity.

The C–H diamond metal oxide semiconductor field effect transistor (MOSFET) is achieved with the C–H diamond surface being utilized as a surface conductive channel, which is based on the 2DHG in the subsurface diamond and facilitate the formation of the p-type channel. However, the surface conducting layer is affected by the temperature of the environment; therefore, a passivating layer is needed to stabilize the adsorbates and surface C–H bonds, which is important for the temperature stability of

the 2DHG. A C–H diamond MOSFET is fabricated with a high-temperature (450 °C) using an atomic layer deposition (ALD) Al_2O_3 passivating film and H_2O as an oxidizing agent. As a result, the C–H diamond MOSFET becomes capable of operating in a wide range of temperatures and has a high breakdown voltage. Because of the low interface states density ($<10^{12}$ eV^{-1} cm^{-2}) of the C–H diamond and the independent crystallographic orientations of the 2DHG, a high drain current density vertical-type diamond MOSFET can be manufactured with the help of a diamond RF power device, which has high power density and low ON resistance.

However, the C–H diamond MOSFETs operates in the normally ON state due to the spontaneous polarization effect of the C–H dipoles, and the existence of a fixed negative charge in the alumina insulating film is attracted by this polarization, and the hole normally induced on the C–H diamond surface. A normally-off diamond power device has become a key topic for research in the diamond-based devices field. The 2DHG diamond achieves a normally-off operation through surface modification, thus destroying or reducing the C–H surface and adjusting and controlling the quantity and type of fixed charge in the insulating film.

In summary, achieving high-performance, normally-off 2DHG diamond MOSFETs are very important for diamond devices that operate as high-performance power devices in electric power conversion systems having semiconductor integrated circuits, such as a high voltage complementary switching circuit.

Chapter 2 In this chapter, a high drain current C–H diamond MOSFET is fabricated

by increasing the gate width (W_G) of the MOSFETs. In the experiment, lateral-type C–H diamond MOSFETs with W_G ranging from 25 μm to 500 μm and vertical-type C–H diamond MOSFETs with W_G ranging from 0.125 mm to 10 mm were fabricated. In the fabrication process of the lateral-type C–H diamond MOSFETs, the Ti/Pt/Au required for the source/drain electrode was formed on an n-doped (100) diamond substrate with an undoped homoepitaxial growth diamond layer. The C–H channel and TiC were formed under high temperature conditions and in an atmosphere of hydrogen and hydrogen plasma, respectively. A 200-nm (ALD) Al_2O_3 passivating film was formed, and the process of MOSFET fabrication was completed after the Al gate deposition.

To further expand the gate width W_G of diamond MOSFETs, vertical-type MOSFETs with multi-trench structures were fabricated on IIb (100) p+ diamond substrates. A nitrogen-doped layer was constructed through the MVPCVD to prevent leakage of current, and multiple trench structures were etched on the substrate of the vertical channel source electrode (Au/Pt/Ti: 20/30/200 nm). Consequently, a multi-finger structure was formed around the trench. After the hydrogen termination and annealing, a 200 nm Al_2O_3 layer was formed on the top, and a Ti/Au drain electrode (10/250 nm) was formed on the backside of the p+ diamond substrate. Finally, a 100-nm Al film was used to fabricate the overlapped-gate electrode.

As a result, it was observed that the maximum value of I_{DS} for lateral-type C–H diamond MOSFETs is −50 mA with W_G = 500 μm, while for vertical-type C–H diamond MOSFETs, the maximum value of I_{DS} is −185 mA with W_G = 5 mm. The

maximum output current of the diamond MOSFET is enhanced by increasing the gate width.

Chapter 3 In the previous chapter, the fabrication process and characteristic analysis of high-current diamond MOSFETs are described. However, all MOSFETs usually operate in the normally-on condition. We use the cascode structure to shift the threshold voltage V_{TH} of the diamond MOSFET to normally-off. The diamond cascode was fabricated by combining a normally-off silicon p-MOSFET with low breakdown voltage and a normally-on C–H diamond MOSFET with high breakdown voltage.

The diamond cascode is composed of lateral- and vertical-type C–H diamond MOSFETs having an enlarged gate width achieved during the normally-off operation. The V_{GD}–I_{DS} characteristic shows that the threshold voltage of the diamond cascode is normally-off at $V_{TH} = -1$ V, and the breakdown voltage of the diamond cascode combined with the lateral-type C–H diamond MOSFET with $L_{GD} = 25$ μm reaches −1735 V when $V_{GS} = 0$ V (a true normally-off voltage blocking condition). In this study, the gate of the diamond MOSFET is effectively controlled by the silicon p-MOSFET, which causes the diamond p-channel cascode to exhibit a normally-off operation and breakdown performance.

The diamond cascode is utilized in the upper branch of a half-bridge inverter as a p-channel normally-off power device, while a normally-off GaN n-FET by cascode circuit is utilized in the lower branch. The gate driver inverter is based on a push-pull circuit, which consists of a Si n-MOSFET (upper branch) and a Si p-MOSFET (lower branch)

to drive the diamond–GaN half-bridge inverter in high operation voltage. Both the half-bridge inverter and the gate driver inverter are under the same drain power voltage (V_{DD}). The output voltage of the gate driver inverter is fed to the diamond–GaN half-bridge inverter as the input gate voltage through resistors connected in series with the drains.

The results show that the diamond–GaN half-bridge complementary inverter at 1000 Hz under high-voltage conditions (200 and 150 V) is realized using a two-stage circuit structure. The switching speed became faster after utilizing the diamond MOSFETs with larger gate widths (fabricated in Chapter 2). T_{ON} = 1.4 μs obtained with W_G = 5 mm for the vertical-type diamond MOSFET in the upper branch is approximately 4 times faster compared to that obtained with WG = 500 μm for lateral-type diamond MOSFET.

In **Chapter 4**, a new comcept to fabricate a high-performance normally-off diamond MOSFET is presented by utilizing the C–Si-bonded diamond surface formation as a two-dimensional layer channel for p-type diamond MOSFETs. The C–Si bonded diamond surface is formed at a high temperature in a reducing gas atmosphere on the SiO_2/diamond interface during boron doping diamond selective growth through SiO2 masking. Above 3 monolayers, C–Si bonding on the diamond surface is confirmed through X-ray photoelectron spectroscopy at the C1s and Si2p core levels from 290 eV–271 eV and 107 eV–95 eV, respectively. In addition, secondary ion mass spectroscopy results suggest that it is not the C–H bonds, but the C–Si bonds at the

interface, which are mainly responsible for the FET operation. 2DHG C–Si diamond MOSFETs are fabricated using the C–Si diamond surface as a p-channel. MOSFETs with L_{SD} in the range of 6–12 μm exhibit appreciable field-effect mobility (140 cm2V-1s-1 at L_{SD} =12 μm and 300 K) and normally-off operation at the same time. The wide temperature characteristics of the C–Si MOSFET were confirmed. The performance of the MOSFET is enhanced as the temperature increases, owing to the boron-doped selectively grown diamond in the source and drain electrodes, and the device shows great stability with a high on/off ratio of 10^6, which is maintained at 673 K. The C–Si MOSFET shows excellent temperature stability and a normally-off operation.

Finally, a C-Si diamond MOSFET with a thinner SiO_2 insulating film and without the Al_2O_3 film was fabricated and tested. These devices show high mobility with the normally-off operation, and the high-speed complementary switching circuit is realized by combining the normally-off C–Si diamond p-MOSFET and the normally-off Si-n MOSFET.

Chapter 5 is the summary of this doctoral thesis, where we mainly discuss the manufacturing method and working mechanism of the high-performance normally-off 2DHG diamond MOSFET. Diamond MOSFETs show great potential for application in electronic circuits and power conversion systems.

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Chapter 1
Overview of diamond power device application

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1.1 Wide bandgap semiconductors

Since the 20th century, semiconductors have gained such importance that development of modern science and technology is tantamount to the development of semiconductor technology. Semiconductors are used in various fields, such as aerospace, computers, and power systems. Silicon (Si), as a semiconductor material, has played an important role in the history of semiconductor development. Owing to the considerable research that has been conducted and mature technology in silicon semiconductors, the commercial and industrial semiconductor market has been dominated by Si in the past decades. However, Si-based semiconductor power devices are approaching the theoretical limits of silicon in terms of various physical characteristics, such as thermal conductivity, breakdown voltage, high temperature characteristics, switching speed, and mobility. Thus, due to the limits in these parameters, it is difficult to develop novel silicon power devices for electronic power systems that operate at high voltage, power, and frequency.

Recently, wide bandgap (WBG) semiconductors (SiC, GaN) have been introduced. Owing to their excellent physical characteristics and ability to break through the theoretical limit of silicon, these devices have been widely studied and applied as second-generation semiconductors. Semiconductor materials with bandgap significantly wider than 3.4 electron volts (eV) are called ultra-wide bandgap semiconductors (UWBGs). The physical properties of these UWBG semiconductor

Material		Silicon	WBG		UWBG		
			4H-SiC	GaN	Diamond	β-Ga_2O_3	AIN
Band gap (eV)		1.1	3.3	3.4	5.5	4.9	6.1
Critical electric field (MV cm^{-1})		0.3	2.8	3.0	7.7-20	10.3	10
Mobility (cm^2 V^{-1} s^{-1})	Electron	1500	900	2260 (2DEG)	4500	180	300
	Hole	480	120	<100 (2DHG)	3800	-	14
Thermal conductivity ($Wm^{-1}K^{-1}$)		150	370	253 (on GaN) 165 (on sapphire) 100 (on Si)	2290-3450	11-27	253
Relative permittivity(a.u.)		11.8	9.8	9	5.5	9.9	8.5
Substrate dislocations (per cm-2)		<10	10^2	10^4	10^4-10^6	10^4	10^4
Saturation Velocity (x10^7 cm s^{-1})	Electron	1	1.9	2.5	2.5	2	1.4
	Hole	0.8	1.2	-	1.4	-	-
Built-in voltage (V)		0.6	2.8	2.9	4.9	-	-

Table1.1 Representative WBG and UWBG semiconductor materials in current industry and research.

materials (e.g., diamond, Ga_2O_3, AIN) exceed the theoretical limit of Si. They have a higher breakdown electric field and better thermal conductivity, which reduces power loss caused by switching of semiconductor power devices made from these materials in high-voltage and high-frequency environments. Low-dimensional UWBG power devices have good working stability and improved working stability over a wide temperature range and operating life in electric power transmission systems. This means that UWBG semiconductor materials have wider application scenarios and greater application potential. In large-scale integrated (LSI) circuits, better temperature stability and thermal conductivity can increase the fault tolerance rate of products and reduce the size of cooling systems. In addition, semiconductor integrated circuits (IC) can work normally in extreme temperature environments (e.g., cosmic environment).

Table 1.1 shows an illustrative list of the semiconductor materials used in industry and

research. Figure 1.1 compares conventional semiconductors and several wide bandgap semiconductors based on their electron velocity and electric field characteristics. It can be seen from the figure that when the bandgap is above that of the WBG semiconductor, the breakdown electric field and thermal conductivity are relatively higher than those of silicon, which makes 4H-SiC suitable for use as high-power amplifiers, switches, and diodes [1]. In diamonds, electron and hole velocities at high electric fields (saturated velocity) are typically higher than that of WBG. Moreover, all parameters of diamonds are superior to other semiconductor materials; hence, diamond has a great potential for use as a next-generation semiconductor material in power devices, amplifiers, and inverters. This doctoral thesis will focus on the fabrication, characteristics, and mechanism of diamond semiconductor power devices and their application in semiconductor circuits. The specific background, research methods, and results will be discussed separately in the succeeding chapters.

1.1.1WBG semiconductor power devices

Compared with conventional semiconductors, power devices made of WBG semiconductor materials have advantages in many performance indexes. Among them, second-generation semiconductors, such as SiC and GaN, are the most typical. SiC and GaN have energy bandgaps approximately two to three times those of conventional semiconductors, such as Si, GaAs, and InP. Compared with GaN, SiC was developed

earlier and the technology is more mature than that of GaN. A large difference between these two semiconductors is their thermal conductivity, which makes SiC dominant in high-power applications. On the contrary, as AlGaN/GaN has a higher electron mobility, GaN-based devices can have a higher switching speed than SiC or Si in high-frequency applications.

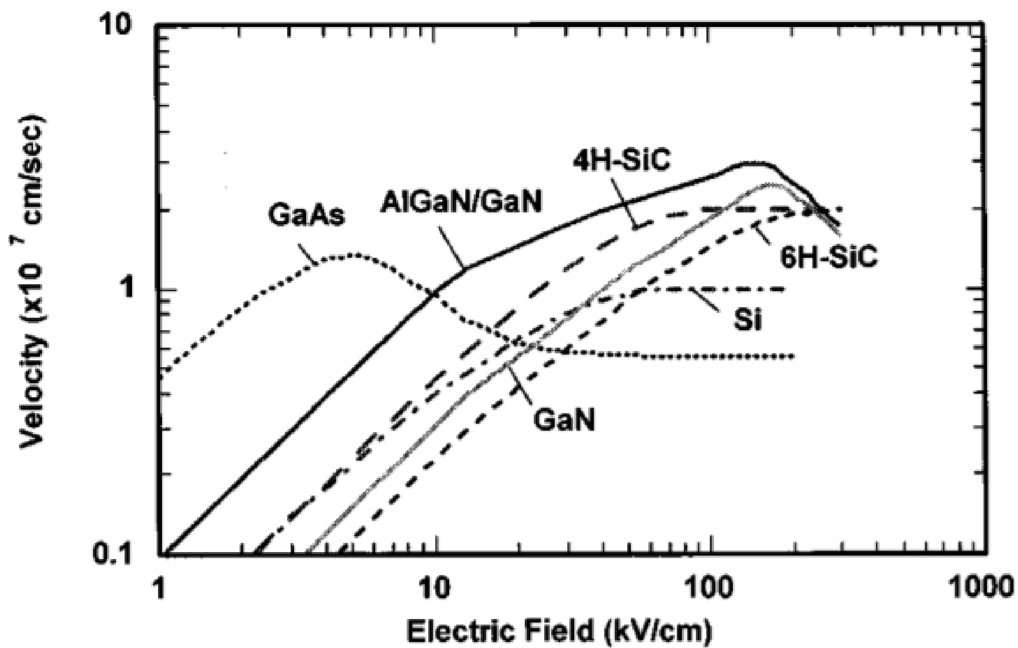


Fig. 1.1 Comparison of electron velocity and electric field characteristics between conventional semiconductors and several wide bandgap semiconductors. Among these characteristics, the charge carrier mobility (cm^2/Vs) can be defined as the slope of v–E characteristics under low electric field [2].

Silicon carbide is an excellent thermal conductor; however, GaN is similar to silicon, which makes SiC-based power switches well suited for high-temperature and high-voltage applications. SiC junction gate field-effect transistor (JFET), with low on-resistance and breakdown voltage in the 1 to 5 kV range, has been achieved [3][4][5]

(Fig. 1.2 (a) and (b)). However, JFET can work in enhancement-mode using cascode technology and can be realized via combination with normally-off Si MOSFET [6] (Fig. 1.2 (c)). The cascode applications in SiC power devices have achieved high breakdown voltage and switching speed [7] (Fig. 1.2 (d)), which makes these devices bring great changes and development to power conversion technology, such as DC–DC converter

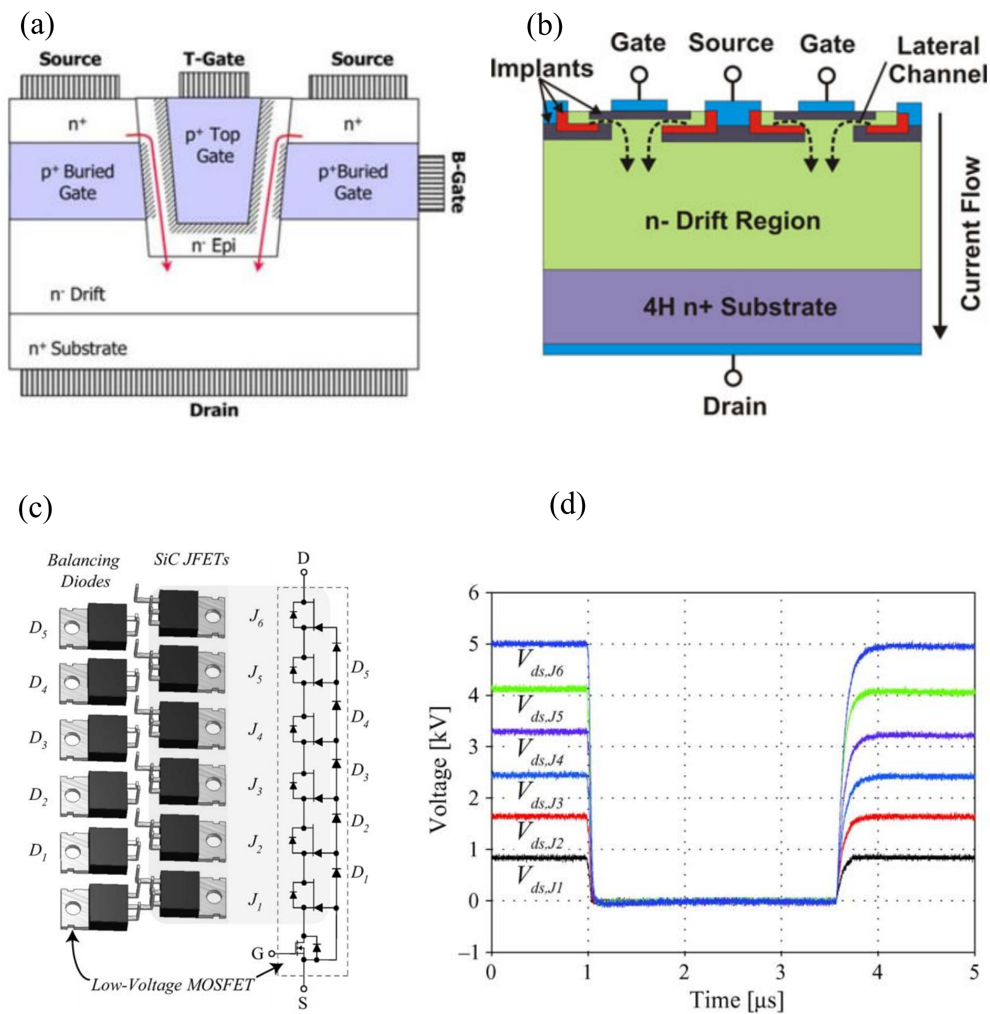
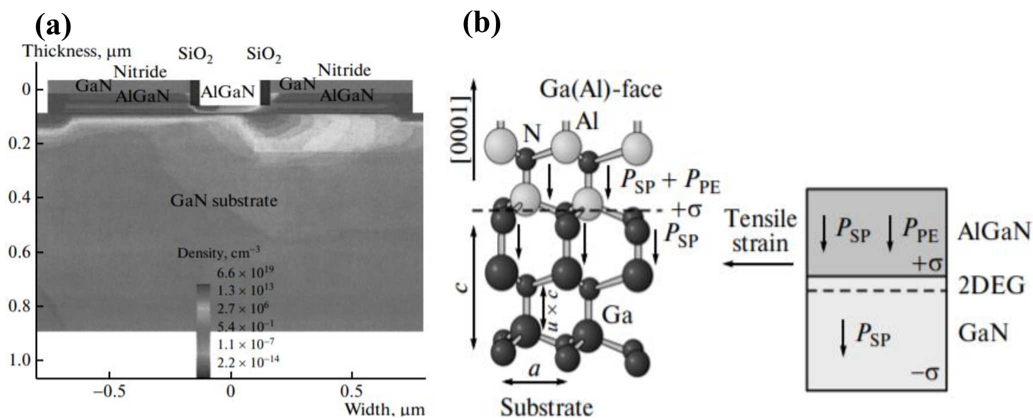


Fig. 1.2 (a) Cross sections of normally-off JFET based on the 4H-SiC and (b) the normally-on SiC JFET with low on-resistance and high breakdown voltage fabricated in vertical structure [3][5]; (c)normally-on high voltage SiC JFET super cascode application combined with six SiC JFETs and a silicon low-voltage MOSFET connected in series. (d) It shows high-speed switching under 5 kV with turn-on time in 50 ns (d) [7].

Gallium nitride-based devices have been used in RF power amplifiers and switching devices [12][13]; GaN epitaxial layers are mainly grown on foreign substrates, especially Si [14], SiC[15], and sapphire. Growing high-quality single crystal gallium nitride thin films is very important for power conversion.

The two-dimensional electron gas (2DEG) formed in AlGaN/GaN heterostructures is one of the most important physical properties that can be applied in power devices, owing to the smaller band gap width of GaN than that of AlGaN. 2DEG can be created in the heterointerface growth of a wide bandgap material over a narrow band gap material, where confinement of electrons in the quantum well is possible (Fig. 1.3 (a)) [16][17]. High electron mobility values (over 2000 $cm^2V^{-1}s^{-1}$) and large 2DEG [18] concentrations owing to the presence of polarization fields [19] and conduction band discontinuity between GaN and AlGaN layers result in the development of heterostructure field-effect transistors (HFETs) [20], high-electron mobility transistors (HEMTs) [21], and MOSFETs. Thus, GaN-based power devices are commercially available with a breakdown voltage in the 20–600 V range and are widely used in small integrated and switch circuits, such as CMOS chip and cascode devices [22] (Fig. 1.2 (b)).



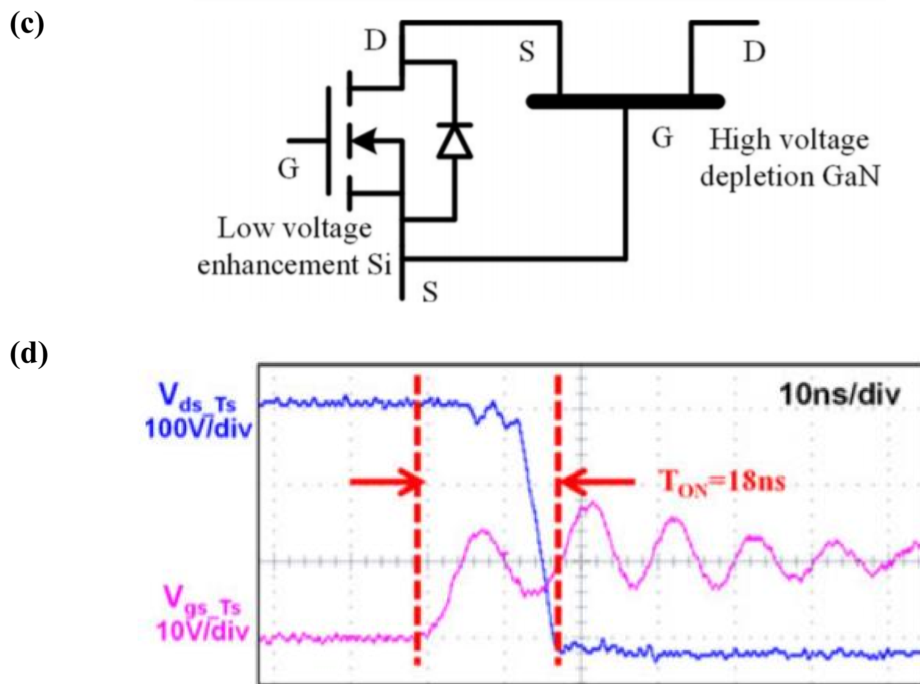


Fig 1.2 (a)Cross sections of AlGaN/GaN based HEMT structure [16]. (b)Crystal structure, polarization effects and 2DEG in the heterointerface of AlGaN/GaN. [16] (c)The normally-on GaN HEMT cascode application combined with low-voltage normally-off Si MOSFET. (d)The turn-on switching waveform of the cascode GaN HEMT [22].

1.2 Diamond

Diamond is not only an expensive gemstone. Owing to its unique physical and electrical properties and a bandgap of 5.5 eV, diamond has become the most promising new-generation semiconductor material beyond SiC and GaN. Natural diamonds are mainly formed approximately 150–200 km deep in the earth. Pure carbon materials crystallize stably under a pressure of 4.5–6×10^9 Pa and temperature of 1100–1600 °C to form

natural diamonds. Generally, only a few places in the deep part of the earth have physical and chemical conditions for diamond formation. Natural diamonds are brought to the surface through the movement of the mantle layer, such as volcanic eruptions. As mentioned in the previous chapter, diamond has excellent electrical properties, such as high thermal conductivity of approximately 2.2 kW m^{-1} K^{-1}, high breakdown field of over 10^7 V cm^{-1}, and high carrier mobility of 2000 $cm^2V^{-1}s^{-1}$. These physical properties make diamonds a potential material for systems such as LED, heat dissipation systems, high-voltage power devices, radio frequency (RF) devices, and sensors. However, as natural diamonds are mined high cost with small quantities, and exist in the form of small single crystals, it is difficult for them to be widely used in electrical and electronic fields.

Artificially synthesized diamonds under low-temperature and low-pressure conditions were first reported by Derjaguin et al. in 1968 [23]. Since then, the development of the preparation technology of diamond substrates has ushered in a revolution in its large-scale application in the regions of semiconductor electronic devices. The mainstream diamond substrate fabrication is divided into high pressure high temperature (HPHT) and chemical vapor deposition (CVD) methods. The HPHT method simulates the formation of natural diamond, where graphite is transformed into a diamond crystal under high temperature of over 1000 °C and pressure above 6 GPa. Impurity concentration and diamond size are difficult to control. On the contrary, compared with the HPHT method, CVD diamond synthesis uses a method that

decomposes hydrocarbon gas mixtures (such as CO_2, CH_4, H_2) into active groups under plasma conditions and deposits diamond on the substrate, where large-size and high-quality diamonds are synthesized on the seed substrate.

1.2.1 Diamond surface modification

The minimum bandgap of diamonds is greater than 5.45 eV and the minimum value of the conduction band is offset from the maximum value of the valence band. In its inherent state, diamond exhibits extremely high resistivity, a semi-insulator physical property. As the conduction band offset is greater than the vacuum energy level, the diamond surface has a negative electron affinity (NEA) characteristic. Moreover, the electron affinity of diamond is sensitive to both crystal orientation and surface impurity termination. For diamond surface modification, the electron affinity is negative for hydrogen-terminated surfaces, but positive electron affinity (PEA) for oxygen-terminated surfaces. This is illustrated by diamond conduction band edge, which is approximately close to the vacuum energy level [24].

Oxygen-terminated diamond can be formed through UV-ozone treatment, oxygen plasma, and oxidation treatment with strong acid at high temperatures, which can generally improve the adhesion of the diamond surface to the dielectric film or metal and is beneficial for the metal electrodes fabrication on the surface. However, the the

high density interface states appeared at oxygen-terminated diamond surface results in high-density interface states, which prohibits the formation of the two-dimensional hole gas conductive layer. This physical property is suitable for isolating each 2DHG diamond device with oxygen termination when fabricating multiple diamond devices on the same diamond substrate.

The diamond surface exhibits NEA through hydrogen termination. The C–H diamond surface has an NEA of approximately 1.3 eV; hence, diamonds with hydrogen-terminated bonds exhibit unique surface conductivity. Energy band bending caused by negative charge adsorption on the C-H surface induces two-dimensional hole gas (2DHG) under the diamond surface. C–H diamonds exhibit a high p-type conductivity.

Fig. 1.3 Bare, hydrogenated, and oxidized diamond band schemes and electron affinity on diamond (100) surface.

Figure 1.4 illustrates the surface modification of diamond. For bare diamond, the outermost carbon atoms in the surface are a 2x1 reconstruction in the form of π bonded. The oxidized diamond shows the same mechanism, where the adsorbates with a higher electronegativity than carbon raise the electron affinity above that of the pure diamond surface. However, those with lower electronegativity than carbon adsorbates, such as H, can terminate the dangling bonds of the carbon atoms on the diamond surface to form the dehydrate. The spontaneous polarization due to the existence of C–H dipoles occurs on the H-terminated surface owing to the difference in electronegativity of hydrogen and carbon, which are 2.1 and 2.5, respectively. The C-H bond is polarized with a positive charge on the top of the C-H diamond surface [25][26] ; the negative charge is excited under the bottom of the carbon atoms. These acceptor-like surface states below the bulk Fermi level contribute to hole accumulation ($\sim 10^{13}$ cm^{-2}) near the surface. The formation of holes with relatively less activation energy is desired. P-type conductivity occurs near the C-H diamond surface has been also discussed on the impurity dopant [27] , acceptor-like surface states[28] or transfer doping model [29].

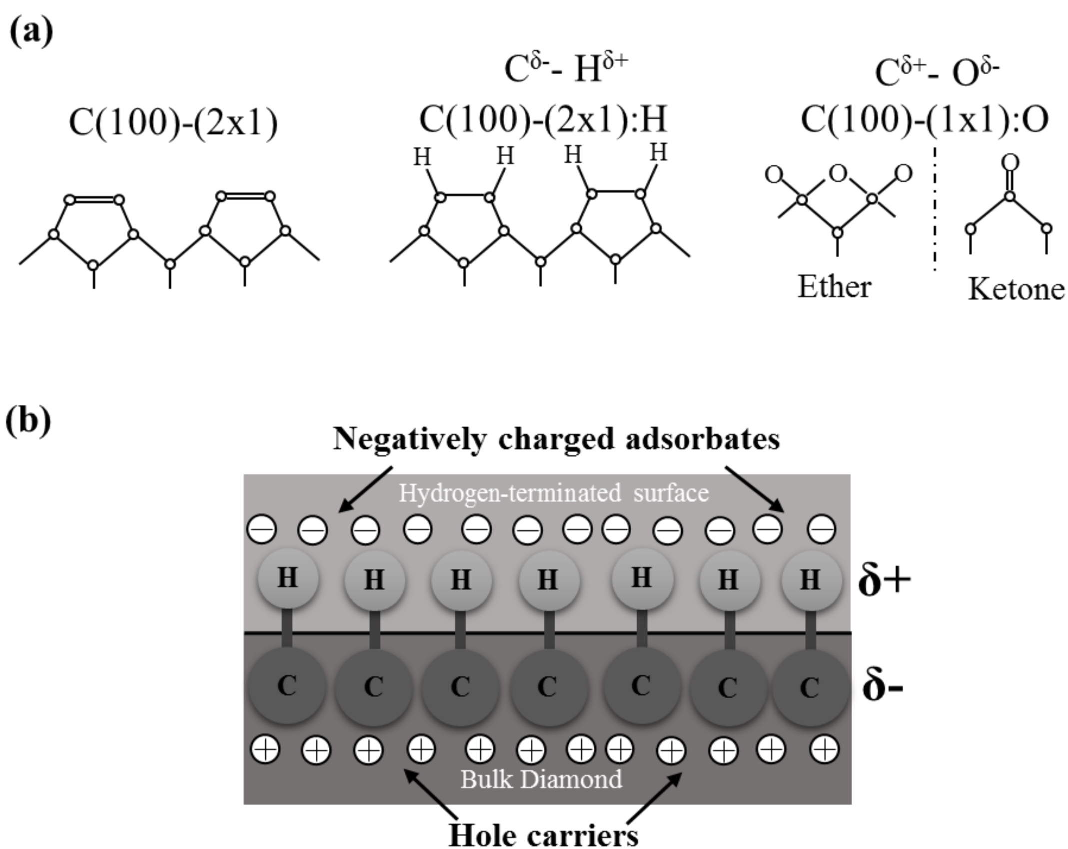


Fig 1.4 (a) Schematic diagram of the atomic arrangement on (100) diamond surface, from left to right, they are bare diamond, hydrogen-terminated diamond, and oxygen-terminated diamond. (b) Spontaneous polarization model of the hydrogen-terminated diamond, where a negatively charged adsorbate induces 2DHG through C-H dipole with different electronegativities.

1.2.2 Hydrogen-terminated diamond FETs

Owing to the unique surface p-type conductivity of C–H diamond, diamond-based p-type enhancement-mode (normally-off), depletion-mode (normally-on) MOSFETs, and metal-semiconductor field-effect transistors (MESFETs) are realized. The p-type enhancement-mode diamond MESFET (Fig. 1.5(a)) was first reported by Kawarada et al. in 1994 [30][31]. This is also the first report on hydrogen-terminated diamond FET characteristics. In this report, homoepitaxial diamond films were deposited on a high-pressure synthetic diamond (001) via the MPCVD at 800℃–900℃ without boron doping. A p-type channel conduction accompanied with hydrogen termination was formed after stop the CO gas supply in the diamond growth via CVD equipment and subsequent plasma treatment with pure hydrogen. The MESFET exhibited normally-off characteristics with a threshold voltage of -2 V (Fig. 1.5 (b)) at room temperature. The enhancement mode of this C-H diamond MESFET because a sufficiently thin conductive layer (speculated to be less than 100nm)is depleted in the channel area by the built-in potential of the Schottky contact. This report has become the basis of the development of a diamond field effect transistor (FET). Although the Schottky contacts of Al are stable at 200 °C in air, surface conduction begins to decrease above 300 °C, which means that the high-temperature C-H MES structure device cannot be realized in air. To make the device work in a high-temperature environment, an oxidation–passivation layer is necessary for diamond devices.

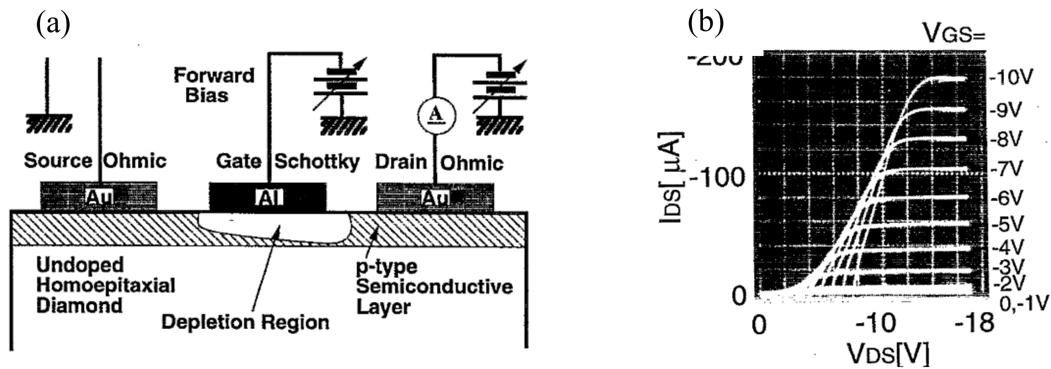


Fig 1.5 (a) Cross-section of the enhancement-mode diamond MESFET using the hydrogen-terminated diamond as a p-type surface semiconducting layer. (b)The Id-Vd characteristic of the p-channel diamond MESFETs with a transconductance of 25 us/mm and threshold voltage of -2 V[30].

Aluminum oxide (Al_2O_3) has a wide band gap, high breakdown voltage, and high dielectric constant. It is an excellent material for gate-insulating films. Initially, alumina was used as a gate insulating film dielectric on a metal-insulator-semiconductor, which was deposited using pulsed laser deposition (PLD) [31]. This prevents the surface of hydrogen termination diamond from being damaged by oxidation with a substrate at high temperature deposition, such as via microwave power vapor deposition (MPCVD) and plasma-enhanced chemical vapor deposition (PECVD). This is unlike high-temperature operations, which use boron as an acceptor in diamond FETs [32][33][34], and where the surface conducting layer is affected by the ambient temperature. In this case, a passivation layer is needed to stabilize the adsorbates and surface C-H bonds, which is important for the temperature stability of 2DHG diamond devices. Although the density of holes can be modulated by the bias voltage applied to the gate at a low

temperature [27], the C-H diamond FET in the 20 K to room temperature range shows a nearly temperature-independent operation [35]. However, the ceiling temperature of the FET operation is also limited by the deposition temperature of the passivation layers [36].

The 2DHG conductivity layer is protected at a high temperature of 550 ℃ air atmosphere covered by an Al_2O_3 passivation film via the atomic layer deposition (ALD) method. The advantage of H_2O as an oxidizing agent is that the reaction between the carbon-hydrogen bond and H_2O and its thermal decomposition are endothermic processes; thus, the alumina deposited by H_2O as an oxidant can be formed at 450 ℃ without damaging the C-H diamond surface, as reported by Hiraiwa et al. [37]. The offset value of the valence band between C-H diamond and Al_2O_3 due to the unoccupied levels in the Al_2O_3 bandgap is below the valence band of diamond (Fig. 1.6 (b)), which leads to a negative fixed charge [38] in the Al_2O_3 film, intensifies the electron potential, and attracts holes at the diamond interface. This is a possible mechanism for inducing 2DHG at the interface of Al_2O_3/C-H diamond. In summary, the high temperature ALD alumina with an H_2O oxidant can substantially improve the stability of the 2DHG diamond MOSFET (Fig. 1.6 (a)) and make the diamond MOSFET operate in a high-temperature environment (Fig. 1.6 (c)) [39] and exhibit high breakdown voltage characteristics [40][41].

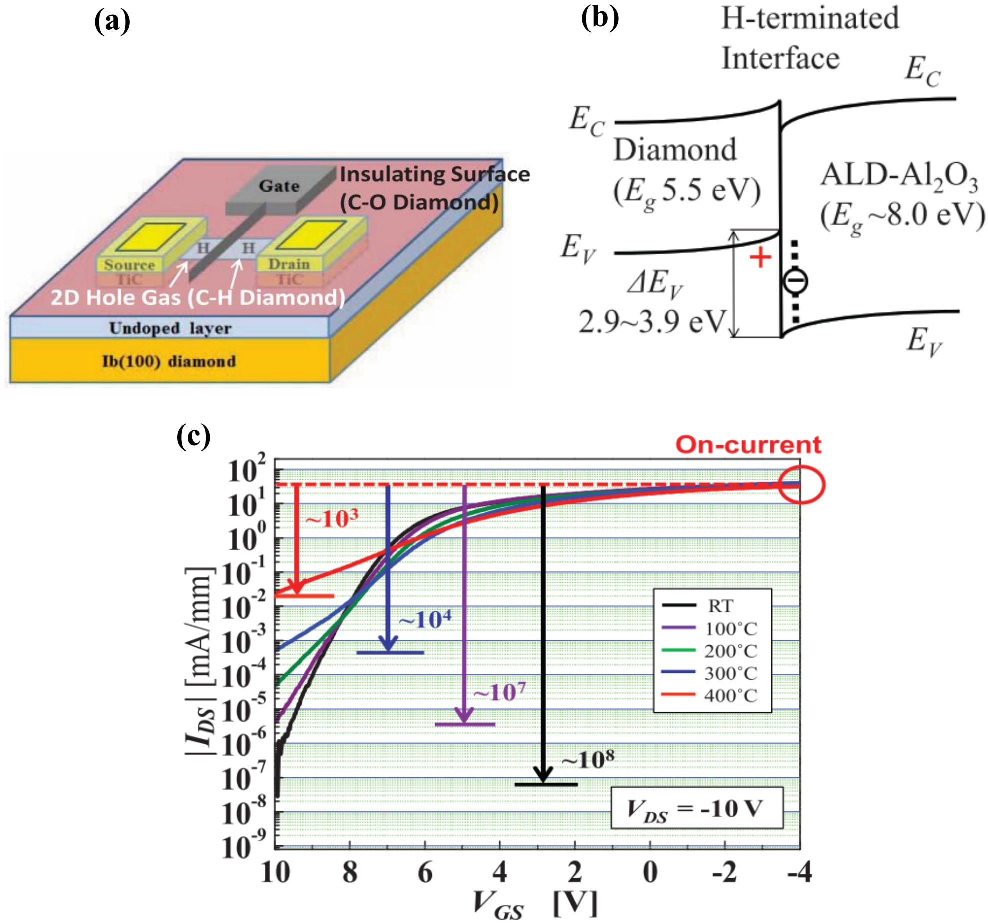


Fig 1.6 (a) Sectional model of diamond MOSFET with a high temperature ALD Al_2O_3 passivation layer. (b)The energy band diagram of the Al_2O_3/C-H diamond and an offset value of the valence band between C-H diamond and Al_2O_3 is 2.9-3.9 eV. (c) ID-VG characteristics of the C-H diamond MOSFET from room temperature to 400℃ [41]

1.2.3 Normally-off operation of the 2DHG diamond FETs

Owing to the negative fixed charge in the alumina insulating film, 2DHG can be induced on the interface of Al_2O_3/C-H diamond even without gate bias. Thus, C-H diamond devices show normally-on characteristics. For a power device, the normally-off characteristic is the key to its application in power systems and integrated circuits;

hence, normally-off operation of C-H diamond MOSFET has become the focus of many studies. For C-H diamond devices, there are two ways to achieve normally-off operation. One is that the formation of 2DHG is affected by the coverage of hydrogen on the diamond surface. If the hydrogen coverage on the surface is reduced and the surface state density with a positive electron affinity surface is increased, the formation of spontaneous polarization 2DHG can be suppressed; thus, changing the threshold voltage of the device to achieve a normally-off operation. Partial C–O channel can achieve the normally-off operation through the reduction of the surface acceptors of the C–H diamond surface conductive layer. This mechanism has been used in metal–insulator FETs (MISFETs) and reported by Umezawa et al. in diamond RF device applications [42], and in diamond MOSFET with an inversion channel (OH terminated channel) with a normally-off operation [43]. However, it is difficult to achieve a high breakdown voltage as the C–O termination is not stable; nevertheless, the partial C–O channel can control the threshold voltage by tuningvalence band maximum Ev effectively.

The normally-off high breakdown voltage diamond MOSFET with partial C–O channel treated by UV/Ozone passivated by ALD-Al_2O_3 film, which was reported by Kitabayashi et al. [44], had a breakdown voltage of over 2000 V at room temperature, the highest breakdown voltage for normally-off 2DHG diamond MOSFET to date.

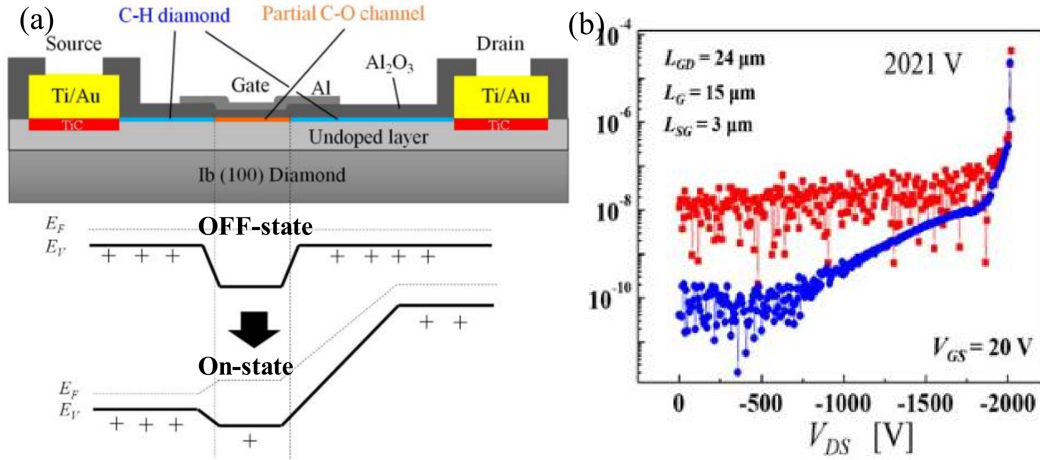


Fig. 1.7 (a) Sectional model of diamond MOSFET with partial C–O channel, where the surface states in the oxygen termination trap the charge on the Ev, which control the hole concentration in the off-state and enable the device operate in normally-off mode.(b) The breakdown characteristics of the partial C–O channel diamond MOSFET with a 24 μm gate-drain length (L_{GD}), and this device shows a breakdown voltage of 2021 V in off-state condition at room temperature[44] .

In addition to the modification on the diamond surface in the channel region of the 2DHG diamond FETs, depleting the accumulation layer of hole carriers in the bulk diamond by adjusting the charge concentration in the insulating film can also achieve normally-off operation. For example, an aluminum oxide insulating film made by a thermal oxidation reaction can reduce the negative fixed charge in the insulating film and the adsorbate on the surface of the C–H diamond, and can realize normally-off operation [45], as shown in Fig. 1.8 (a). On the contrary, using a high dielectric constant (high k) material, such as HfO_2, as an insulating film, enables the contact to change the charge balance on the hydrogen terminal diamond surface and also causes the diamond FET to exhibit normally-off characteristics [46].

The electrical characteristics of the Si-terminated diamond MOSFETs show that a normally-off operation was first reported by W. Fei, T. Bi et al. [47] of the Kawarda

group. The mechanism utilized SiO_2 as an insulating film without any charge when a negative voltage was applied through the gate to induce 2DHG at the bottom of the carbon atoms in the C-Si dipole; thus, achieving a high field-effect mobility (μ_{FE}) FET operating characteristics. It is worth mentioning that as there is no charge in the insulating film, there is no accumulation layer of hole carriers under the C-Si channel when no gate voltage is applied. Detailed research on the physical properties and mechanism of C-Si diamond MOSFETs will be presented in Chapter IV.

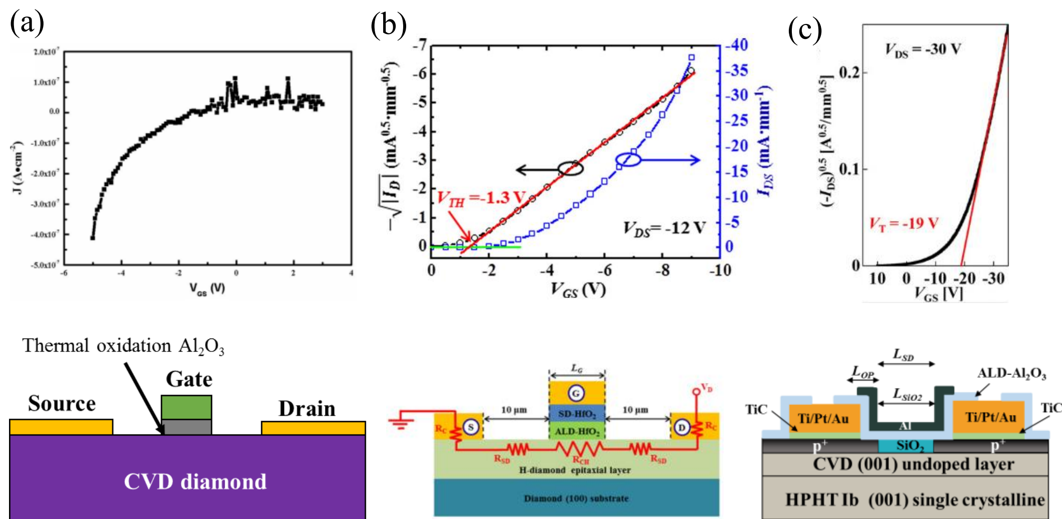


Fig. 1.8 A sectional model of normally-off diamond FETs with different gate insulator and its normally-off operations: (a) the thermal oxidation Al_2O_3 gate insulator diamond MOSFET [45]; (b) the high dielectric constant material gate insulator diamond FET[46]; and (c) the silicon terminated (C-Si bonded) diamond MOSFET with SiO_2 gate insulator[47].

1.2.4 High performance 2DHG diamond power MOSFET applications

The unique p-type conductivity, high hole carrier density, and high thermal conductivity of C-H diamond make it suitable for fabricating high-power FETs as the output power of power devices is not only limited by the manufacturing process, but also by the physical properties of the semiconductor materials. For example, the heating of RF devices at high frequencies limits their power output. In addition, semiconductor materials with high thermal conductivity and high carrier mobility substantially improve power output and reduce power loss [48]. High saturation velocity may ensure that devices operate at higher operating frequencies [49].

In the manufacturing processes, reducing the size of the device or reducing the thickness of the insulating film can improve the current and power outputs, which is reflected in the microwave power MOSFET based on C–H diamond. C-H diamond RF power MOSFET with a maximum output power density of 2.14 W/mm at 1 GHz has been reported [50]. The RF diamond MOSFET with highest large-signal output power density of 3.8 W/mm has been reported in 2019. It has the highest carrier velocity of 1×10^7 cm/s in small-signal performance with $L_G = 0.5$ μm. These indexes are also the highest among p-type MOSFET[51].

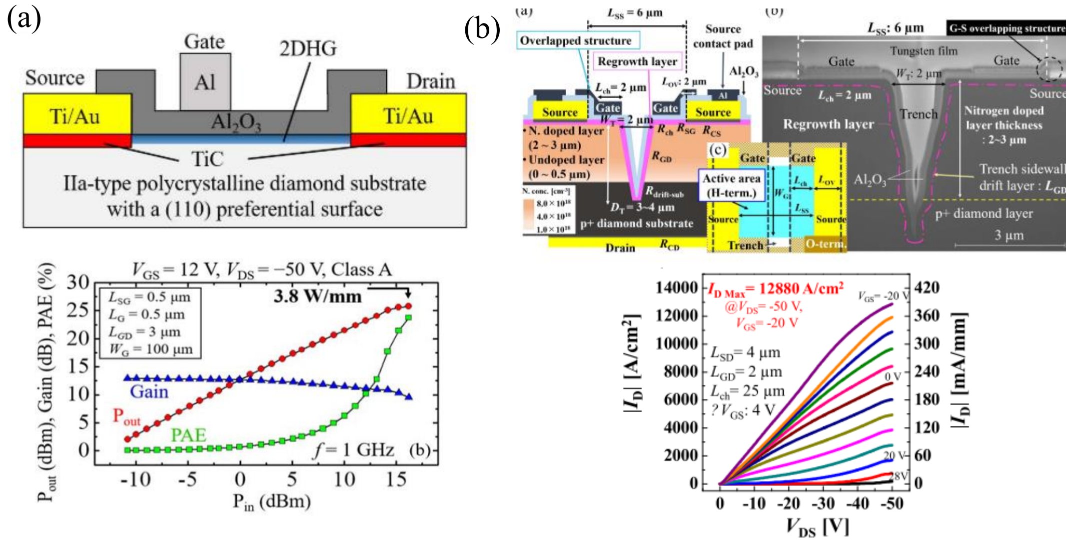


Fig. 1.9 (a) The lateral-type RF C-H diamond MOSFET with output power density of 3.8 W/mm, which is the highest in the diamond-based RF devices [51]; (b) V-shaped trench structure vertical-type diamond MOSFET with specific low on-resistance and high drain current density [54].

The formation of 2DHG is independent of the crystal direction of diamond [29]; thus, C-H diamond can also be used for the fabrication of vertical-type devices. Vertical-type devices are widely used in GaN and SiC devices. The vertical structure allows the source and drain of MOSFETs to be not fabricated on the same surface of the semiconductor substrate, which can improve the device integration on the same substrate, and is beneficial for the fabrication of high-current power devices with large gate widths. In diamond-based FETs, the primordial vertical structure FETs [52], which have been proposed as junction FETs. The vertical-type diamond MOSFETs with trench structures have been developed and measured by the Waseda University group. [52][53].

Fig. 1.9 (b) shows the 2DHG vertical-type MOSFET with a V-shaped trench structure,

which was achieved specific on-resistance of 3.2 mΩcm^2 with an overlapping gate between gate-source electrode and a high drain current density of over 12000 A/cm^2.[54]

Although p-type diamond devices have been fully demonstrated and developed, the n-type doping of diamond is still challenging due to the phosphorous deep donor at 0.57 eV [55]; thus, the electrical characteristics of n-type diamond devices need to be evaluated. However, 2DHG diamond devices can still be used as excellent p-type devices in CMOS and semiconductor circuits combined with GaN or SiC n-channel power devices. Owing to their excellent thermal conductivity and good insulation characteristics with bare diamond, a CMOS inverter semiconductor circuit based on a diamond MOSFET and GaN HEMT fabricated on one diamond substrate is expected for next-generation CMOS switching circuits (Fig.1.10).

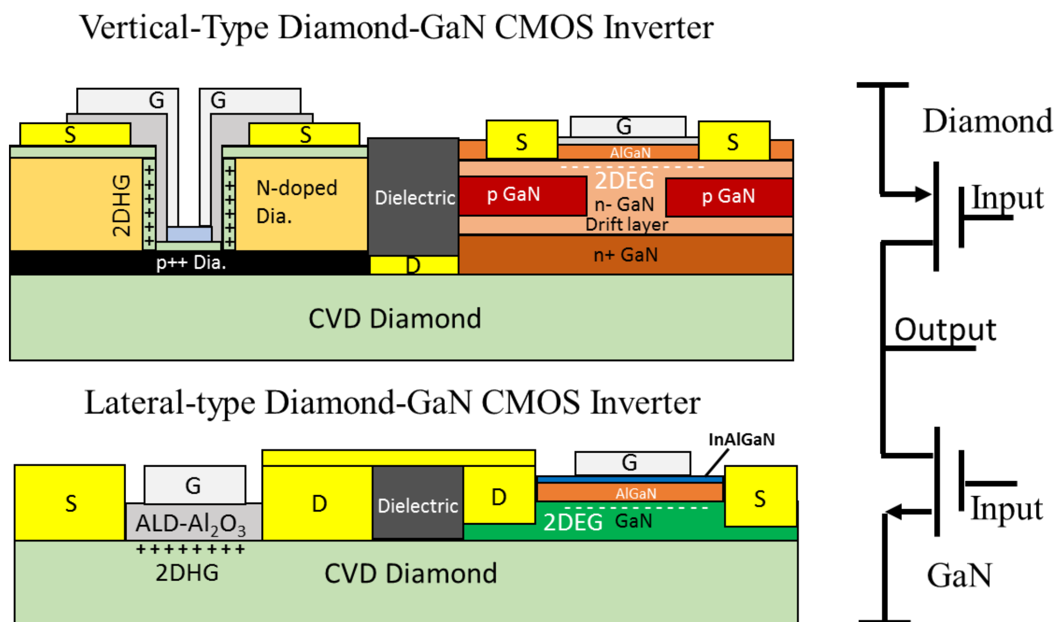


Fig. 1.10 Proposed schematic diagram of two types diamond-GaN CMOS inverter with common drain output structure.

1.3 Advantages of diamond in the Development of Society 5.0

With the invention of generators in the mid-19th century, mankind began to enter the electrical age. The use and invention of electricity marked the gradual integration of science and technology and the macroscopic application of electricity. With the development of the semiconductor industry, human beings have made significant progress in various fields of the third scientific and technological revolution. The application of semiconductor devices in research has enabled human beings to apply electricity the micro field.

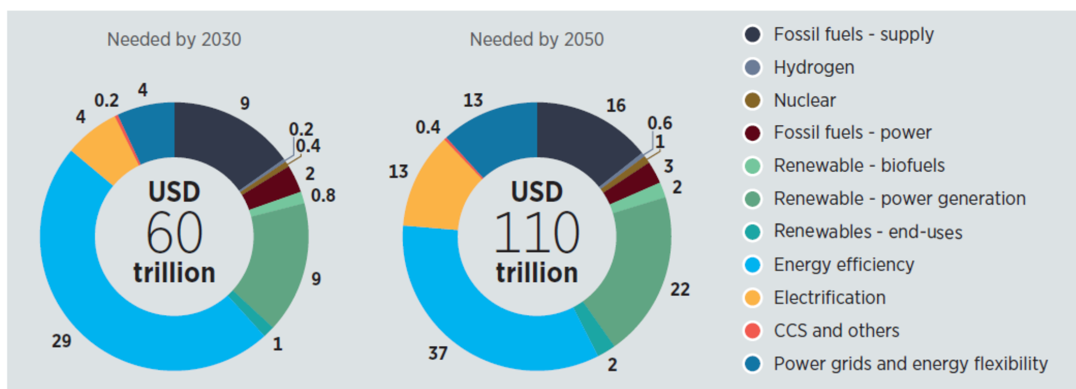


Fig. 1.11 Proportion of global investment in energy between 2030 and 2050 based on the forecast of the International Renewable Energy Agency. The proportion of financial investment in renewable energy and energy efficiency will be substantially increased. (Data source: International Renewable Energy Agency, 2020b)[57].

The next scientific and technological revolution will lead the world to the Internet of Things (IoT) era. The world's energy demand will shift from low-carbon to renewable and cleaner energy. Electricity liberalization will be the infrastructure for building Society 5.0 [56]. According to the global energy budget financial report released by

The International Renewable Energy Agency (IRENA) in 2020 (Fig. 1.11) [57], from 2030 to 2050, the global budget ratio for renewable energy and energy conversion efficiency will increase exponentially, which means that more focus will be given to renewable energy (wind power, geothermal power, solar energy) and energy saving systems (such as inverter and transformer) in the future [58]. These fields of science and technology need the support of semiconductor technology. As mentioned above, due to the limitations of traditional semiconductor materials, semiconductor materials with better physical properties will become the key to the future of science and technology.

Diamonds have the highest breakdown electric field and thermal conductivity among semiconductor materials at present, which makes diamond power devices suitable in high-voltage and intrinsic carrier density, where other semiconductors cannot work. These make diamond advantageous in geothermal and bandgap. It is worth noting that the raw materials required for the synthesis of diamonds are all renewable resources. CO_2 and CH_4 can be separated and purified from greenhouse gas and biogas, respectively, while hydrogen can be obtained by electrolyzing water through solar energy or wind power. In the context of low-carbon society and carbon fixation, diamond can be used as a renewable next-generation semiconductor material, and the market share of diamond semiconductor devices will substantially increase in the future. In addition, in the context of energy conversion rate, utilizing the physical properties of diamond's high carrier mobility, the high-frequency and high-voltage inverter

manufactured by diamond power devices will be indispensable for reducing energy loss and improving power generation efficiency. The development and research of high-performance diamond power devices will reduce the utilization cost of renewable energy and improve the efficiency of energy utilization in the future.

In this doctoral thesis, the fabrication and evaluation of diamond power devices, circuit application technology (such as cascode and inverter circuits), and the fabrication and operation analysis of the high-performance normally-off diamond power device will be discussed.

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Chapter 2

Current enhanced Hydrogen termination diamond MOSFETs

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2.1 Gate width Enlarged Hydrogen-terminated diamond MOSFET

. Diamond power devices can be created by modifying the surface of diamonds, and the hole density on hydrogen-terminated diamond surfaces is approximately 10^{13} cm^{-2}. A C–H surface can be used as a p-channel FET.

For applications involving high-voltage switching circuits such as inverters, it is important to design power devices with high withstand voltages and high output currents. To realize the high output current of diamond devices and reduce the two-dimensional size of the devices, it is extremely effective to use metal with a high work function as an electrode metal to reduce the ON resistance (Ron) to enhance the current capability of diamond MOSFETs. Generally, the maximum current of a MOSFET can be expressed as follows:

$$I_{Dmax} = \frac{1}{L_G}\mu C_G(V_{GS} - V_T - \frac{V_{DS}}{2})(V_{DS} - I_{Dmax}R_{SD}) \text{.......... I}$$

In this formula, μ, C_G, and R_{SD} are the mobility, gate capacitance, and series resistance between the source and drain electrodes, respectively. It is clear that the output current can be increased by decreasing the gate length (L_G) and decreasing the thickness of the insulating film to increase the C_G. Furthermore, the mobility μ of a C–H diamond MOSFET on a (100) diamond is approximately 100 $cm^2V^{-1}s^{-1}$[1][2], and I_{Dmax} can be increased by increasing the channel mobility, such as using CVD diamond with less nitrogen content or using a diamond substrate with a different crystal orientation such

as IIa (111) diamond etc.; additionally, using an insulating film with a smaller dielectric constant can improve the mobility. In the linear region, I_D can be derived from formula I as follows:

$$I_D = W_G \mu C_G (V_G - V_T) \frac{V_{DS}}{L_G} \text{....................II}$$

As shown in Equation II, a direct relationship exists between I_D and the gate width in switching devices and inverter circuits. MOSFET devices operate in the on state (linear region) when switching at high frequency; therefore, increasing W_G is the most direct solution for enhancing the MOSFET output current. This chapter focuses on the fabrication and electrical characteristic analysis of lateral- and vertical-type diamond MOSFETs with large W_G.

2.2 Lateral-type C–H diamond MOSFETs

A high-pressure high-temperature (HPHT) synthetic Ib (001) diamond substrate was used to fabricate lateral-type C–H diamond MOSFETs. After grinding and polishing, the average surface roughness (Ra) of the substrate was approximately 3.3 nm with obvious polishing vestiges. To reduce the roughness of the diamond surface and the concentration of nitrogen and boron in Ib-type diamond substrate, a homoepitaxial undoped diamond layer of 500 nm thickness was deposited on the diamond substrate via microwave plasma chemical vapor deposition (MPCVD) in the presence of the following gases: H_2, 394 sccm; CH_4, 3 sccm; CO_2, 3 sccm. (H_2:CH_4:CO_2 = 98.5%:0.75%:0.75%). The power of the microwave plasma was 750 W, and the chamber pressure and temperature during growth were 35 Torr and 600 °C, respectively, after the diamond substrates were processed with hot mixed acid treatment (H_2SO_4:HNO_3 = 3:1) at 240 °C and subsequently cleaned with an organic solvent.

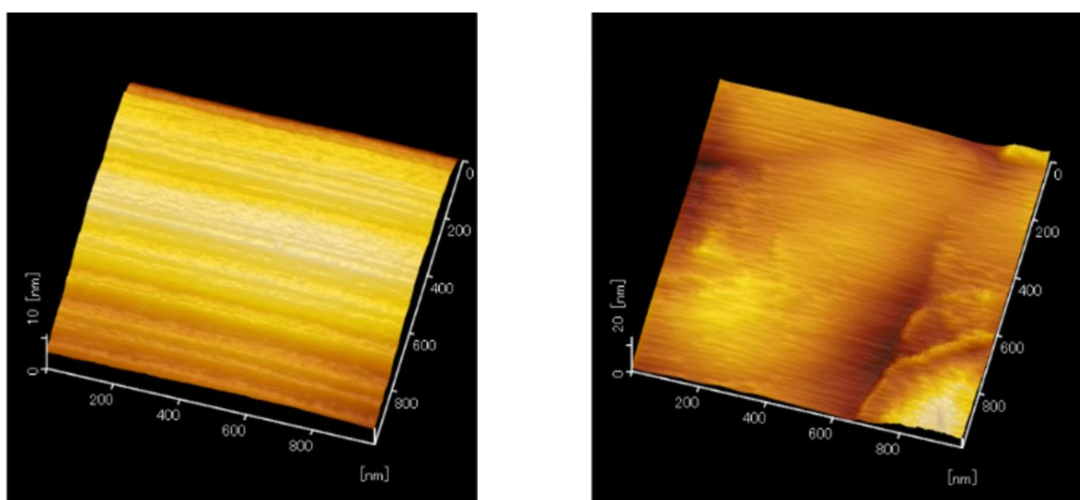


Fig 2.1 The AFM mapping of the diamond substrate (a) after polishing with Ra = 3.3 nm. (b) After homoepitaxial growth with Ra = 0.16 nm.

The average surface roughness was 0.16 nm, and the atomic force microscopy (AFM) 3D mapping of this substrate in a 1 μm × 1 μm region is shown in Fig 2.1 (b). According to previous reports, the concentration of nitrogen and boron in undoped homoepitaxial growth diamond are 2×10^{16} and 2×10^{14} cm^{-3} , respectively[3].

The H_2 that may exist on the diamond surface was removed through UV irradiation in an O_3 atmosphere for 3 h to form oxygen terminals on the diamond surface. The oxidized diamond surface will increase the adhesion strength between the diamond and electrode metal. The electrode area was patterned via photolithography using a high-sensitivity photoresist TSMR-27cp and PMGI. The total thickness of the photoresist exceeded 2 μm. Theoretically, metal electrodes smaller than this thickness can be fabricated. However, to lift-off smoothly, the total thickness of the metal plated by the electron beam deposition system should be significantly smaller than that of the photoresist (source and drain electrodes: Ti/Pt/Au = 20/30/100 nm). All patterning were performed via photolithography, and the description will be omitted in the subsequent manufacturing processes.

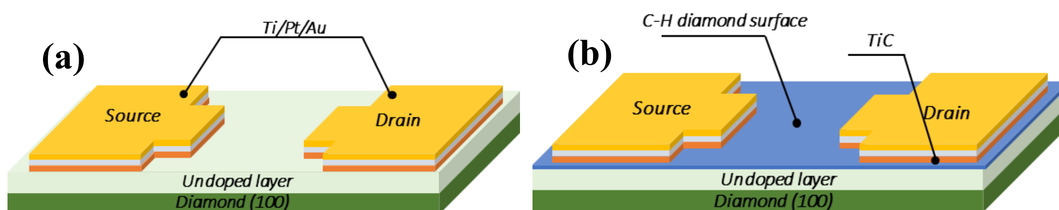


Fig. 2.2 (a) Metal electrodes deposited using electron beam deposition system with Ti/Pt/Au=20/30/100 nm. (b) TiC formed on diamond/Ti interface during annealing with H_2 at 500 °C, and hydrogen-termination was formed via MPCVD using hydrogen plasma.

The diamond substrate with the Ti/Pt/Au electrode was annealed in a H_2 atmosphere for 30 min at 500 °C. During this condition, TiC was situated between the diamond substrate and the electrode. TiC increases the adhesion of metal electrodes and reduces the Ohmic resistance of the source and drain, whereas the C–H diamond surface for the conductive channel was formed at 600 °C by point-arc remote plasma chemical vapor deposition (point-arc MPCVD) with 100 sccm of H_2 gas and the C–H diamond surface as the conductive channel formed by point-arc MPCVD with a microwave power of 70 W. Hydrogen plasma can be lit at a power of 60 W, and under high temperature and plasma, hydrogen termination can be formed on the diamond surface in point-arc MPCVD (as shown in Fig. 2.2 (b)).

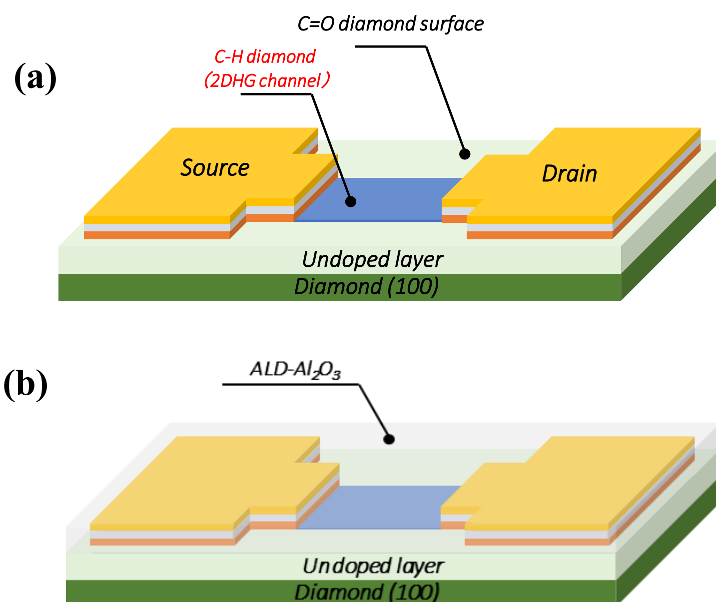


Fig 2.3 (a) The isolation process by the oxygen plasma and the (b)200nm high temperature ALD-Al_2O_3 passivation layer for gate insulator

To isolate the MOSFETs fabricated on the same substrate from each other, the hydrogen terminal outside the channel area of each MOSFET was removed using oxygen plasma. Furthermore, because the widths of the hydrogen-terminated area covered by the photoresist were different, the MOSFET in this experiment had different gate widths, ranging from 25 to 500 µm (Fig. 2.3 (a)). After the isolation process, all the devices were covered by an Al_2O_3 passivation film via atomic layer deposition (ALD) at 450 °C using H_2O as an oxidant (Fig 2.3 (b)).

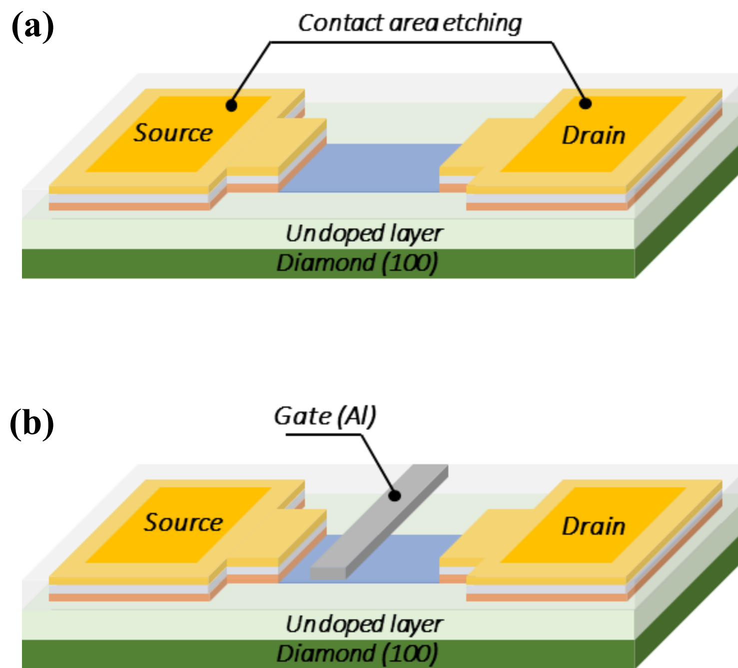


Fig 2.4 (a)Passivation layer on source/drain region etched via NMD-3 for contact area. (b) Aluminum gate deposited by thermal evaporation system.

After the passivation layer on the source/drain region was etched by NMD-3 for the contact area with NMD-3 of 2.38%, a 100 nm aluminum layer was deposited via vacuum evaporation for the gate electrode (Figs. 2.4 (a) and (b)), and the MOSFET fabrication was completed. The top views of the C–H diamond MOSFET were obtained using optical microscopy and are shown in Fig. 2.5 (a). A sectional model of the diamond MOSFET is shown in Fig. 2.5 (b); the source–gate lengths (L_{GS}) and L_G for all of the C–H diamond devices were 2 and 4 μm, respectively, resulting in MOSFETs with high breakdown voltages and gate–drain lengths between 15 and 20 μm.

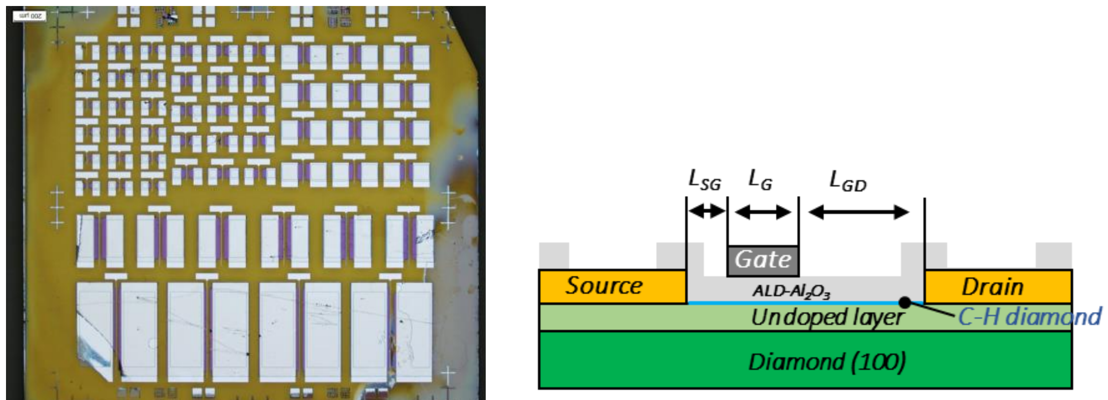


Fig 2.5 (a) C–H diamond MOSFETs on Ib (100) diamond substrate; WG of each substrate region was 25, 50, 100, 250, and 500 μm. (b) Sectional model of lateral-type C–H diamond MOSFETs in this work.

2.2.1 Electric characteristic of lateral-type C–H diamond MOSFETs

The DC electric characteristics of lateral-type C–H diamond MOSFETs were tested using a semiconductor device analyzer (Precision Current–Voltage Analyzer Series (B1500a, Keysight). Because the devices on the same substrate are affected by the experimental environment in the manufacturing process, such as plasma strength, temperature, and contact quality after annealing of metal electrodes, the DC electrical characteristics of small-sized devices will exhibit individual differences. Therefore, in this section, the characteristics of representative devices of different sizes will be described.

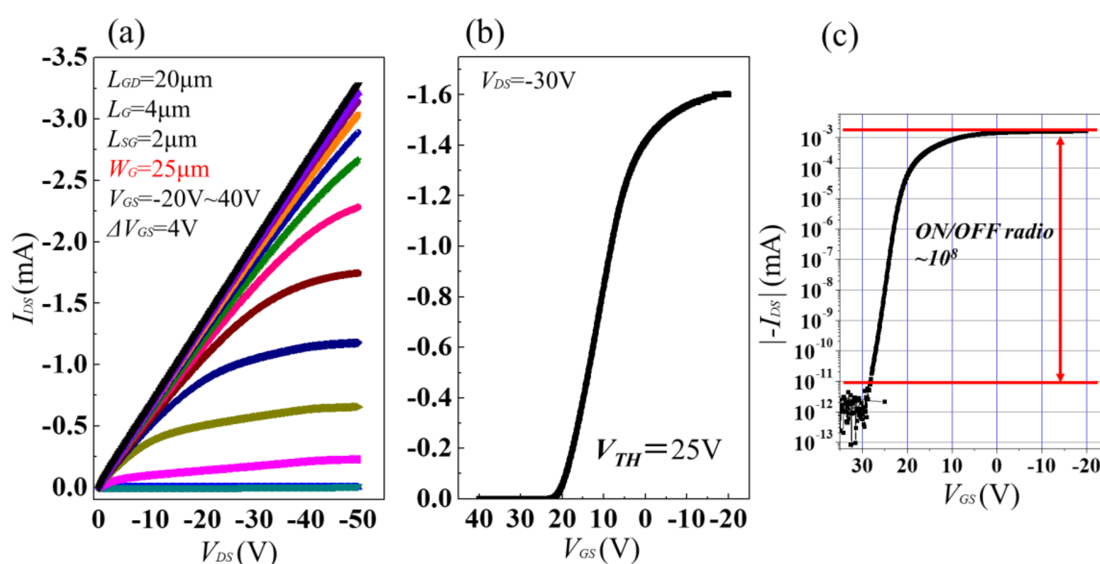


Fig 2.6 DC electric characteristics of lateral-type C-H diamond MOSFETs with W_G = 25 μm; I_{DS}–V_{DS} characteristic curve showing (a) I_{DMAX} of -3.4 mA @ V_{GS} = -20 V and V_{DS} = -50 V. This device shows V_{TH} = 25 V in the I_{GS}–V_{GS} characteristic curve (b), and (c) on/off ratio exceeding 10^8.

The I_{DS}–V_{DS} and I_{GS}–V_{GS} characteristic curves of the C–H diamond MOSFETs with W_G = 25 μm are shown in Figs. 2.6 (a) (b), At V_{GS} = -20 V and V_{DS} = -50 V, the maximum drain current of this device was -3.4 mA, the maximum current density was -136 mm/mA, and the maximum transconductance g_m was 4.1 mS/mm at V_{DS} = -15 V. To reflect the device's current capability more intuitively, the electrical characteristics of other devices are based on the current value as the ordinate. This MOSFET exhibited normal operation owing to the polarization effect at the hydrogen-terminated diamond and Al_2O_3 interface, resulting in 2DHG attraction in the channel region, even without a negative gate bias. By applying a positive gate voltage to the gate, the channel's hole can be neutralized, the device turns off, and the MOSFET shows an on/off ratio exceeding 10^8 at room temperature.

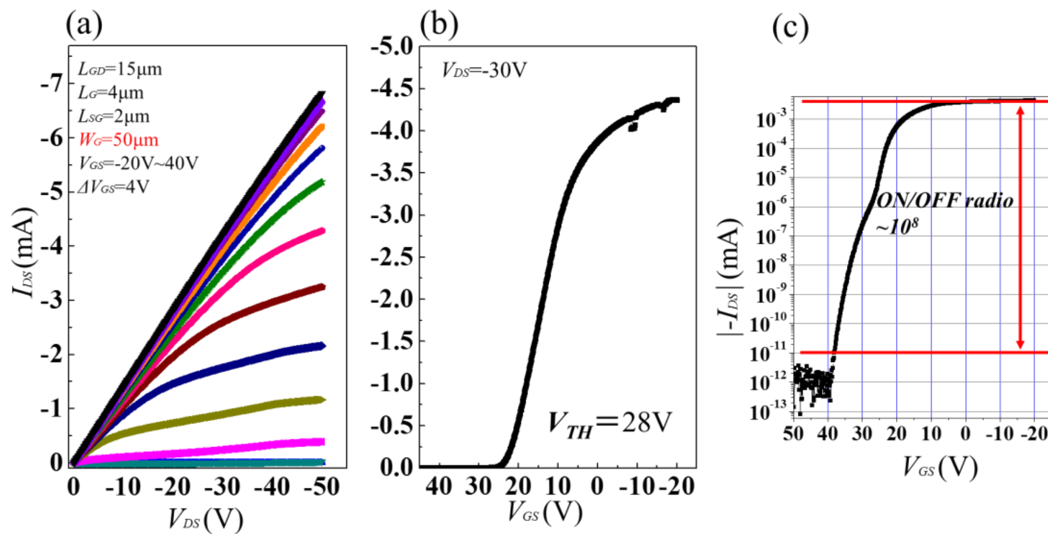


Fig. 2.7 Characteristic curves of C–H diamond MOSFETs with W_G = 50 μm; I_{DS}–V_{DS} characteristic curves showing (a) I_{DMAX} of -7.1 mA @ V_{GS} = -20 V and V_{DS} = -50 V, and maximum g_m was 4.9 mS/mm at V_{DS} = -15 V. This device shows V_{TH} = 28 V in I_{GS}–V_{GS} characteristic curve (b), and (c) on/off ratio exceeding 10^8.

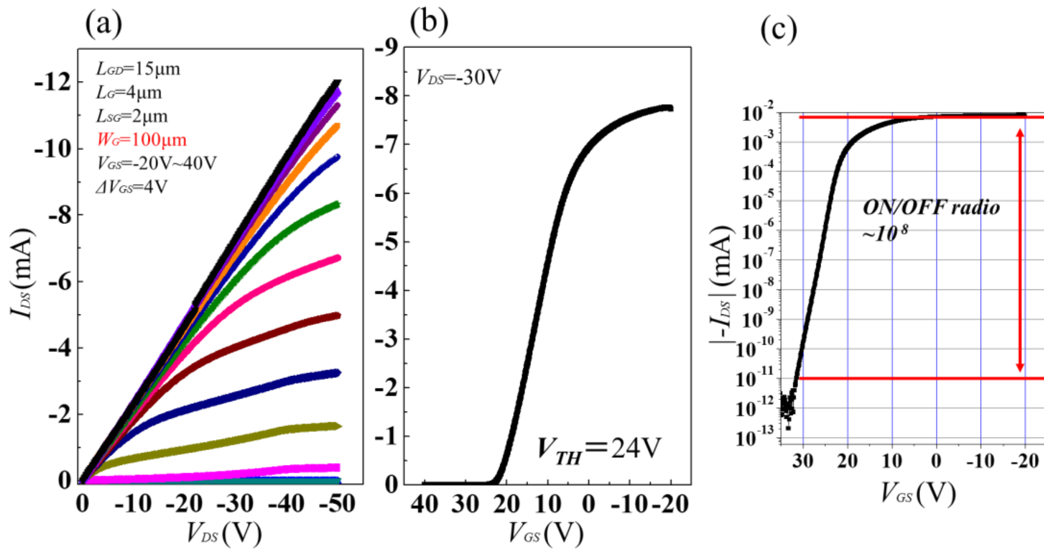


Fig. 2.8 Characteristic curves of C–H diamond MOSFETs with W_G = 100 µm; I_{DS}–V_{DS} characteristic curves showing (a) I_{DMAX} of -12.3 mA @ V_{GS} = -20 V and V_{DS} = -50 V; maximum g_m was 4.1 mS/mm at V_{DS} = -15 V. This device shows V_{TH} = 24 V in I_{GS}–V_{GS} characteristic curve (b), and (c) on/off ratio exceeding 10^8.

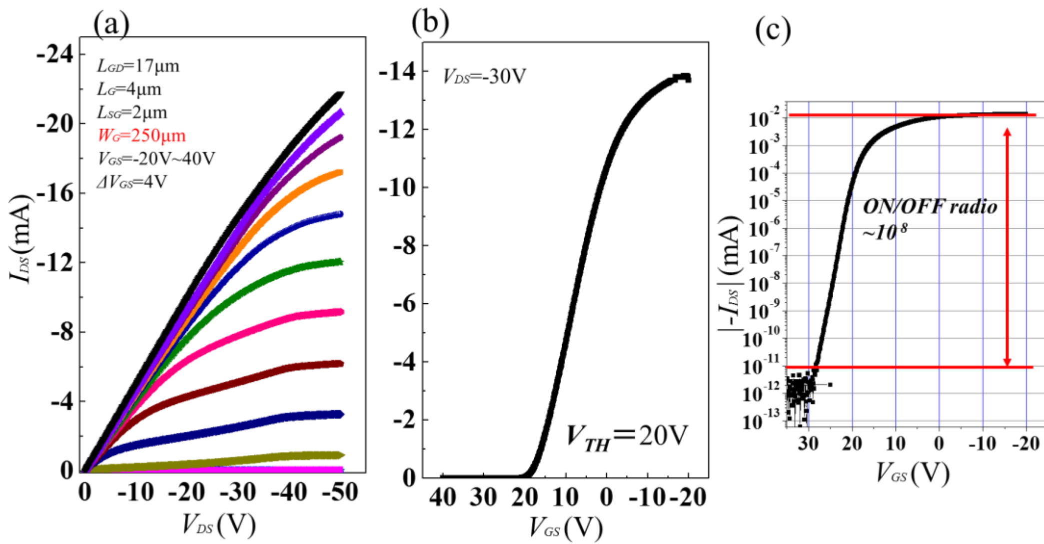


Fig. 2.9 Characteristic curves of C–H diamond MOSFETs with W_G = 250 µm; I_{DS}–V_{DS} characteristic curves showing (a) I_{DMAX} of -22 mA @ V_{GS} = -20 V and V_{DS} = -50 V; maximum g_m was 4.1 mS/mm at V_{DS} = -15 V. This device shows V_{TH} = 20 V in I_{GS}–V_{GS} characteristic curve (b), and (c) on/off ratio exceeding 10^8.

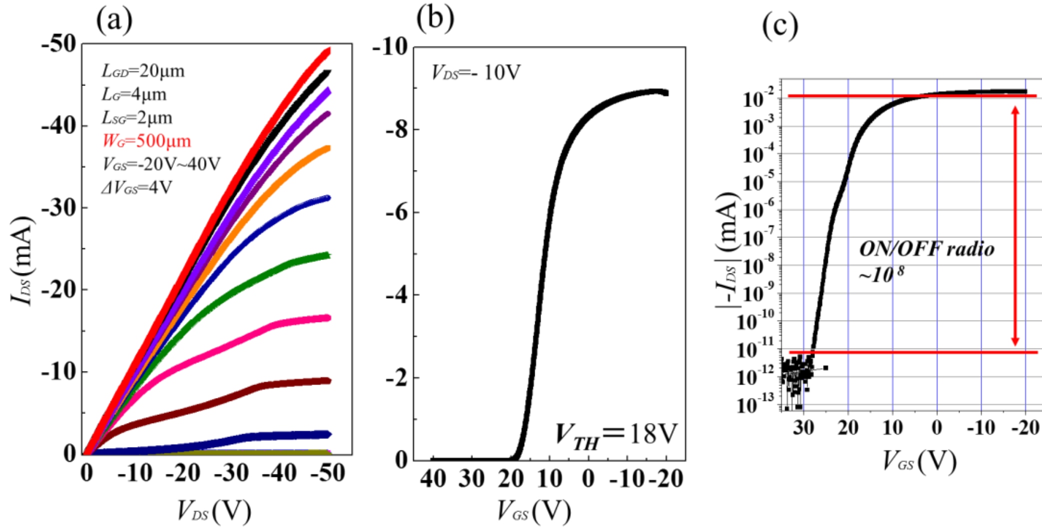


Fig. 2.10 Characteristic curves of C–H diamond MOSFETs with W_G = 500 μm; I_{DS}–V_{DS} characteristic curve showing (a) I_{DMAX} of -50 mA @ V_{GS} = -20 V and V_{DS} = -50 V; maximum g_m was 3.36 mS/mm at V_{DS} = -15 V. This device shows V_{TH} = -18 V in I_{GS}–V_{GS} characteristic curve (b), and (c) on/off ratio exceeding 10^8.

The DC characteristics of the C–H diamond MOSFETs with gate widths ranging from 50 to 500 μm are shown in Figs. 2.7 to 2.10. In the I_{DS}–V_{DS} characteristic curve of devices with gate widths ranging from 50 to 500 μm, it was observed that the increasing rate of the maximum current value of MOSFETs was proportional to the gate width. With the widening of the gate width, the current output capacity of the devices increased proportionally. In the I_{GS}–V_{GS} characteristic curve, the threshold voltage was maintained at almost the same level, and all showed normal operation. This suggests that the gate's ability to modulate the drain current does not affect the gate width of the MOSFETs. In general, a longer gate length enables the drain current to reach the saturation region faster and reduce the threshold voltage (rendering the device easier to turn off).

The diamond MOSFET with a gate width of 500 μm is shown in Fig. 2.8. The maximum current value reached -50 mA, and the drain current value was more than twice that of the MOSFET with a gate width of 250 μm. Generally, during device fabrication, the device's performance in the periphery of the diamond substrate is worse than that in the middle of the substrate. The roughness of the substrate around the diamond is greater than that in the center during the homoepitaxial growth in MPCVD, which may result in an increase in the resistance of the channel area of the MOSFET and decrease the output current. However, the MOSFET still exhibits normal p-type operating characteristics and operates normally with an on/off ratio of 10^8.

By enlarging the gate width of lateral-type C–H diamond MOSFETs, the drain current of the device is increased significantly. Theoretically, a MOSFET with a larger current can be obtained by expanding the gate width, but the first pass yield (FPY) will be affected by the manufacturing process. The planar structure of lateral-type MOSFETs causes the electrode metal to occupy a larger area, thereby limiting the number of devices that can be fabricated on the same substrate.

2.3 Vertical-type C–H diamond MOSFETs

Because C-H diamond possesses surface conductivity, implying that the formation of 2DHG is independent of the diamond surface direction, the diamond vertical-type device can be realized using a C–H p-type conductive channel formed by the sidewall. Because the source and drain metal electrodes can be formed on different sides (upper and backside) of the diamond substrate, this three-dimensional structure is suitable for fabricating large gate width MOSFETs. Herein, the fabrication of a vertical-type diamond MOSFET with a multi-trench series structure and its electrical characteristics are analyzed.

A 3 mm × 3 mm × 0.5 mm IIb (100) single crystalline diamond substrate was used to fabricate vertical-type diamond MOSFETs; the diamond substrate was doped heavily with boron at a concentration of ~10^{21}/cm^3. It differs from lateral-type MOSFETs; vertical-type MOSFETs require that the diamond in contact with the drain electrode in the backside to possess conductivity. The electric resistance of this boron doped (100) diamond substrate is approximately 0.10–0.05 Ω·cm. After the diamond substrates were processed using a hot mixed acid and organic solvent treatment, a 500 nm homoepitaxial undoped diamond layer was deposited via MPCVD under high-speed homoepitaxial growth conditions (170 nm/min) using the following gas ratio, i.e., H_2:CH_4:CO_2 = 98.5%:0.75%:0.75%, after that hot mixed acid treatment was performed again to remove graphite that may be synthesized during the growth process (Fig. 2.11

(a)).

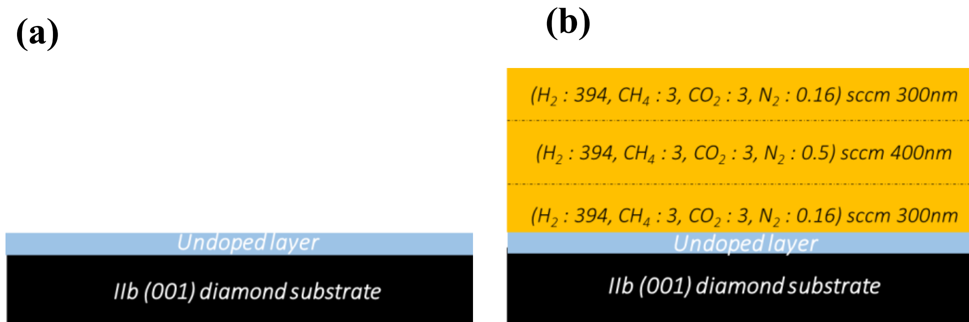


Fig. 2.11 (a) 500 nm homoepitaxial undoped diamond layer via MPCVD on IIb (001) diamond substrate. (b) To prevent leakage current in longitudinal direction of vertical-type C–H diamond MOSFETs, nitrogen-doped epitaxial diamond layers with different nitrogen concentration was deposited after undoped layer was fabricated.

To prevent leakage current from passing through bulk diamond in vertical-type C–H diamond MOSFETs, three layers of nitrogen-doped epitaxial diamond layers were deposited on the undoped layer, and the doping concentration was controlled by controlling the flow rate of NO_2 gas during MPCVD (Fig. 2.11 (b)). The average nitrogen concentration of the three nitrogen-doped diamond layers was approximately $10^{19}/cm^3$. The temperature, microwave power, and chamber pressure during the diamond growth were 600 °C, 750 W, and 35 Torr, respectively. The Fermi level can be maintained above the intrinsic Fermi level owing to the nitrogen deep donor with an activation energy of 1.7 eV. Therefore, the nitrogen-doped diamond layers can block the leakage current caused by 2DHG induced by the Al_2O_3/C–H diamond interface, which is crucial for reducing the leakage current of vertical-type C–H diamond MOSFETs after turning off and enlarging the drift layer region length to increase the

breakdown voltage [4].

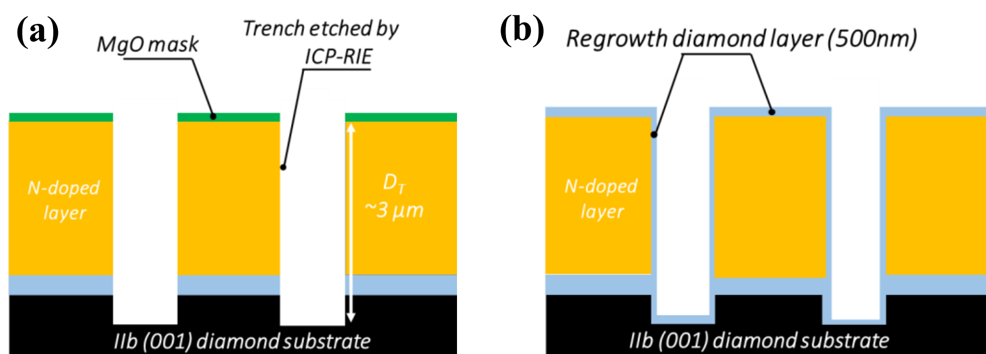


Fig. 2.12 (a) Multiple-trench structure etched by oxygen plasma in ICP–RIE with MgO mask; depth of the each trench was ~ 3 µm. (b)a 500nm regrowth diamond layer deposited via MPCVD; undoped diamond layer on side wall of trench was proposed to induce 2DHG after hydrogen termination and formed p-channel for vertical-type C–H diamond MOSFETs.

The MgO mask for the trench etching process was deposited using a Dual-Ion-Beam-Sputtering system (DIBS), and the MgO layer thickness was 150 nm. The trench was patterned via lithography, and the multiple-trench structure was fabricated using oxygen plasma via ICP-RIE. The depth of each trench (D_T) was ~ 3 µm, and the value of D_T depended on the total thickness of the homoepitaxial diamond layer on the p-type diamond substrate. For the current to reach the drain electrode, D_T must be larger than the total thickness of the homo-epigenetic diamond layer. The MgO mask after the ICP-RIE process can be removed by pure water in the ultrasonic cleaning.

After the trench structures were fabricated as shown in Fig. 2.12 (a), a 500 nm fixed regrowth undoped diamond layer was deposited again to reduce the damage and roughness on the trench sidewall during ICP-RIE (Fig. 2.12 (b)). This undoped diamond

layer was proposed to induce the 2DHG channel vertically.

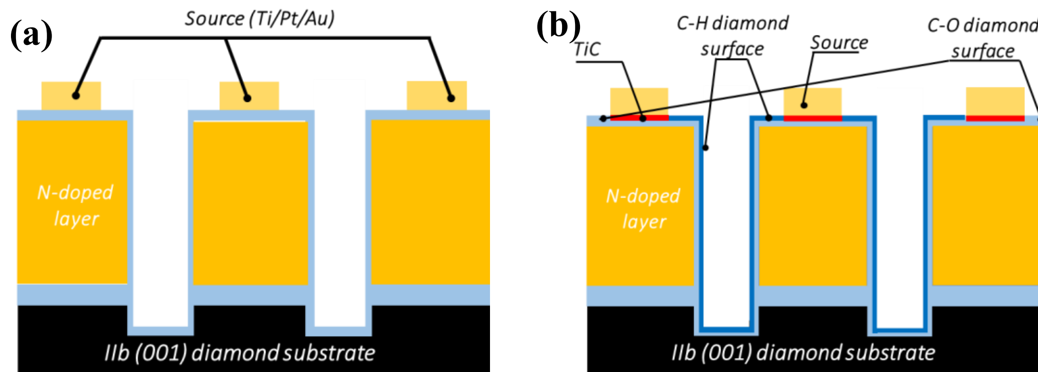


Fig. 2.13 (a) Source electrode (Au/Pt/Ti = 20/30/200 nm) with multifinger structure was formed. (b) TiC was formed during annealing with H_2 at 500 °C, hydrogen-termination diamond was formed on sidewall of trench via MPCVD using hydrogen plasma, and C–O diamond surface for isolating each MOSFET was formed via oxygen plasma treatment.

After the multifinger-like source electrode surrounding the trench side was deposited, TiC and hydrogen termination were formed (Fig. 2.13 (a)) via the high temperature in the hydrogen atmosphere and hydrogen plasma, respectively. The C–O diamond surface for isolation was formed via oxygen plasma treatment (shown in Fig. 2.13 (b)).

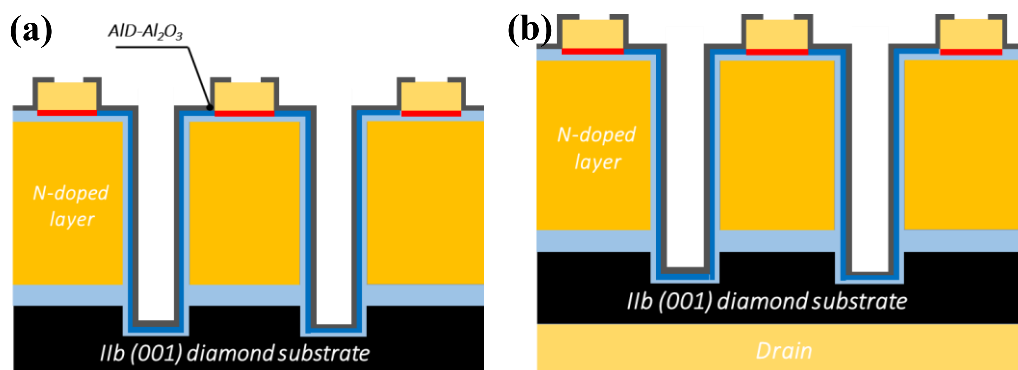


Fig. 2.14 (a) 200 nm ALD–Al_2O_3 passivation layer for gate insulator deposited at 450 °C. (b) Drain electrode (Ti/Au= 10/250 nm) at backside of IIb diamond substrate formed via DIBS.

The 200 nm Al_2O_3 passivation layer for the gate insulator was deposited using ALD equipment at 450 °C, and 10/250 nm of Ti/Au layer was formed for the drain electrode at the back side of the diamond substrate. Finally, after Al_2O_3 was etched by using NMD-3 for the contact area (Figs. 2.14 (a) (b)), a 100 nm Al layer for the overlapping gate was deposited using a thermal evaporation system. The overlapping gate was covered by the insulating film of the source electrode, and the overlapping area was 1 μm^2 (L_{OV} = 1 μm). This structure can reduce the distance between the gate and source (L_{SD}) to approximately 0 as well as reduce the gate–source resistance (R_{GS}). A longer gate length enables the gate electrode to regulate the MOSFET's drain current more effectively.

The MOSFET's partial top view and section view are shown in Figs. 2.15 (a) and (b), respectively. An optical microscope photograph of the vertical-type C–H diamond MOSFET with W_G exceeding 2 mm is shown in Fig. 2.15 (c). Based on the parallel structure of the gates, the multifinger-like vertical-type MOSFET is equivalent to connecting multiple devices with a single trench in series through the source electrode to broaden the gate width and increase the total output current. W_G is calculated as follows:

$$W_G = 2W_T + L_T$$

W_T is the width of the trench; in this fabrication, each W_T is 60 μm, and L_T is the length of the trench, which is 5 μm.

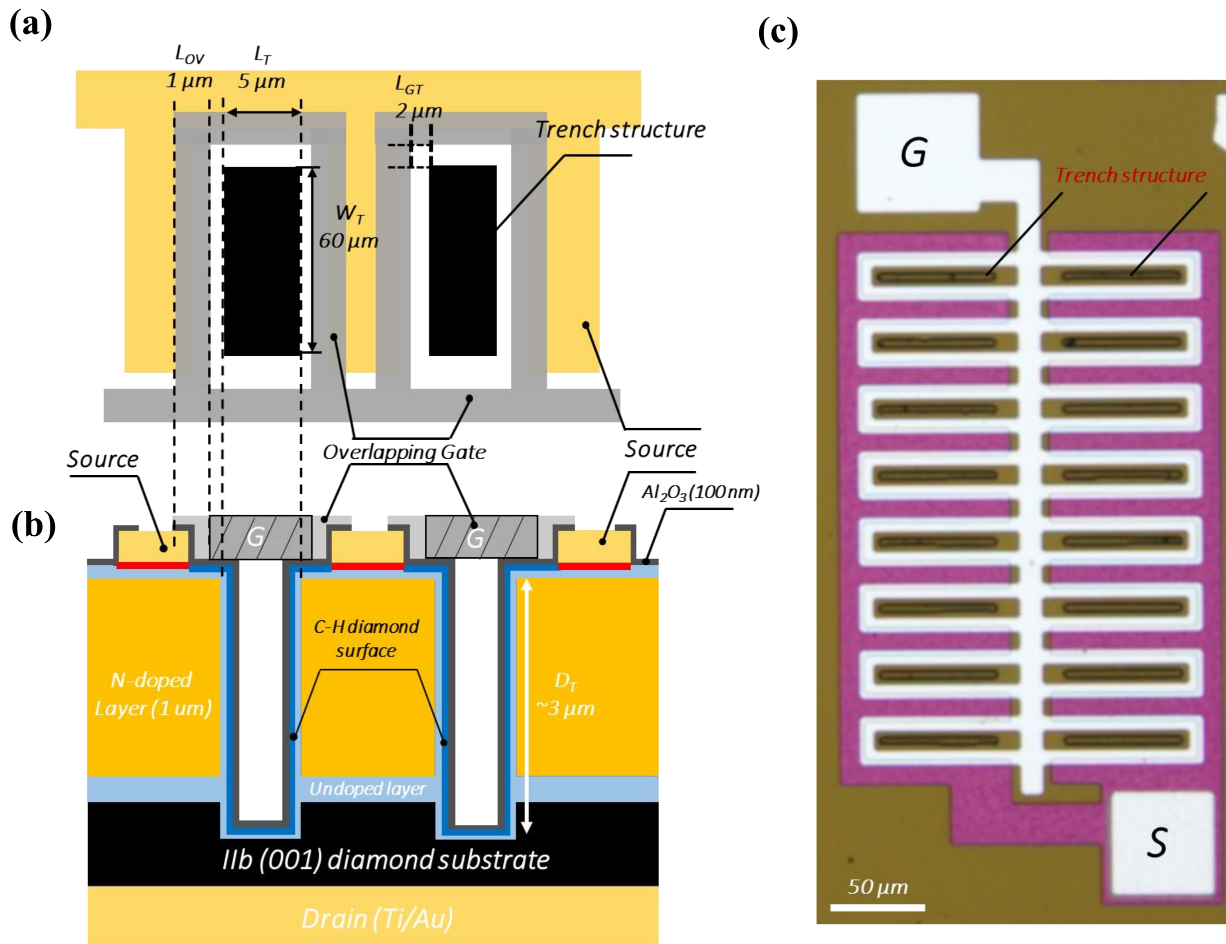


Fig. 2.15 (a) Partial top view of vertical-type C–H diamond MOSFET. (b) Partial section view of vertical-type C–H diamond MOSFET. (c) Optical microscopy photograph of devices fabricated in this experiment, with W_G = 2 mm (16 trenches).

2.3.2 Electric characteristic of vertical-type C–H diamond MOSFETs

In this section, several vertical-type C–H diamond MOSFETs were fabricated with gate widths ranging from 0.125 to 10 mm, to observe drain currents exceeding those of lateral-type C–H diamond MOSFETs. This section discusses the electrical characteristics of devices with gate widths exceeding 1 mm. The MOSFETs with the highest current value in the same W_G devices are listed below.

The electric characteristics were tested using B1500a, Keysight. Because the vertical-type C–H diamond MOSFETs produced this time will have a large current, to eliminate the effect of probe heating and device heating in the test, the pulse measurement method with a period of 10 ms, width of 2 ms, and duty ratio of 0.2 was adopted for the electrical characteristics test.

The I_{DS}–V_{DS} and I_{GS}–V_{GS} characteristic curves of the vertical-type diamond MOSFETs with W_G = 1 mm are shown in Figs. 2.16 (a) (b). At V_{GS} = -20 V and V_{DS} = -30 V, the maximum drain current value of this device was -90 mA, the maximum current density was -90 mm/mA, and the maximum transconductance g_m was 2.5 mS/mm at V_{DS} = -20 V. The maximum I_{DS} of the devices improved significantly by enlarging the gate width. However, in the linear region of the I_{DS}–V_{DS} characteristic curve, the I_{DS} curve of the device did not rise in a straight line, but a small g_m region appeared at the initial rising-up stage, when the vertical device is turned on, holes

carriers need to pass through the undoped diamond layer at the bottom of the trench to reach the p+ diamond to realize the channel conduction.

The on-resistance was considered as follows: only gold was used as the drain of the device, and the surface roughness of the diamond back side affected the adhesion of the metal electrode, resulting in a deteriorated ohmic contact. Meanwhile, the conductive channel (2DHG) of the diamond vertical-type device appeared on the undoped diamond surface of the trench sidewall, and a 500 nm regrowth diamond layer appeared at the bottom of the trench. This diamond layer was undoped and had a potential barrier of 0.38 eV between the boron-doped diamond substrates, resulting in resistance (Fig. 2.17). As shown from the I_{GS}–V_{GS} characteristic curve, the device indicated normal operation with V_{TH} = 23 V, and the on/off ratio was 10^8, and the Ron is 46mΩ/cm^2 at V_{DS}=-20 V.

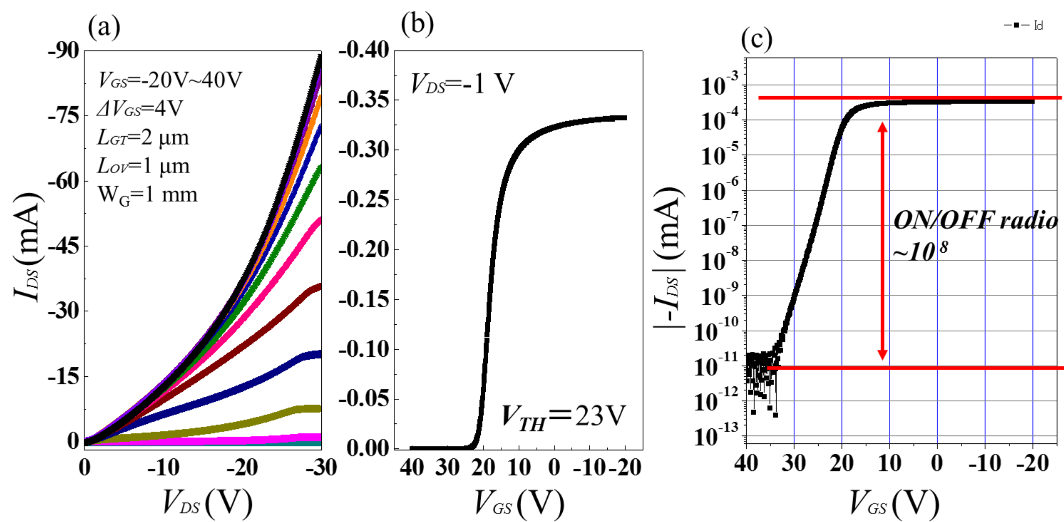


Fig. 2.16 (a) Characteristic curves of vertical-type C–H diamond MOSFETs with W_G = 1 mm; I_{DS}–V_{DS} characteristic curve showing (a) I_{DMAX} of -90 mA @ V_{GS} = -20 V and V_{DS} = -30 V; maximum g_m was 2.5 mS/mm at V_{DS} = 20 V. This device shows V_{TH} = -23 V in I_{GS}–V_{GS} characteristic curve (b), and (c) on/off ratio exceeding 10^8.

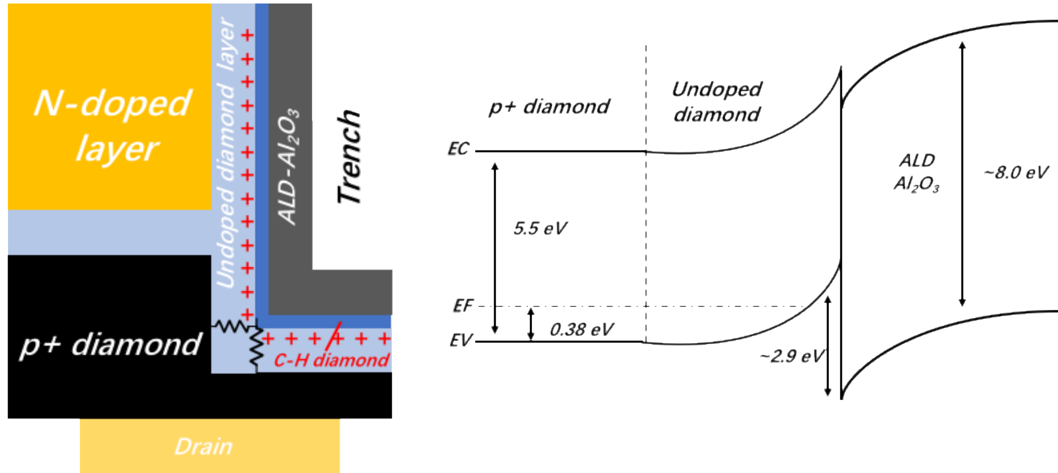


Fig. 2.17. Left side shows section view of trench region in vertical-type C–H diamond MOSFETs; 2DHG was induced on Al_2O_3/C–H diamond surface. When device is turned on, hole carries should pass though the undoped/p+ diamond interface to reach the drain. Energy band diagram of this model is shown at right side; 0.38 eV bandgap between undoped diamond and p+ diamond at room temperature is suggested.

The characteristics of the vertical-type diamond MOSFETs with W_G = 2 mm are shown in Figs. 2.18 (a) (b). At V_{GS} = -20 V and V_{DS} = -30 V, the maximum drain current of this device was -140 mA, the maximum current density was -70 mm/mA, and the maximum g_m was 2.1 mS/mm at V_{DS} = -20 V. and the Ron is 60 mΩ/cm^2 at V_{DS}=-20 V.

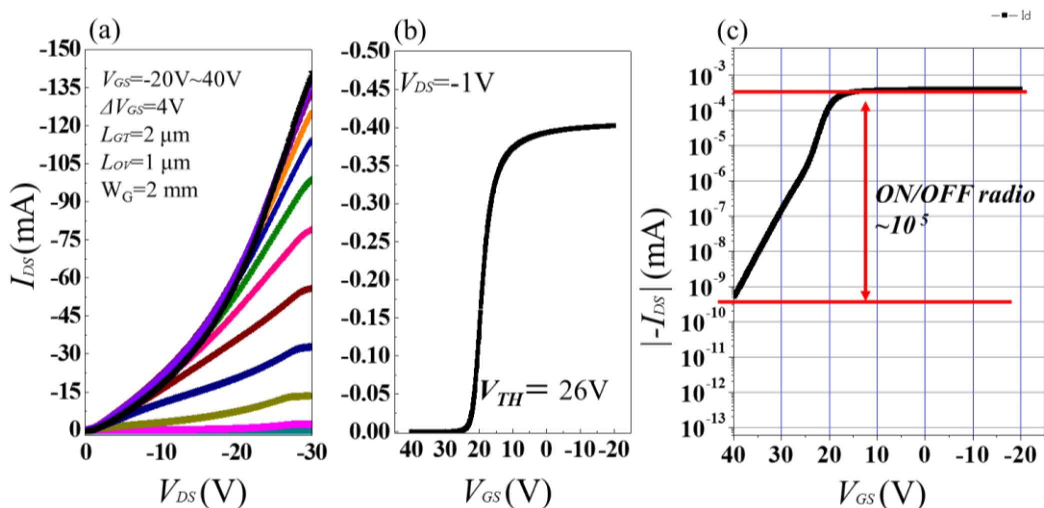


Fig. 2.18. (a) I_{DS}–V_{DS} and (b), (c) I_{DS}–V_{GS} characteristic curve of vertical-type C–H diamond MOSFETs with W_G =2 mm, and (c) on/off ratio exceeding 10^5.

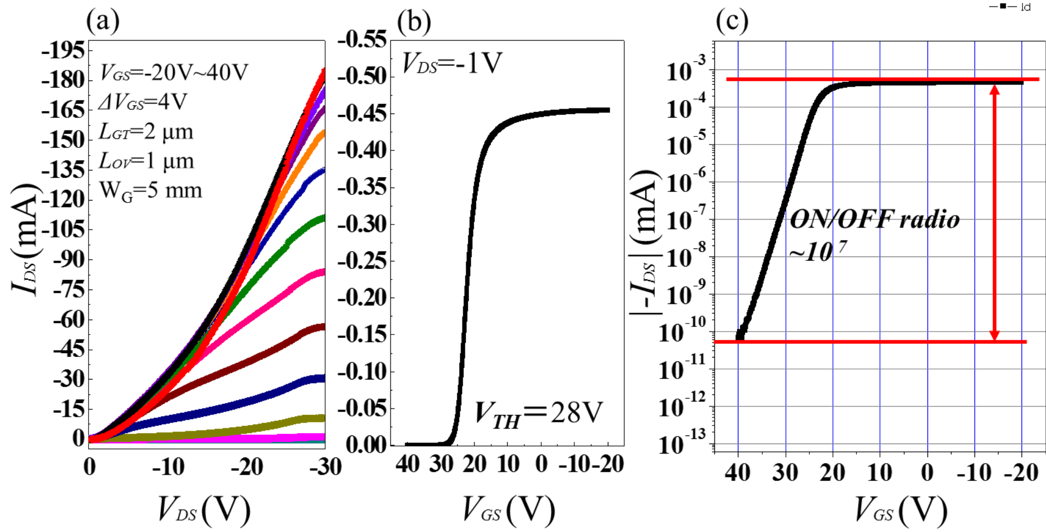


Fig. 2.19. (a) I_{DS}–V_{DS} and (b), (c) I_{DS}–V_{GS} characteristic curves of vertical-type C–H diamond MOSFETs with W_G =5 mm at room temperature, and (c) on/off ratio exceeding 10^7.

The characteristic curves of the vertical-type diamond MOSFETs with W_G = 5 mm are shown in Figs. 2.19 (a) (b). At V_{GS} = -20 V and V_{DS} = -30 V, the maximum drain current of this device was -185 mA, the maximum current density was -34 mm/mA, and the maximum transconductance g_m was 1.4 mS/mm at V_{DS} = -20 V. The device operates normally with V_{TH} = 23 V at room temperature, with an on/off ratio of 10^7. and the Ron is 91 mΩ/cm^2 at V_{DS}=-20 V.

The electrical characteristics of the device with the largest gate width in this device fabrication are shown in Fig. 2.20. This vertical-type diamond MOSFET possesses I_{DSMAX} = -179 mA, V_{GS} = -20 V, V_{DS} = -30 V, and the maximum current density of 16 mm/mA; furthermore, the device operates normally with V_{TH} = 25 V at room temperature, with an on/off ratio of 10^7. and the Ron is 170 mΩ/cm^2 at V_{DS}=-20 V.

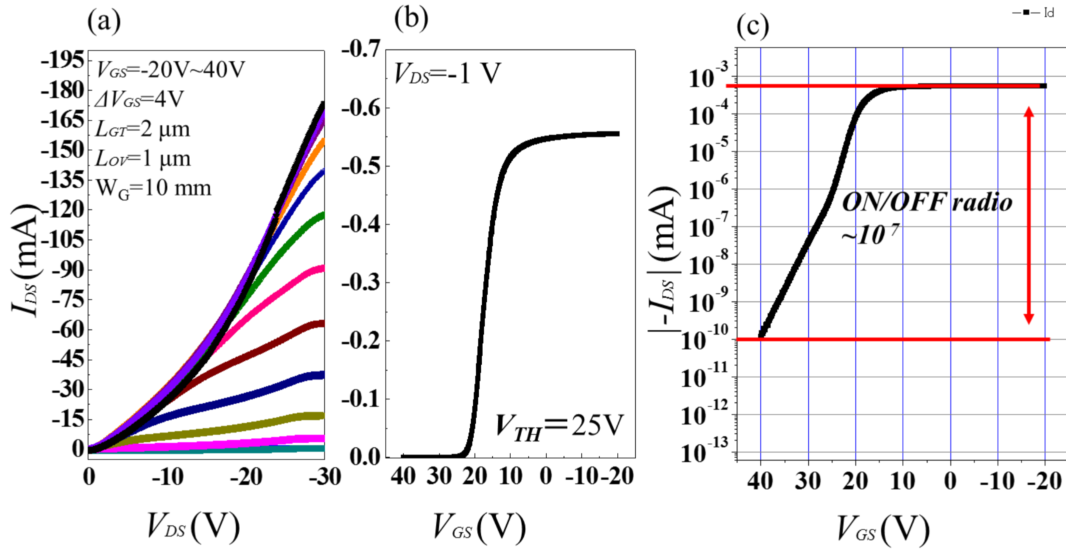


Fig. 2.20. (a) I_{DS}–V_{DS} and (b), (c) I_{DS}–V_{GS} characteristic curves of vertical-type C–H diamond MOSFETs with W_G =10 mm at room temperature. and (c) on/off ratio exceeding 10^7.

The Fig. 2.21 (a) shows the Ron of the vertical-type C–H diamond MOSFETs with different gate width, according to Ids-Vds characteristics, it can be calculated that the Ron of the vertical-type MOSFETs decreases with the increase of W_G. Compared with W_G=5mm MOSFET, the specific Ron of MOSFET with W_G=10mm does not decrease obviously, but compared with 1mm MOSFET, Ron decreases over 2 times. By normalizing the Ron with the active area of the device, it can be seen that Ron increases with the increase of W_G of the MOSFETs (Fig.2.21 (b)),this is considered that when turn-on the diamond vertical-type device with multi-trench structure, not all of the trench operate, which makes the resistance of the W_G=10mm device higher than that of the W_G=5mm device when calculating the specific Ron.

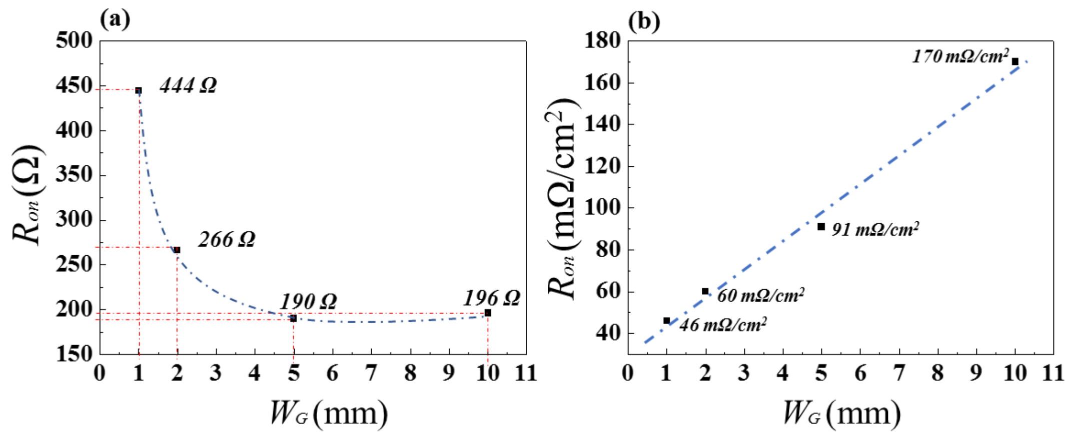
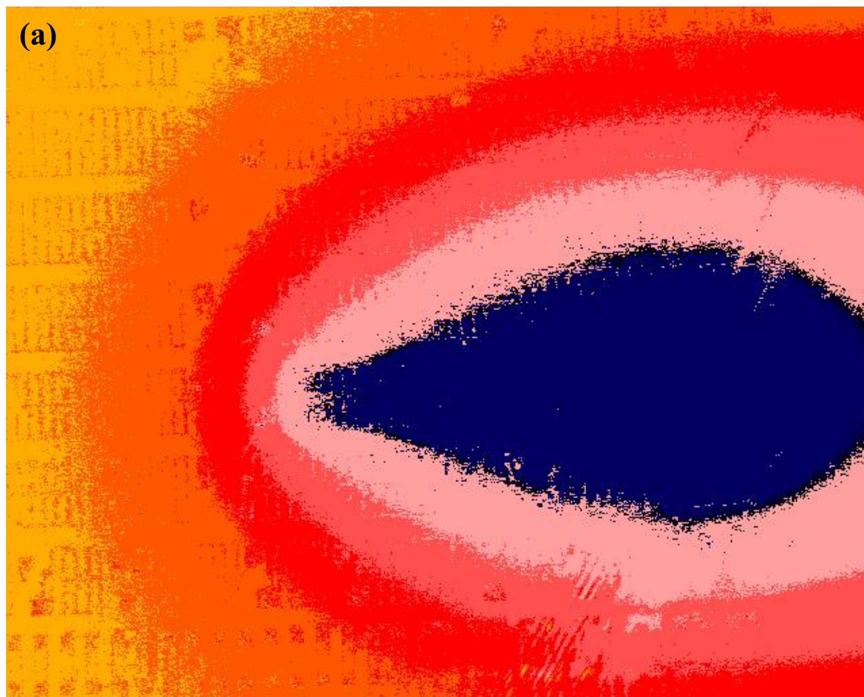


Fig. 2.21. (a) The Ron-W_G relation and (b) the specific Ron-W_G curve of the vertical-type C–H diamond MOSFETs with W_G =1 mm to W_G =10 mm in this section

The thermal distribution of the W_G = 10 mm vertical-type diamond MOSFET obtained using a lock-in thermography system (THEMOS-1000) is shown in Figs. 2.22 (a) (b).



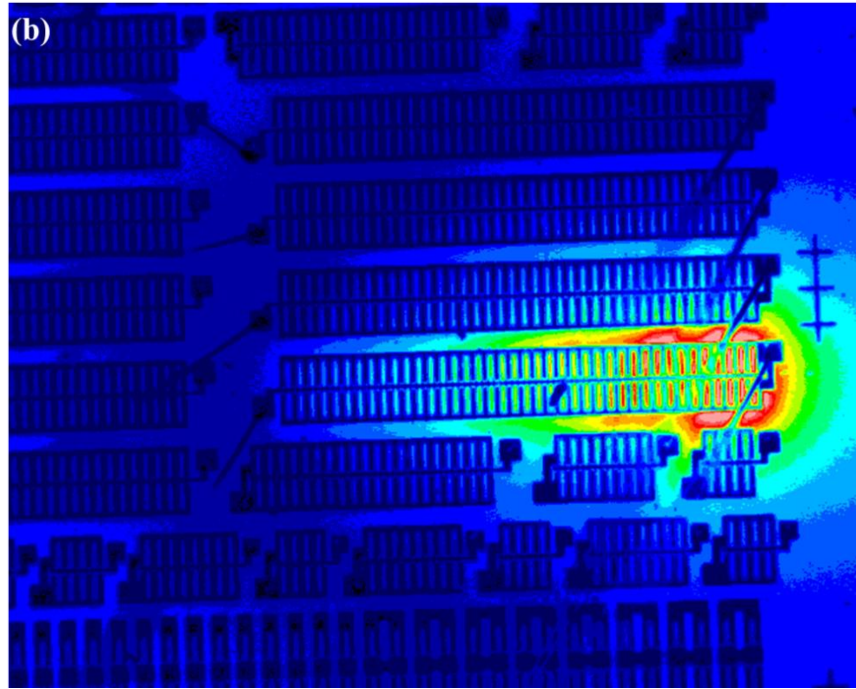


Fig. 2.22. (a) Surface temperature–time mapping of vertical-type C–H diamond MOSFETs in on state. Black part in the center shows area with the earliest temperature rise. (b) Surface temperature distribution mapping of vertical-type C–H diamond MOSFETs in on state. Red part shows area with the highest temperature.

The thermal distribution results indicated that when the device was turned on, the electrodes of the MOSFET near the source side heated up rapidly. However, when the device was in the on state, the temperature rise area appeared only in a part of the device, which suggested that a part of the gate is not activated, and that most of the channel was not conducting when bias was supplied. This may have caused the maximum current did not increase significantly when W_G was enlarged to 10 mm.

2.4 Conclusion

For power conversion applications, enhancing the output power is key for fabricating high-frequency power switches and inverters. In this chapter, the feasibility of increasing the output current by enlarging the gate width of diamond devices is demonstrated. Lateral-type C–H diamond MOSFETs with W_G=25–500 μm and vertical-type C–H diamond MOSFETs with W_G = 0.125 to 10 mm were fabricated. Consequently, the maximum output current of the diamond MOSFET was enhanced by enlarging the gate width. The lateral-type C–H diamond MOSFETs indicated a maximum I_{DS} = -50 mA with W_G = 500 μm, and the vertical-type C–H diamond MOSFETs indicated a maximum I_{DS} = -185 mA with W_G = 5 mm. However, with the increase in the gate width, the maximum current of the large-sized MOSFET did not increase. In lateral-type devices, this is considered to be associated with the bottom contact resistance between regrown undoped layer and highly boron doped substrate and the device and the Ohmic contact of the device.

As of the vertical-type diamond MOSFETs, the maximum drain current of this device was -185 mA of a device with W_G= 5 m, and the I_{DSMAX} of the device with W_G = 10 mm was at the same level as that of the device with W_G = 5 mm due to the source or gate electrode did not active all the trench, This problem can be solved by use thicker Au as the source metal or reduce the length of the device to make sure the all the trench operate when the bias voltage turn on the MOSFET.

However, in the experiment, all the diamond MOSFETs were successfully fabricated, but all the C-H diamond MOSFET shows the normally-on operation, These MOSFETs will be applied in cascode circuits and inverters. The application of the diamond MOSFET circuit will be discussed in the next chapter.

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Chapter 3

Normally-off 2DHG Diamond MOSFETs Cascode Circuit Application and Diamond Half-Bridge Complementary Inverter

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3.1 Normally off 2DHG Diamond MOSFET Cascode Application

Diamond is an ideal semiconductor material that can be applied in next-generation high-frequency and high-voltage power devices. Although it is difficult to dope n-type diamond, n-channel diamond power devices offer certain advantages and hence need to be developed. Owing to the excellent p-type semiconductor physical properties of C-H diamond surfaces [1], p-channel diamond power devices have been widely investigated [2][3][4][5]. However, p-channel devices using other wide-bandgap semiconductor materials, such as 4H-SiC and GaN, are limited by the disadvantages of p-type material properties, such as low mobility and high interface state density [6][7][8][9][10]. Hence, it is difficult to apply them in high switching speed and high output power semiconductor circuits or power conversion systems. However, diamond p-channel devices exhibit excellent mobility (exceeding 100 $cm^2V^{-1}s^{-1}$) and low interface state density (~10^{12} eV^{-1} cm^{-2}); hence, they can replace high-performance wide-bandgap p-type semiconductor power devices for applications in electronic circuits and power conversion systems, such as inverters and converters.

However, because of the 2DHG induced on the C–H diamond surface as well as the negative fixed charge in the ALD Al_2O_3 insulating film aggravating the spontaneous polarization effect of the C–H dipole, diamond MOSFETs show depletion mode operation even without a negative bias on the gate electrode. This characteristic has been discussed in Chapter II; the 2DHG inducing exhibits crystallographic orientations independent of the diamond surface, whereas the lateral-type C–H diamond MOSFETs

and vertical-type diamond MOSFETs operate normally. To apply diamond devices to electric power conversion systems, a normally off operation is required. By modifying the diamond surface in the channel region or adjusting the charge in the insulating film, normally off diamond MOSFETs have been investigated [11][12][13][14][15]; however, the realization of normally off diamond devices via these methods is achieved at the expense of some electrical characteristics of the devices because the formation of 2DHG is associated with the coverage of hydrogen on the diamond surface and the negative charge content in the insulating film, and the current density of these normally off diamond MOSFETs is much lower than that of normally on C–H diamond MOSFETs.

The application of wide bandgap semiconductor power devices in the cascode configuration has been reported. In n-channel devices, GaN HEMTs have been applied in cascode structures and used as switching devices in power electronics [16][17][18], and its power applications [19] have been reported as well. However, the realization of a high breakdown voltage of 1000 V cascode combined with GaN lateral structure device is still difficult due to the restricted physical properties of GaN-based semiconductor materials.

In this study, the properties of high breakdown electric fields based on diamond, i.e., the diamond cascode by combining a low-breakdown-voltage normally off silicon p-MOSFET with high-breakdown-voltage normally-on C–H diamond MOSFETs, indicate that the gate of the diamond MOSFET is effectively controlled by the silicon

p-MOSFET, resulting in a normally off operation and breakdown in the diamond p-channel cascode. Further details will be provided in this section.

3.1.1 Circuit construction of diamond cascode

The schematic circuit diagram of the diamond p-channel cascode is shown in Fig. 3.1. The gate of the diamond MOSFET and the source of the Si MOSFET have the same electric potential as the common ground. In addition, the source of the diamond MOSFET is connected to the drain of the Si MOSFET; this implies that in the diamond cascode circuit, two devices share one gate of the Si MOSFET as the control port of the output current. Whereas the drain electrode of the diamond MOSFET is used as the output port of the entire cascode structure, the gate of the diamond device is connected to the source of the Si MOSFET as the source electrode of the diamond cascode.

In the diamond cascode, the source–drain voltage of the silicon MOSFET (V_{DS}, Si) is equivalent to the gate–source voltage of the diamond MOSFET (V_{GS}, Dia), which can be expressed as follows:

$$V_{GS,Dia} = V_{DS,Si} \quad \dots\dots\dots (1)$$

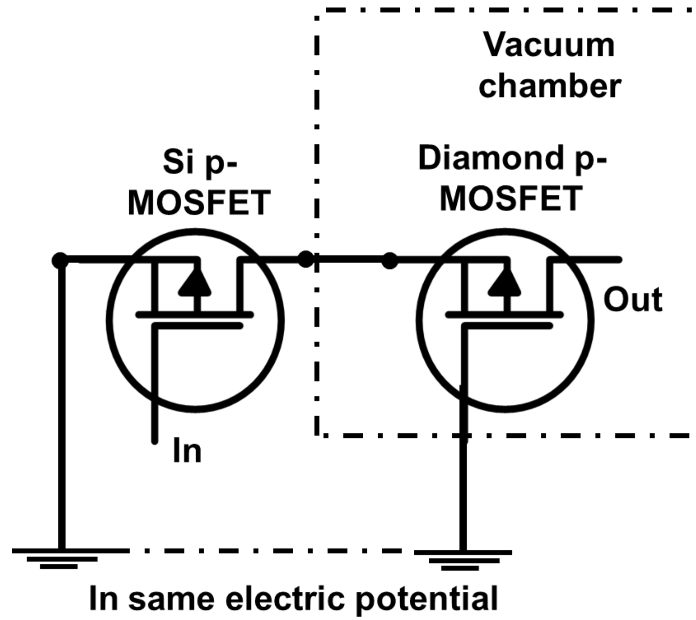

Fig. 3.1 Schematic circuit diagram of diamond p-channel cascode; normally on diamond MOSFET combined with normally off Si MOSFET; gate of Si MOSFET as input to control threshold voltage of entire structure; drain of diamond

When the silicon MOSFET was turned on, $V_{DS,\ Si}$ decreased to a low potential (approximately 0 V), and $V_{DS,\ Si}$ became lower than the threshold voltage ($V_{TH,Dia}$) of the diamond MOSFET. The cascode changed to the ON state (shown in Fig. 3.2(a)) because the diamond MOSFET was in the ON state at $V_{GS} = 0$ V (normally on). The equation for the ON state of the diamond cascode can be expressed as follows:

$$(V_{GS,Dia} = V_{DS,Si} = 0\ \mathrm{V}) \leq V_{TH,Dia} \cdots\cdots\ (2)$$

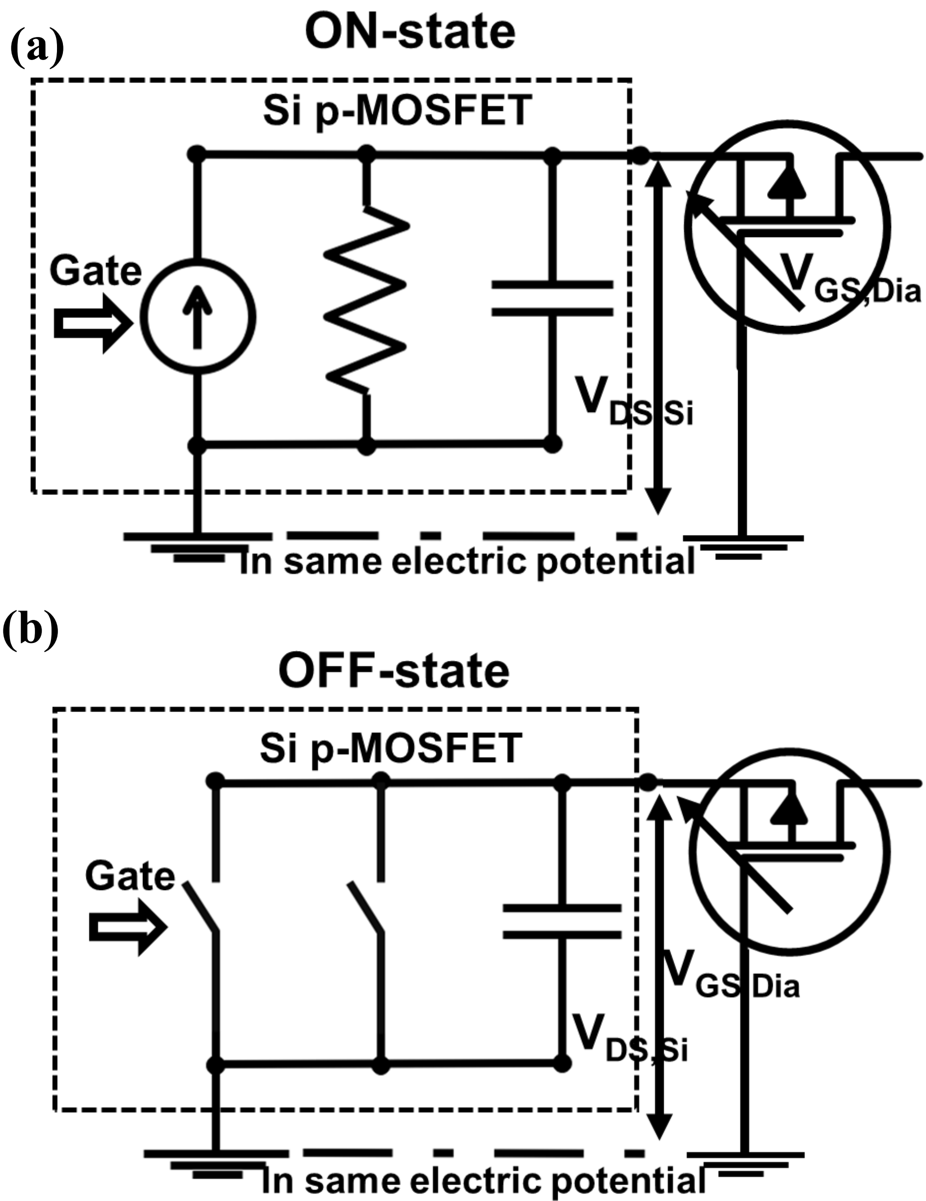

Fig. 3.2 Equivalent circuit of diamond cascode in (a) ON state when Si MOSFET was turned on; internal circuit is equivalent to a resistor and capacitor connected in parallel. (b) Diamond cascode in OFF state when Si MOSFET was turned off; internal circuit is equivalent to parasitic capacitance connected in series with source electrode of diamond MOSFET.

When the diamond cascode in the ON state, the internal circuit is equivalent to the parallel connection of the current source, resistance, and capacitance in the Si MOSFET. The resistance is primarily from contact resistance and channel resistance, and the

capacity depends on the length of the gate electrode and the thickness of the insulating film.

The equivalent circuit of the diamond cascode in the OFF state is shown in Fig. 3.2 (b). When the Si MOSFET is turned off, $V_{DS,Si}$ increases because the voltage is blocked between the source and drain of the Si MOSFET, and only the capacitance is charging, which increases the voltage potential in the source of the diamond MOSFET. When $V_{DS,Si}$ exceeds the threshold voltage of the diamond FET, the cascode changes to the OFF state. The equation for the OFF state is as follows:

$$(V_{DS,Si} = V_{GS,Dia}) \geq V_{TH,Dia} \cdots\cdots\cdots (3)$$

Because of the small size of the diamond MOSFET, the diamond substrate was set in a vacuum chamber with an external circuit and the wiring of the high-voltage device measuring system (B1500A, Agilent) when the cascode circuit was assembled. In fact, using packaging technology to wire diamond MOSFETs finely can significantly simplify the circuit design and reduce the parasitic resistance existing in the wires. However, in packaging, the possible fusing of internal wiring must be considered when the device is operating in a high-voltage environment. Because the diamond cascode will be applied to the inverter circuit for the high-voltage switching test, external wiring was adopted in the experiment to assemble the cascode circuit. The low-voltage Si MOSFET (< 100 V) (2sj380, TOSHIBA) was connected to B1500A by the terminal

box. The main structure and wiring are shown in Fig. 3.3.

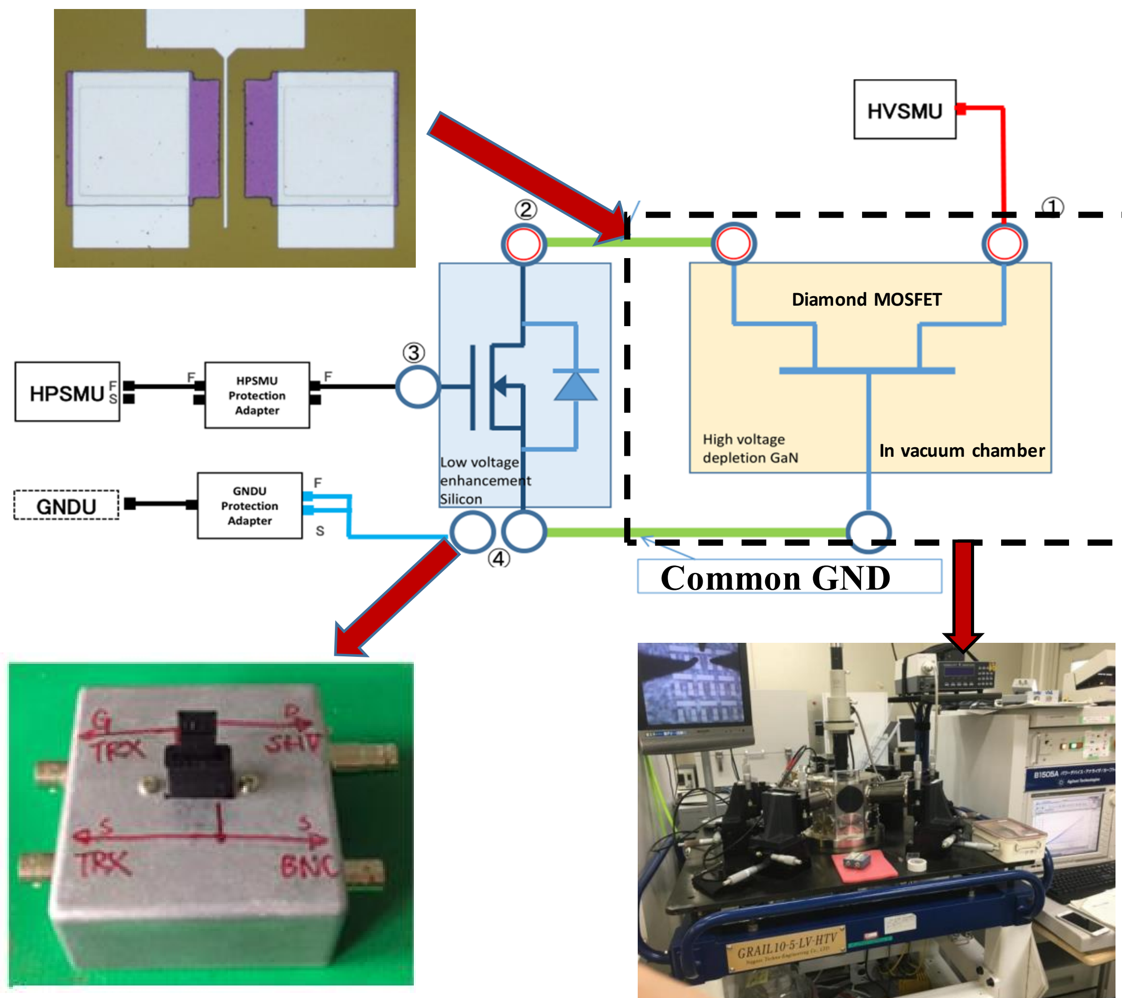

Fig. 3.3 Experimental circuit assembly of diamond cascode in high-voltage device measuring system; diamond MOSFET set in vacuum chamber; Si MOSFET product connected with diamond device via terminal box.

3.1.2 The electrical characteristics of diamond cascode

In Chapter II, the fabrication process and characteristic analysis of high-current diamond MOSFETs are presented. In this section, the characteristics of the most

representative devices after applying the diamond cascode are analyzed.

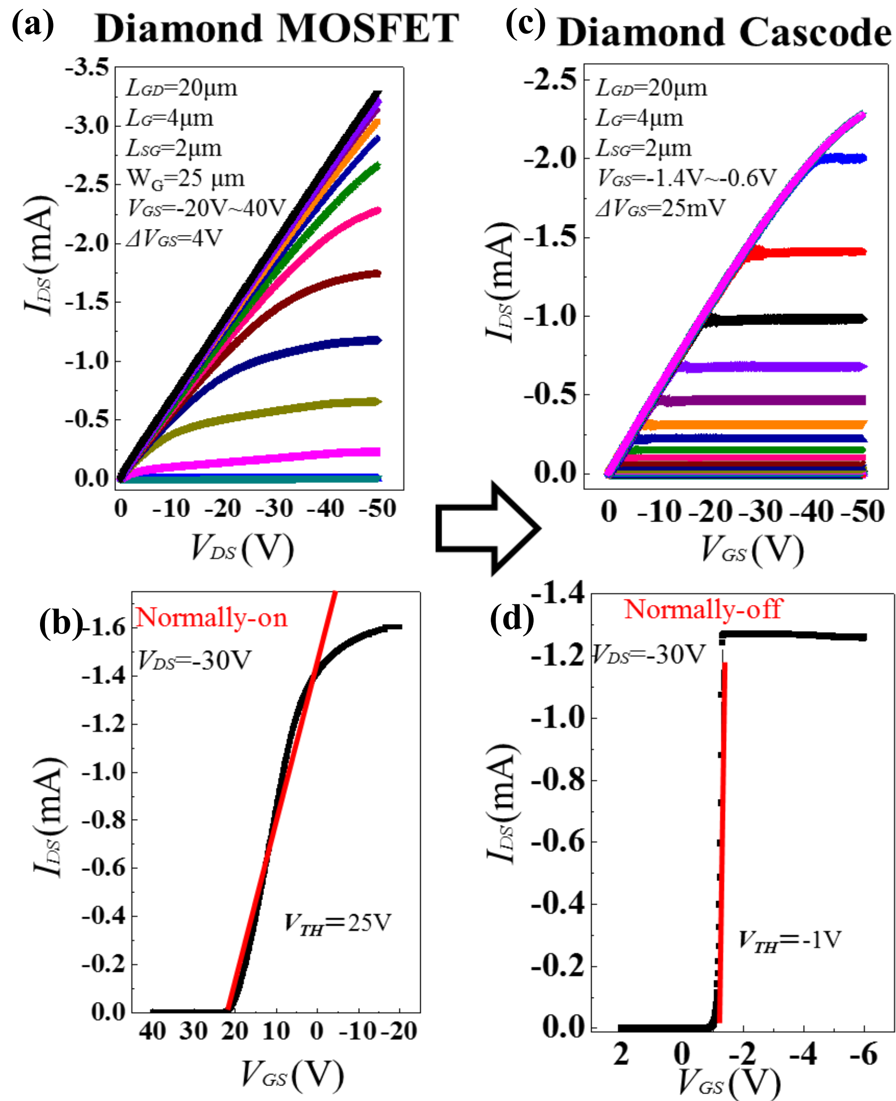

Fig. 3.4 (a) I_{DS}–V_{DS} characteristic curves; (b) I_{GS}–V_{GS} characteristic curves of lateral-type C–H diamond MOSFETs with W_G = 25 μm; (c) I_{DS}–V_{DS} and (d) I_{GS}–V_{GS} characteristic curves of device after it was applied to diamond cascode.

The V_{GS}–I_{DS} and V_{DS}–I_{DS} characteristics of the lateral-type C–H diamond MOSFET with W_G = 25 μm after it was applied to the diamond cascode are shown in Fig. 3.4. The normally off cascode Si MOSFET shifted V_{TH} to -1 V at V_{DS} = -30 V. As shown

from the characteristic curves, the threshold voltage was well controlled at -1 V through the regulation of the Si MOSFET, owing to the threshold voltage of the Si device product. The g_m (~640 mS/mm at V_{DS} = -20 V), which can be calculated from the V_{DS}–I_{DS} characteristic curve of the diamond cascode, increased significantly owing to the gate control ability of the Si device.

The characteristic curve of the largest W_G (500 µm) lateral-type C–H diamond MOSFET fabricated in this experiment and its cascode operation are shown in Fig. 3.5. By regulating the Si MOSFET, the threshold voltage shifted to -1 V at V_{DS} = -10 V, demonstrating a normally off operation. The maximum drain current was -31.8 mA at V_{DS} = -50 V when V_{GS} = -1.4 V. As the gate bias of the cascode structure increases, the output current of the cascode will eventually reach the same level as the maximum current value of the diamond MOSFET. The results show that with the increase in W_G of the diamond MOSFET, the output current of the cascode increases, but V_{TH} is still maintained at the threshold voltage of the Si device. Hence, it can be concluded that in the diamond cascode, the threshold voltage is determined by the Si MOSFET, whereas the output current is determined by the diamond MOSFET.

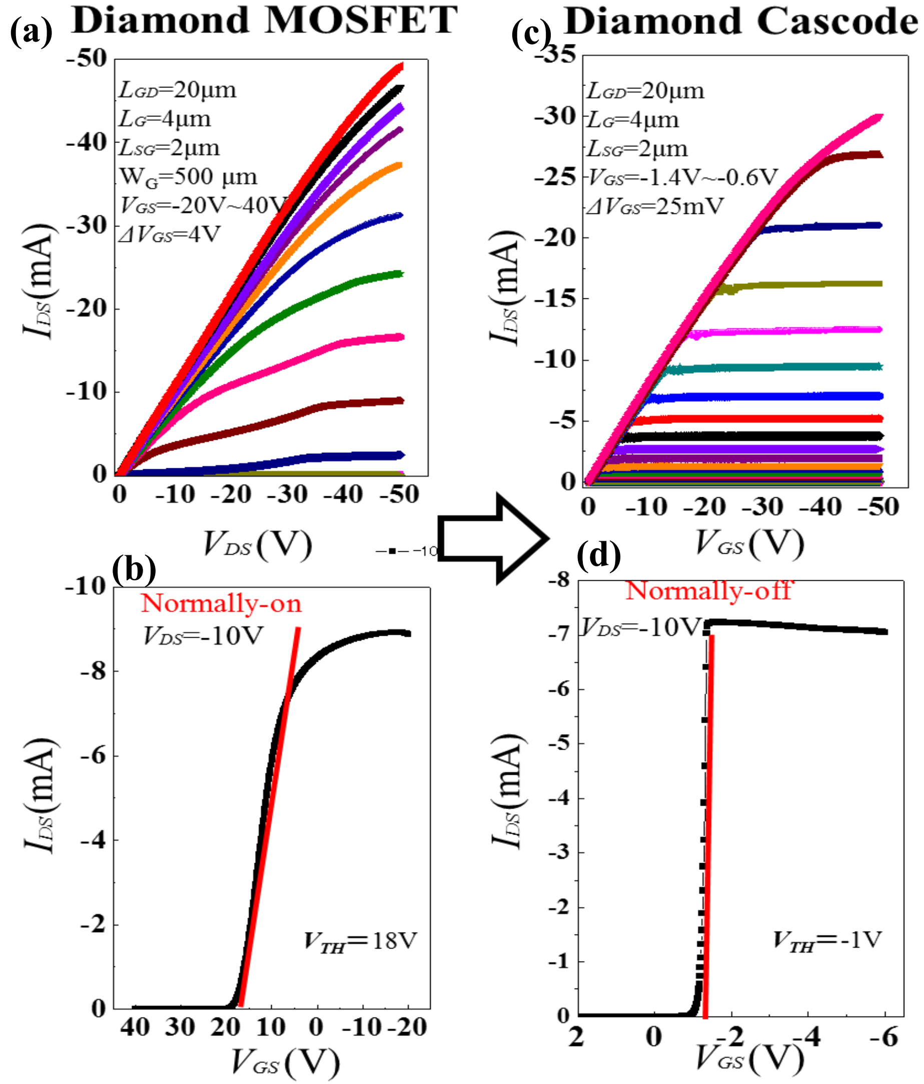

Fig. 3.5 (a) I_{DS}–V_{DS} characteristic curve; (b) I_{GS}–V_{GS} characteristic curve of lateral-type C–H diamond MOSFET with W_G = 500 μm; (c) I_{DS}–V_{DS} and (d) I_{GS}–V_{GS} characteristic curves of device after it was applied to diamond cascode.

If the current characteristics of the diamond MOSFET and diamond cascode are placed in the same ordinate system, then the difference in output current between the diamond MOSFET and diamond cascode can be compared. Figs. 3.6 (a) (b) show the I_{GS}–V_{GS} characteristics of the diamond MOSFET and its cascode structure, respectively. In the saturated region under V_{DS} = -10 V, a difference of 0.8 mA in the current value is observed between the diamond MOSFET and diamond cascode. The current loss is

primarily attributed to the resistance caused by the wire in the circuit and the terminal box of the Si MOSFET (resistance is around 3 Ω). However, the diamond cascode is still superior over the traditional normally off method in diamond device technology; consequently, the cascode exhibits a faster saturation speed and less current loss.

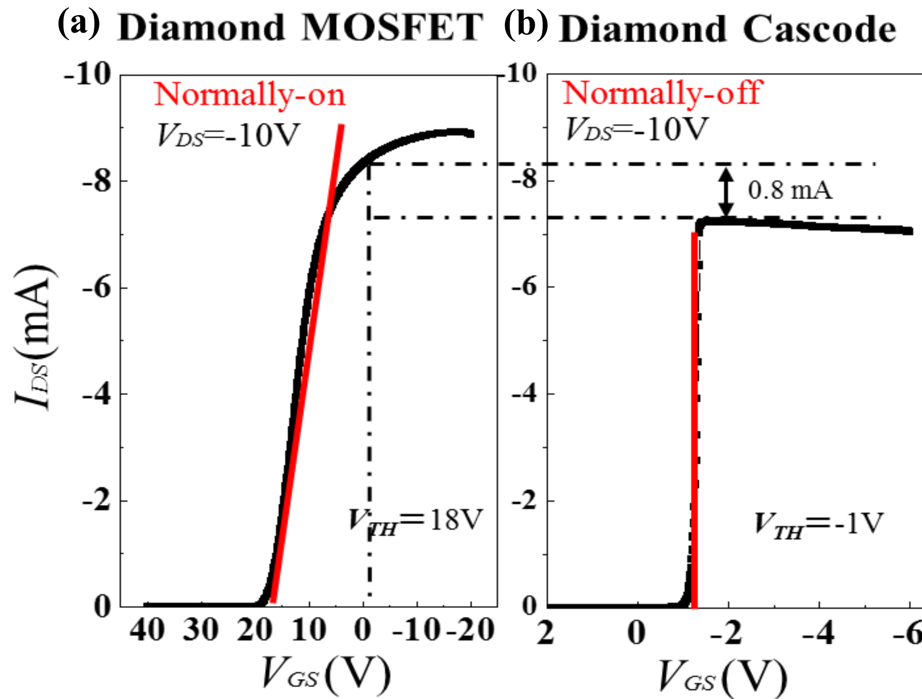

Fig. 3.6 I_{DS}–V_{GS} characteristics of (a) diamond MOSFET and (b) diamond cascode with W_G = 500 μm; comparing I_{DS} at the same V_{GS} (-1.5 V) and V_{DS} (-10 V), 0.8 mA current loss was observed in diamond cascode, attributable to resistance and parasitic capacitance in experimental circuit.

The cascode operation was also confirmed by applying the vertical-type C–H diamond MOSFETs. The V_{GS}–I_{DS} and V_{DS}–I_{DS} characteristic curves of the diamond MOSFET with W_G = 1 mm and diamond cascode are shown in Fig. 3.7.

In the vertical-type diamond cascode, the normally off Si MOSFET in cascode

shifted V_{TH} to -1 V at V_{DS} = -1 V effectively, thereby preventing excessive current from the Si MOSFET. The vertical-type diamond cascode was tested at a lower source–drain bias, and the maximum drain current was -11.5 mA at V_{DS} = -10 V when V_{GS} = -1.4 V; furthermore, the transconductance amplified to 120 mS/mm at V_{DS} = -10 V by the cascode, i.e., approximately 50 times that of this vertical-type diamond MOSFET.

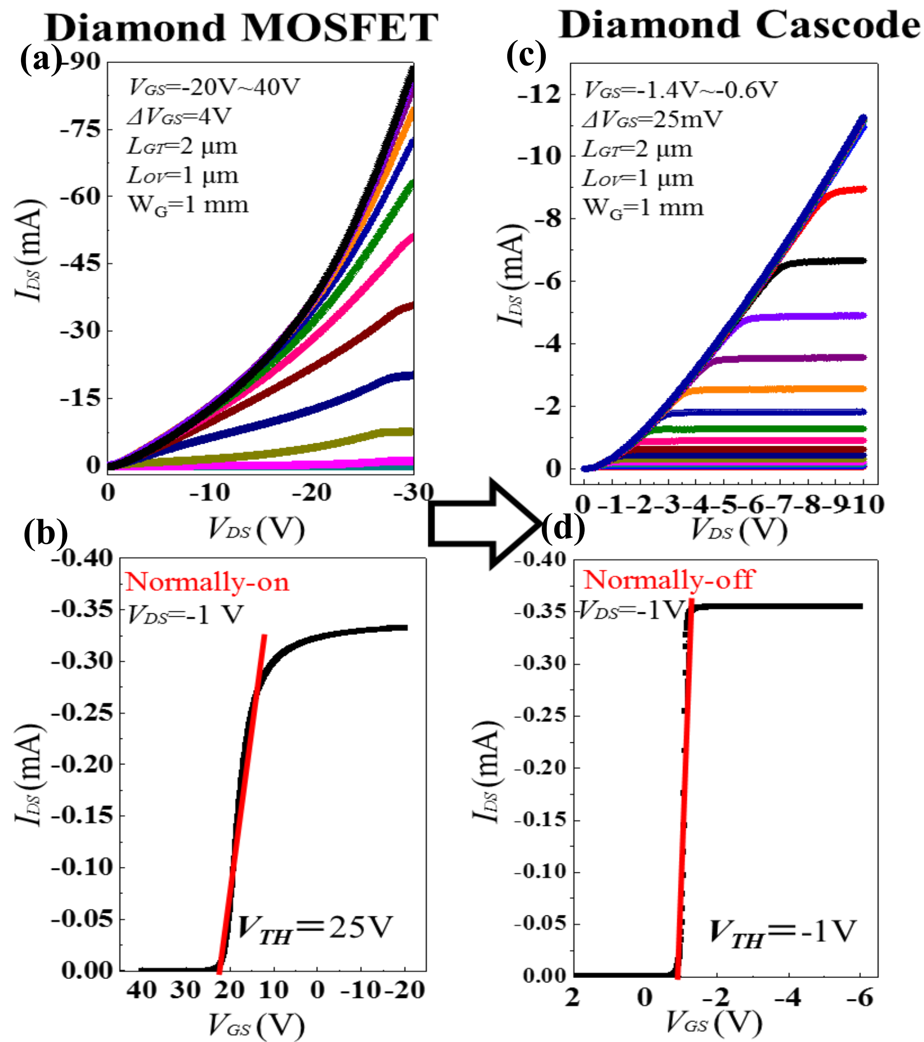

Fig. 3.7 (a) I_{DS}–V_{DS} characteristic curve; (b) I_{GS}–V_{GS} characteristic curve of vertical-type C–H diamond MOSFET with W_G = 1 mm; (c) I_{DS}–V_{DS} and (d) I_{GS}–V_{GS} characteristic curves of device after it was applied to diamond cascode.

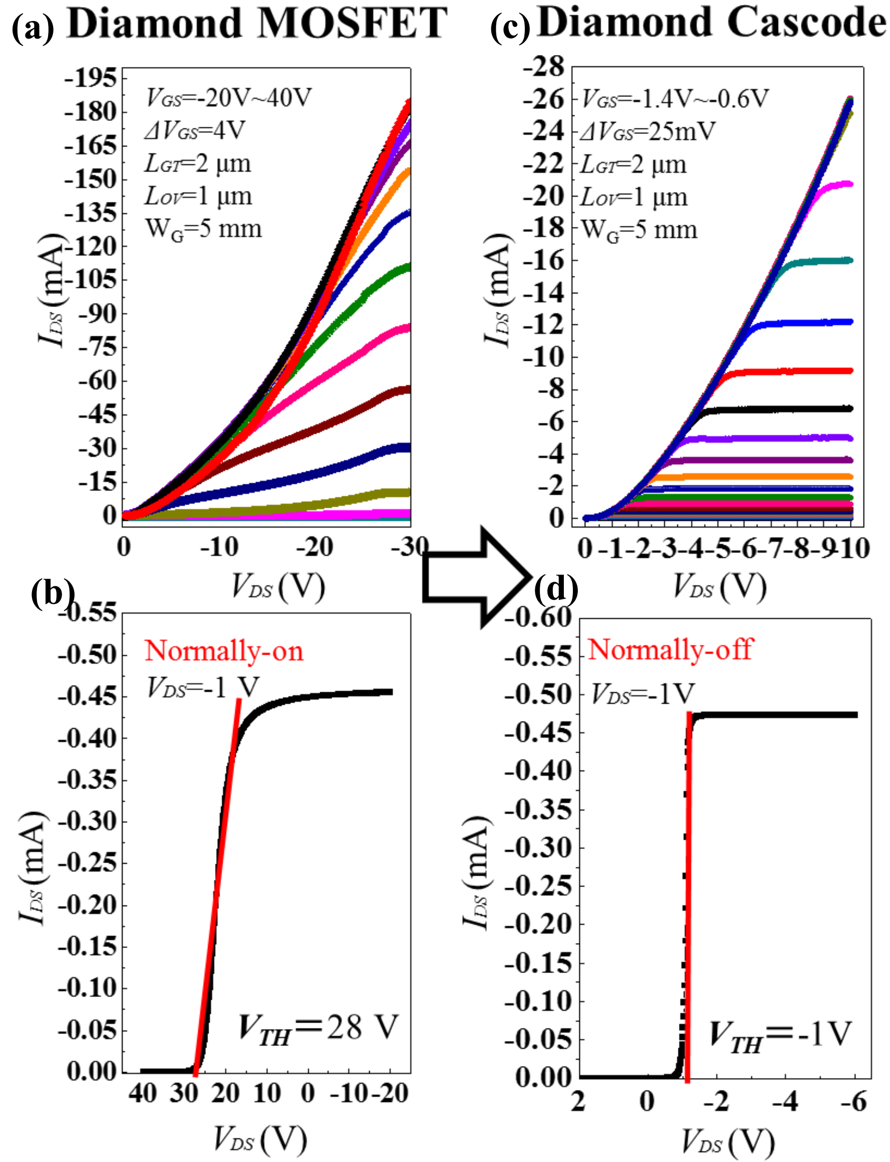

Fig. 3.8 (a) I_{DS}–V_{DS} characteristic curve; (b) I_{GS}–V_{GS} characteristic curve of vertical-type C–H diamond MOSFET with W_G = 5 mm; (c) I_{DS}–V_{DS} and (d) I_{GS}–V_{GS} characteristic curves of device after it was applied to diamond cascode.

The vertical-type C–H diamond MOSFET with W_G = 5 mm and its cascode characteristics are shown in Fig. 3.8. In this study, the largest drain current was obtained in this device. In the I_{DS}–V_{DS} characteristic curve of the cascode, the maximum drain current was -27 mA at V_{DS} = -10 V when V_{GS} = -1.4 V. The Si MOSFET shifted V_{TH} to -1 V at V_{DS} = -1 V, and the cascode exhibited a normally off operation. The

transconductance increased to 32 mS/mm, which was more than 50 times that of the vertical-type diamond MOSFET at V_{DS} = -10 V.

3.1.3 The Breakdown characteristics of diamond cascode

C–H diamond MOSFETs exhibit ultrahigh breakdown characteristics owing to the physical properties of diamond and the passivation layer of the ALD–Al_2O_3 for lateral power devices. For a 200 nm Al_2O_3 passivation layer, the breakdown voltage is associated with the L_{GD} of the MOSFET, and the V_B/L_{GD} preserves 1 MV/cm for a L_{GD} ranging from 5 to 10 μm [20].

The high breakdown voltage can be realized on the diamond cascode because the breakdown characteristic is governed by the diamond MOSFET in the cascode structure. In this experiment, the diamond cascode was measured via B1500a, which is different from measuring the diamond MOSFET individually. A diamond cascode blocking high voltages with V_{GS} = 0 V will be tested because of the normally off operation (a real normally off voltage blocking condition). Meanwhile, a diamond MOSFET should supply a positive voltage to the gate electrode to maintain the OFF state even under high voltages.

To demonstrate the relationship between the L_{GD} of the diamond MOSFET and the breakdown voltage of the diamond cascode, a diamond MOSFET with the same W_G but different L_{GD} was used in the cascode circuit in this experiment.

The breakdown voltage of the diamond cascode with a diamond MOSFET L_{GD} = 5 μm is shown in Fig. 3.9. The cascode achieved V_B = -415 V at V_{GS} = 0 V. It is noteworthy that the V_B of the Si MOSFET combined in the cascode circuit is merely -100 V, which exceeds the breakdown voltage, and the diamond MOSFET blocked the high voltage in the cascode.

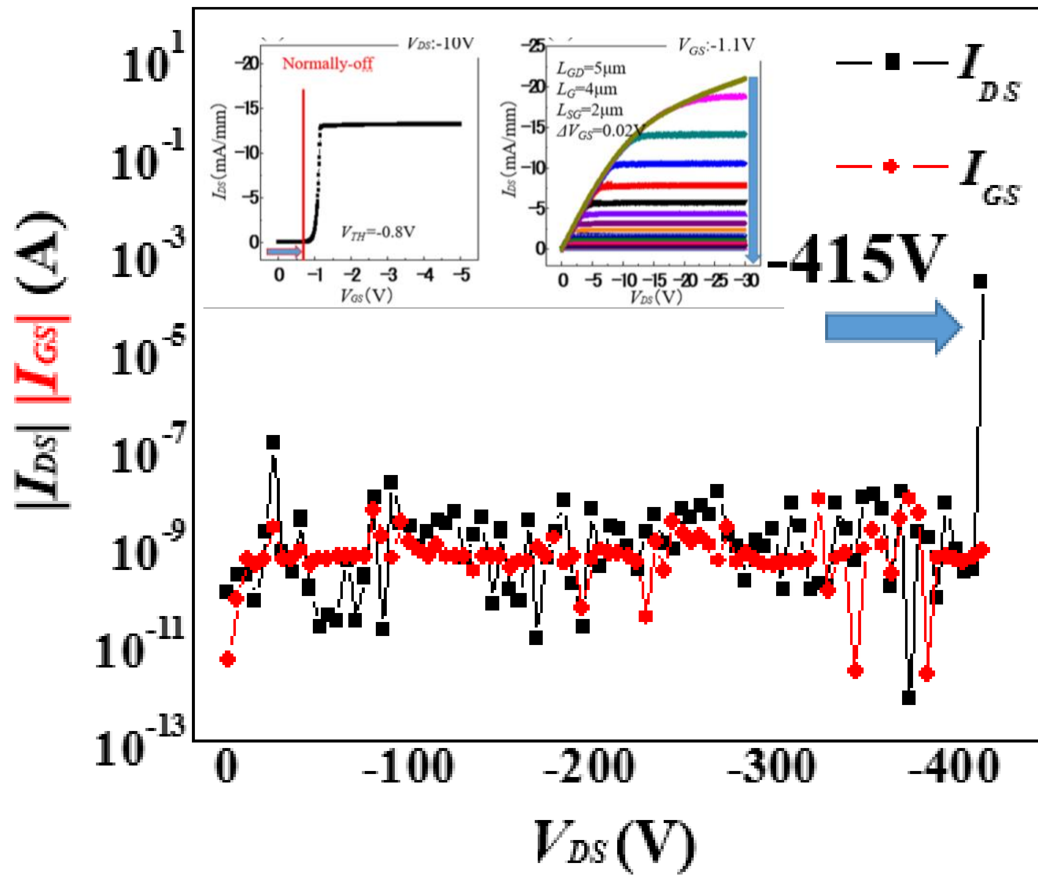

Fig. 3.9 Breakdown characteristic curve of diamond cascode with diamond MOSFET L_{GD} =5 μm; I_{DS}–V_{DS} and I_{GS}–V_{GS} characteristic curves shown as insets; breakdown voltage was -415 V at V_{GS} = 0 V for this cascode.

A high breakdown voltage was achieved when the diamond MOSFET was applied in the cascode configuration, with L_G = 2 μm, L_{SG} = 2 μm, and L_{GD} = 26 μm. The V_{DS}–I_{DS} and V_{GS}–I_{DS} characteristics are illustrated in Fig. 3.10. The breakdown voltage of

the diamond cascode reached -1735 V when the diamond cascode was turned off ($V_{GS,Si}$ = 0 V).

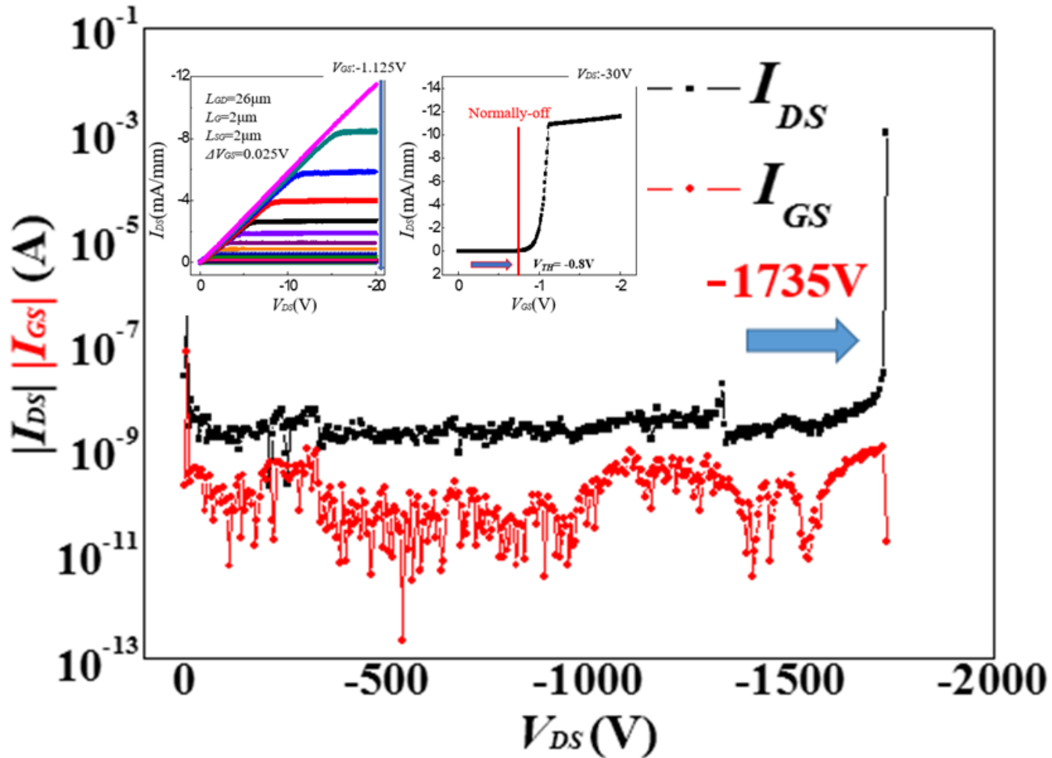

Fig. 3.10 Breakdown characteristic curve of diamond cascode with diamond MOSFET L_{GD} = 26 μm; I_{DS}–V_{DS} and I_{GS}–V_{GS} characteristic curves shown as insets; breakdown voltage was -1735 V at V_{GS} = 0 V for this cascode.

In addition, the I_{GS} remained at a low level even though a breakdown occurred; this is because in the experiment, I_{GS} is the current value of the Si p-MOSFET gate, and breakdown occurs be at the gate oxide side of the diamond FET. I_{DS} will increase rapidly, and when it reaches 10^{-3} A (preset I_{DS} limit value), the high-voltage device measuring system (B1500A, Agilent) will reduce the increase in V_{DS}. However, when breakdown occurred, the normally-off Si p-MOSFET in the OFF state did not break down, the Si p-MOSFET operated normally, the I_{GS} remained at a low value, and the Si p-MOSFET

operated normally, even after the breakdown experiment was verified. The breakdown experiments demonstrate that the breakdown voltage of the cascode depends entirely on the diamond MOSFET, and that it is easy to obtain high-breakdown normally off diamond power devices without sacrificing the current characteristics using the diamond cascode method.

3.2 Diamond Cascode Application for Diamond p-FET GaN n-FET Half-Bridge Complementary Inverter

The diamond power devices achieved a high reliability normally off operation and maintained the high breakdown characteristics via cascode technology, as discussed in the previous section. Furthermore, the diamond cascode enabled the application of diamond devices in high-voltage complementary inverter circuits. It is difficult to realize the application of high-operation voltage p-type wide-bandgap semiconductor power devices without modules in high-voltage switching circuits. In this section, experiments and discussions pertaining to the application of the diamond device as a p-type power device in high-voltage inverter circuits will be presented.

3.2.1 Circuit construction of diamond half-bridge complementary inverter

In the conventional CMOS inverter structure (NOT logic gate), the main structure of the circuit comprises two enhancement-mode transistors. The gate electrodes of p- and n-type transistors are connected as input terminals, and the connected drain serves as the output port (common drain). The input electrical signal achieves an output waveform opposite to that of the input signal by controlling the single transistor to turn on/off the device (Note: the phase difference between the input and output waveforms is 180°). The basic logic principle is shown in Fig. 3.11.

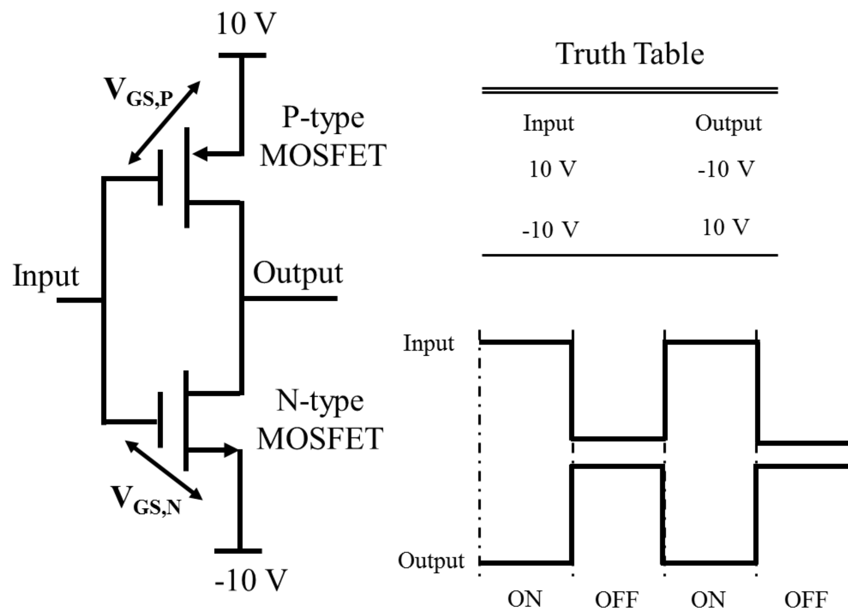

Fig. 3.11 CMOS NOT logic gate; main circuit comprises n-and p-type MOSFETs with common gate/drain as input/output port. Truth table and input/output waveform shown in left side for V_{DD} = ±10 V.

During a low supply voltage (V_{DD}), $V_{GS,N}$ decreases to 0 V when the input signal is 10 V, and the p-MOSFET will be in the OFF state; however, when $V_{GS,N}$ is 20 V, the n-MOSFET will turn on. The output is the input opposite voltage (-10 V). The truth table is shown in Fig. 3.9. However, V_{DD} is low when a high voltage is applied to the V_{DD} (e.g., ±100 V). When the input voltage is 10 V, $V_{GS,N}$ = 110 V; this input voltage is significantly greater than the threshold voltage of the p-MOSFET, and this device will turn-on. However, $V_{GS,P}$ = -90 V in this case, meaning that the p- and n-MSOFETs are in the on state simultaneously, and the inverter arm will be short circuited. Moreover, in current products comprising MOSFETs (like the 2Sj380, TOSHIBA, the V_{GS} range is ± 20V), the V_{GS} of the device can barely achieve a voltage exceeding 20 V.

This implies that if the diamond cascode is applied in high-voltage inverter circuits,

the turn-on and turn-off of the high- and low-arm devices must be controlled by two insulated gate drivers. Furthermore, the two-gate driver must maintain the in-phase output to ensure that the high- and low-arm devices in a high-voltage diamond inverter will not turn on simultaneously; otherwise, the circuit composition will become more complex, and a gate driver IC with a high output voltage will be difficult to realize.

In summary, to drive the diamond inverter in a high-voltage environment, we adopted a gate driver inverter with a common source as the output port. The basic schematic diagram is presented in Fig. 3.12, which differs from the conventional CMOS inverter schematic diagram shown in Fig. 3.11.

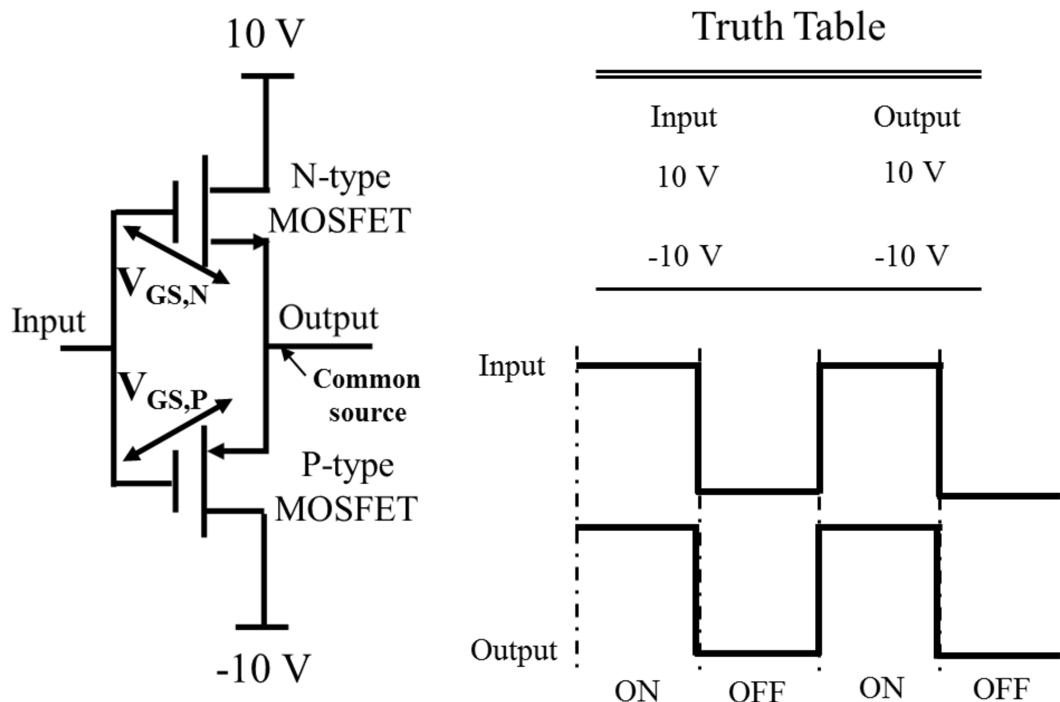

Fig. 3.12 Schematic diagram circuit of common source CMOS inverter; main circuit comprises n-type MOSFET (high arm) and p-type MOSFET (low arm) with common gate/source as input/output port; truth table and input/output waveform shown in left side for V_{DD} = ±10 V.

The common-source-type inverter applies the n- and p-MOSFETs as the high- and low-arms, respectively, because the supply bias is on the drain port. Meanwhile, $V_{GS,N}$ and $V_{GS,P}$ are defined at the input voltage, and the input voltage reaches one of the threshold voltages to turn on the device on one side because the potential of the source (the output port) is 0 V when the devices are in the OFF state. This connection method can prevent the two devices in the high/low arms being turned on simultaneously. This circuit structure has been used in the application of a 0-deadtime CMOS inverter [21]. Although this CMOS circuit structure does not result in opposite input and output signals, its output characteristics can be used as a signal amplifier of the same-phase input signal.

Therefore, based on the common-source-type CMOS inverter, we can achieve a same-phase voltage division signal by connecting a resistor in series on the drain side of the MOSFETs. Based on this circuit principle, a gate driver inverter suitable for driving high-voltage inverter circuits can be designed, of which the schematic diagram circuit is shown in Fig. 3.13.

The gate driver inverter circuit comprises enhancement-mode p- and n-MOSFETs in a common-source structure. This common-source port is no longer used as a voltage signal output terminal but is connected to the ground to ensure that the gate voltage is equal to the input voltage. Four resistors for voltage division are connected in series between the drain and V_{DD} of the p- and n-MOSFETs, and they are labeled as R1, R2, R3, and R4 in the figure. When the input voltage is -5 V (this voltage requires the

threshold voltage of the device), the p MOSFET will turn on, $V_A = V_{DD}\frac{R_2}{R_1+R_2}$, the n-MOSFET is still in the OFF state, and V_B = -V_{DD}. However, when Vin =5 V, the p-MOSFET will be turned off, V_A = -V_{DD}, and $V_B = V_{DD}\frac{R_3}{R_3+R_4}$. The truth table is shown in Fig. 3.13(b).

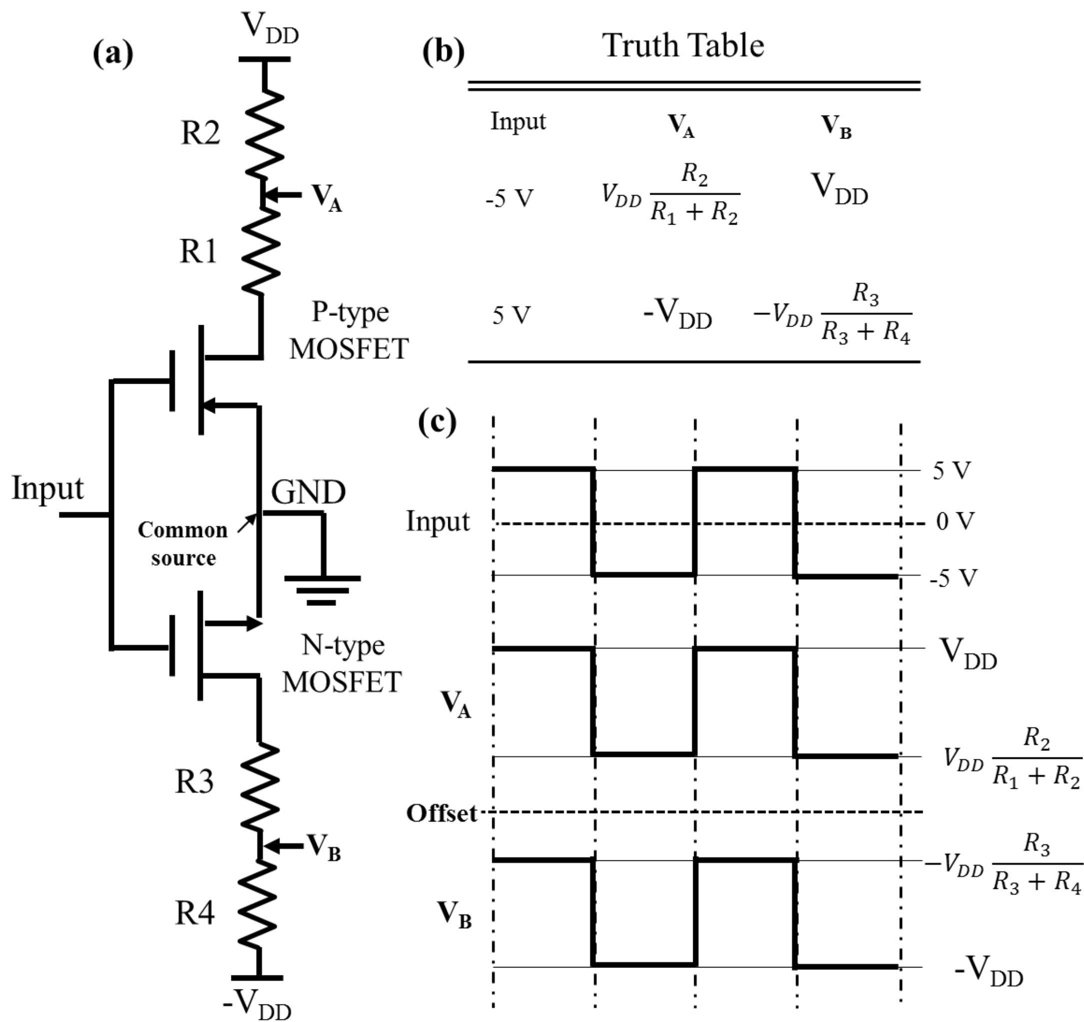

Fig. 3.13 (a) Schematic diagram of gate driver inverter circuit with common source; voltage division signal obtained by connecting a resistor in series on drain side of MOSFETs is proposed. (b) Truth table shows relationship between input voltage signal and V_A, V_B. (c) Theoretical input and output waveform of input voltage, V_A and V_B.

Based on the input and output signals in Fig. 3.13 (c), it is clear that when V_{DD} is not equal to 0, the absolute value of the potential$| \pm V_{DD} \frac{R_3}{R_3+R_4}|$ will always be greater than 0. This means that the rectangular wave signal voltage is increased. If the amplitude of the output signal (V_A,V_B) is greater than the threshold voltage of the power device in the inverter, then this dual-channel with the same-phase voltage signal can control the high and low arms of the inverter to turn on and off the device at a high supply voltage.

The actual circuit assembly and schematic diagram are shown in Fig. 3.14 (a). The signal generator is used to output a rectangular wave signal; the Si n-MOSFET (TK100E10N1) and Si p-MOSFET (2sj280) are connected by a common source. Five resistors are connected in series to the drain of each MOSFET (R = 100 Ω), and the resistance value can be adjusted for different V_{DD}. All electronic components are built in a terminal box. The circuit wiring diagram is shown in Fig. 3.14 (b).

At the operation voltage of 200 V (V_{DD} = 100 V, -V_{DD} = -100 V), the outputs of Ch1 and Ch2 are as shown in Fig. 3.14 (c). When the input signal voltage is 5 V to -5 V with a frequency of 1000 Hz, the output voltage signal increased, as per calculations. The amplitude of the waveform is 20 V, which is the upper limit of V_{GS} of the MOSFET, and it can control the switching of the MOSFET. Using this gate driver inverter, a high-voltage diamond inverter can be realized.

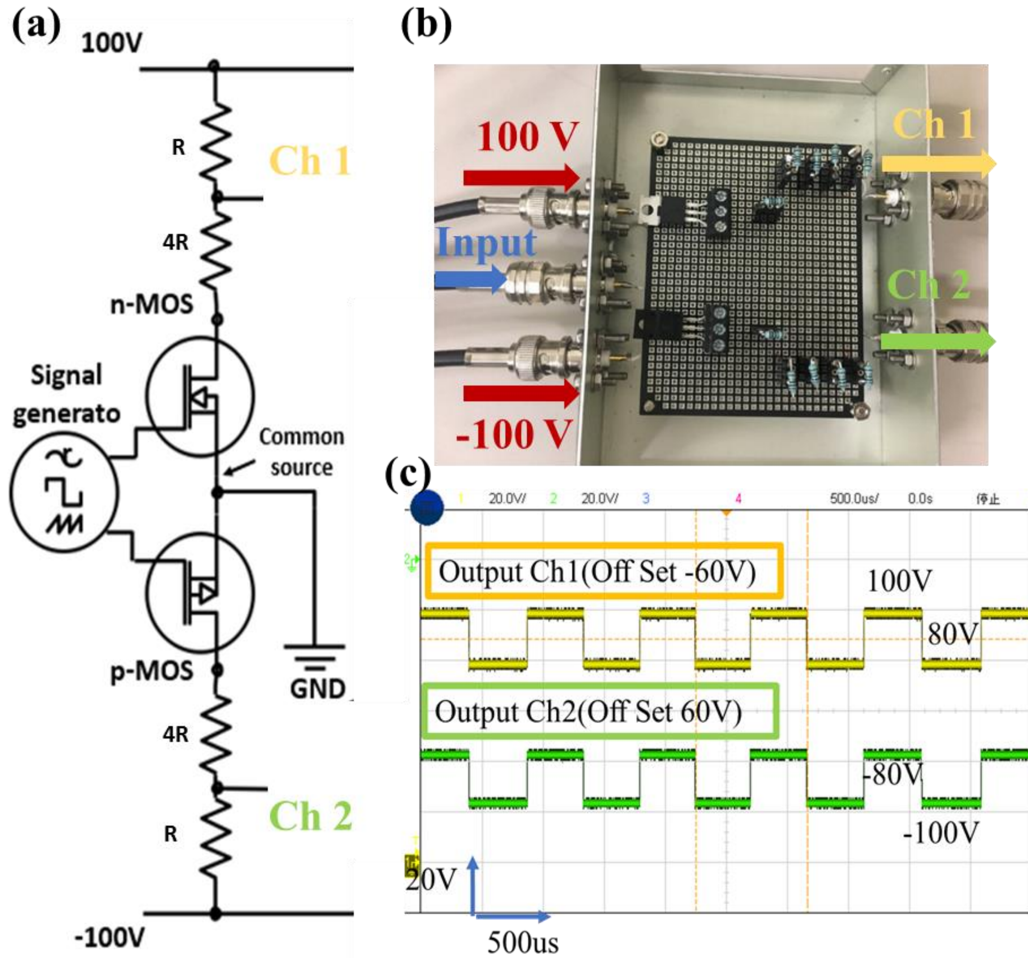

Fig. 3.14 (a) Gate driver inverter circuit; (b) circuit wiring diagram of gate driver inverter in terminal box. (c) Output of Ch1 and Ch2 with input signal of 5 V to -5 V; output voltage signal increased at operation voltage of 200 V.

Fig. 3.15(a) shows the circuit configuration of the diamond–GaN half-bridge complementary inverter. The inverter circuit primarily comprises two stages: the gate driver inverter circuit (Stage I) and a diamond–GaN half-bridge inverter (Stage II). In the Stage II diamond set in the high arm as a p-channel power device, the GaN cascode TPH3206PS is connected in the low arm.

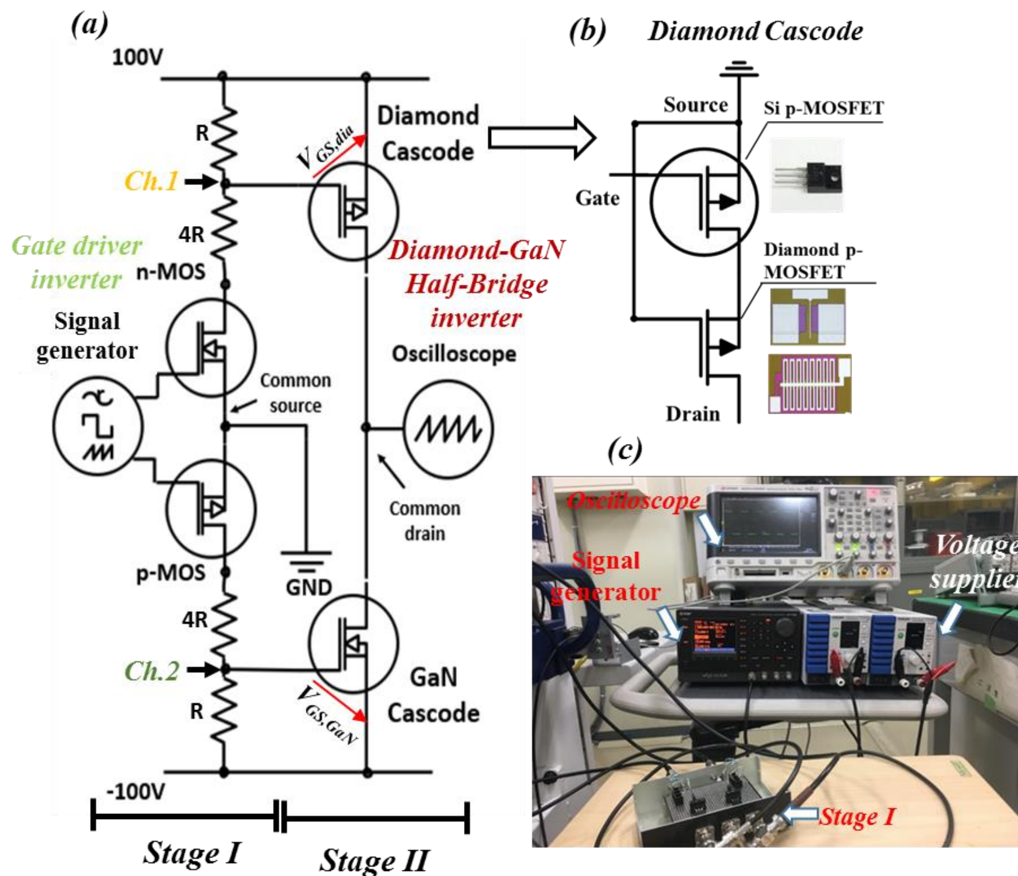

Fig. 3.15 (a) Diamond–GaN half-bridge complementary inverter circuit with double-stage structure. (b) Principle structure of diamond p-FET cascode. (c) Inverter circuit measurement environment of this study.

The same DC bias voltage (V_{DD} = 100 V, -V_{DD} = -100 V) was applied to both stages. The voltage outputs from the two channels of the gate driver inverter (Ch1 and Ch2 for high and low arms, respectively) are input to the diamond and GaN cascode, respectively. The assembly method of the diamond cascode (Fig. 3.15 (b)) has been presented in the previous section. The GaN cascode is connected to the circuit from the outside through the terminal box, and the inverter circuit measurement environment of this study is shown in Fig. 3.15 (c).

3.2.2 Switching speed enhancement by enlarging gate width in diamond cascode application of high-voltage half-bridge inverter

When the diamond-GaN half-bridge inverter switches at 200 V, the divided voltage states in Ch1 and Ch2 should be calculated using the following equations when resistors 4R and R are connected in series with the drain of the upper/lower devices in stage I (gate driver inverter as shown in Fig.3.13 (a)), as follows:

$$V_{Ch,Low} = \pm 100 \left(\frac{4R}{4R+R} \right) \quad (1)$$

$$V_{Ch,High} = 100 \quad (2)$$

Equations (1) and (2) represent Ch1/2 in the low and high states when the devices in stage I are turned ON and OFF, respectively. The load side of Stage II is connected to an oscilloscope to observe the output voltage waveform. $V_{GS,Dia}$ or $V_{GS,GaN}$ equivalent to the state of the device on the same side of stage II will be turned on only when the voltage signal input from Stage I is the set at a low state [Eq. (3)]. Otherwise, the device turns off [Eq. (4)].

$$V_{GS,\mathrm{ON}} = \pm 100 - V_{Ch,Low} \ \left(V_{TH} \leq V_{GS,ON} \leq V_{GS,B} \right) \quad (3)$$

$$V_{GS,\mathrm{OFF}} = \pm 100 - V_{Ch,High} = 0 \quad (4)$$

In Eqs. (3) and (4), V_{TH} is the threshold voltage of the diamond cascode and GaN cascode. $V_{GS,B}$ is the gate port breakdown voltage of the normally off low-voltage Si MOSFET in both cascode circuits. In this study, R = 100 Ω. The switching state and

truth table of the entire inverter circuit are shown in Fig. 3.16.

TRUTH TABLE OF THE DIAMOND-GAN HALF-BRIDGE COMPLEMENTARY INVERTER

Input	**Stage I**		**Channel state**		**Stage II**		**Output**
Signal generator	n-MOSFET	p-MOSFET	Ch.1	Ch.2	Diamond cascode	GaN cascode	Oscilloscope
5V	*ON*	*OFF*	*High*	*Low*	*ON*	*OFF*	*100*
-5V	*OFF*	*ON*	*Low*	*High*	*OFF*	*ON*	*-100*

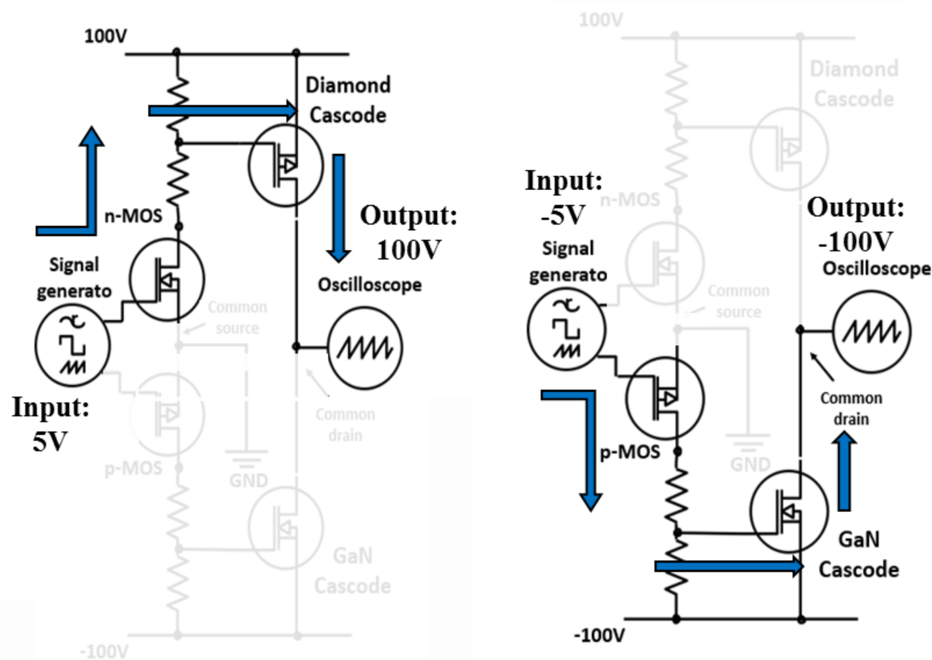

Fig. 3.16 Truth table of diamond–GaN half-bridge complementary inverter circuit with double-stage structure. Voltage input and output transmission path of input voltages 5 V and -5 V.

Based on calculations by referring to the schematic diagram, the input signal was amplified, and the inverter action of DC/AC conversion was realized. Next, in the experiment, the diamond–GaN half-bridge inverter operation was confirmed, and the switching waveform of the lateral-type diamond cascode with $W_G = 25$ μm in the half-bridge inverter is shown in Fig. 3.17. The switching frequency of the input signal from

the signal generator was 1000 Hz.

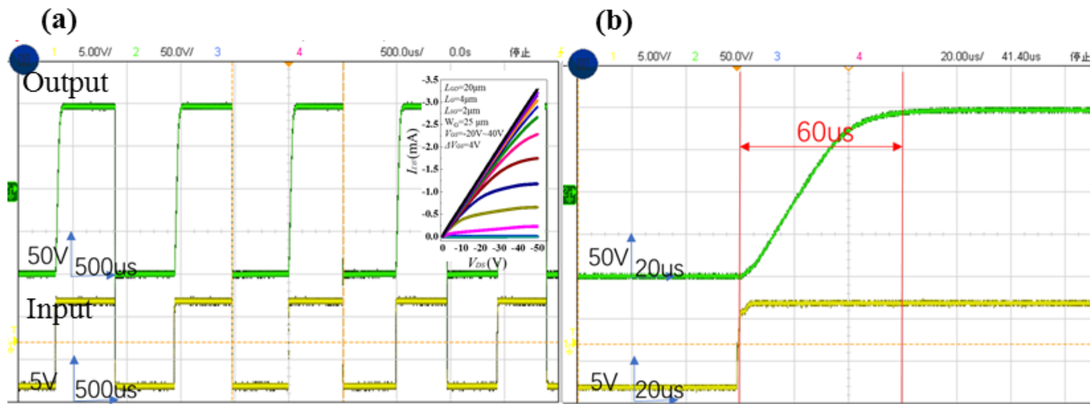

Fig. 3.17 (a) Output voltage waveform of lateral-type diamond cascode with enlarged gate width diamond MOSFET (W_G = 25 μm) in half-bridge inverter (operation voltage 200 V). (b) Voltage rising time (T_{on}) of diamond cascode side when high arm turns on; T_{on}= 60 μs.

The output of the half-bridge inverter shows a switching time (T_{on}) of 60 μs in the upper arm during a high operation voltage of 200 V when the diamond MOSFET with a gate width of 25 μm was used. The delay could be due to the maximum drain–current imbalance between the smaller gate width of the diamond MOSFET compared with the GaN n-HEMT in the GaN cascode; the shorter channel width resulted in the current driving capability between two sides in the inverter. In fact, in Si MOSFET products, a structure with a larger gate width is often used to increase the output current of the device and increase the output power. Therefore, increasing the gate width of the diamond MOSFET to increase the output current of the diamond MOSFET can reduce this imbalance effect. This is the most important reason for fabricating diamond MOSFETs with large gate widths, as described in Chapter 2.

The switching waveform of the lateral-type diamond cascode with an enlarged gate width diamond MOSFET (W_G = 500 μm) in a half-bridge inverter is shown in Fig. 3.18.

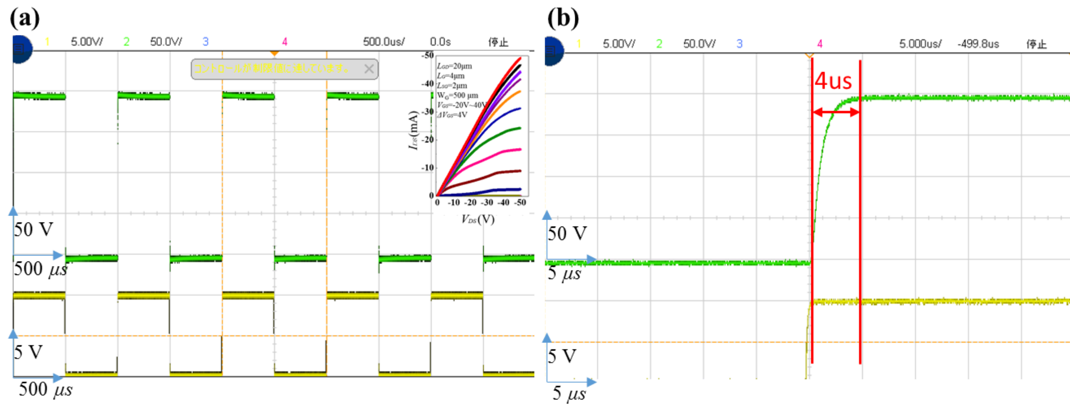

Fig. 3.18 (a) Output voltage waveform of lateral-type diamond cascode with enlarged gate width diamond MOSFET (W_G = 500 μm) in half-bridge inverter (operation voltage 200 V). (b) Voltage rising time (T_{on}) of diamond cascode side when high arm turns on; T_{on} = 4 μs.

By enlarging the gate width of the diamond MOSFET in the high arm, the switching speed of the diamond cascode side improved significantly; the ton reduced to 4 μs, which was 15 times faster than that of the diamond MOSFET with W_G = 25 μm.

When the vertical-type MOSFETs are applied in the half-bridge inverter, because of the large gate width of the multi-finger structure, a strong electrothermal effect will be produced when switching devices, and the V_{DD} value will be adjusted based on the actual situation in the next experiment.

The switching waveform of the vertical-type diamond cascode with an enlarged gate width diamond MOSFET (W_G = 1 mm) in the half-bridge inverter is shown in Fig. 3.19.

Under a supply voltage of 80 V, the vertical-type MOSFET half-bridge inverter operation was confirmed, the switching speed further improved, and the ton decreased

to 2.3 μs. However, this MOSFET broke down when the supply voltage increased to 100 V. However, the ton is related to the time constant, which is affected by the capacitance and resistance in the switching circuit, and is independent of the supply voltage.

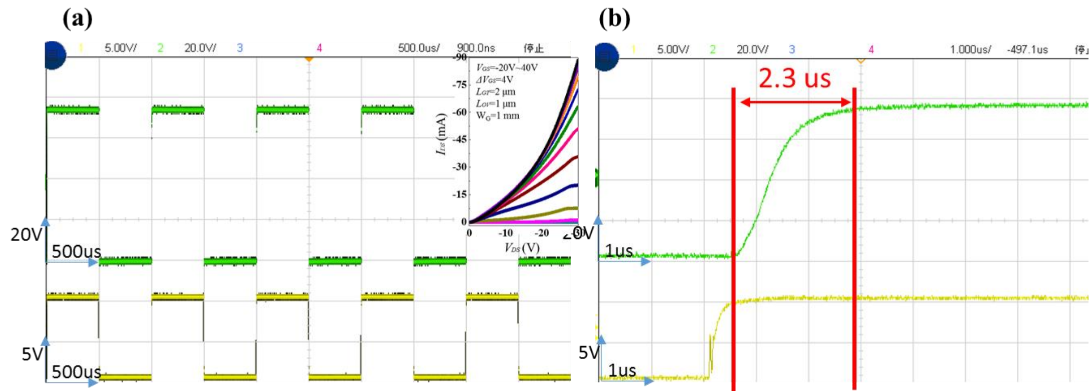

Fig. 3.19 (a) Output voltage waveform of vertical-type diamond cascode with enlarged gate width diamond MOSFET (W_G = 1 mm) in half-bridge inverter (operation voltage 80 V). (b) Voltage rising time (ton) of diamond cascode side when high arm turns on; ton = 2.3 μs.

The diamond cascode with an enlarged gate width diamond MOSFET (W_G = 2 mm) shows T_{on} = 1.8 μs (in 80 V) (Figs. 3.20 (a)(b)); however, the diamond MOSFET with W_G = 5 mm applied to the inverter shows T_{on} = 1.6 μs (in 150 V) (Figs. 3.20 (c)(d)). This is because no significant enhancement was observed in the maximum current between the two devices, and not all trench channels were operating as intended when the devices with longer gate widths were turned on, particularly when switching at high frequencies. Furthermore, the devices (including the resistances in the stageI) switching in high frequency will emitted heat, thereby could be a reason decreasing the switching speed. However, with the increase in the gate width of the diamond MOSFET, the

current driving capabilities of the diamond and GaN cascode were balanced in the half-bridge inverter, and the switching improved.

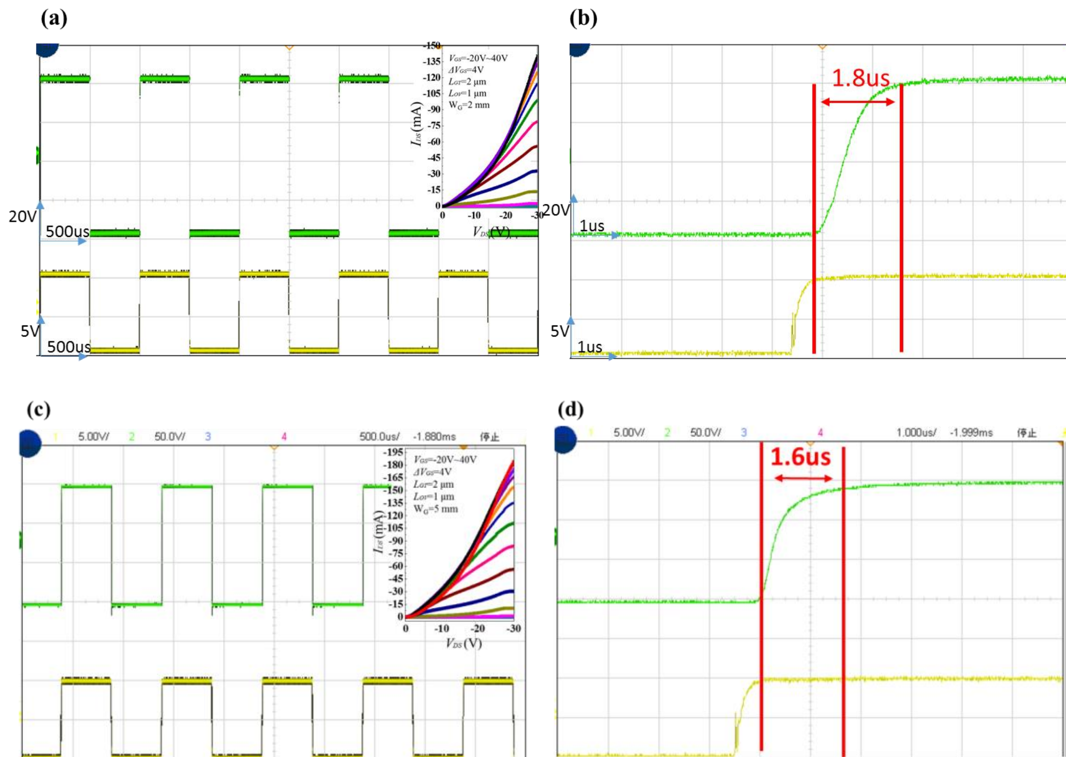

Fig. 3.20 (a) (b) Output voltage waveform of vertical-type diamond cascode with enlarged gate width diamond MOSFET (W_G = 2 mm) in half-bridge inverter (operation voltage 80 V); Ton= 1.8 μs. (c)(d) Output of vertical-type diamond cascode with enlarged gate width diamond MOSFET (W_G = 5 mm) in half-bridge inverter (operation voltage 150 V); ton = 1.6 μs.

3.3 Conclusion

In this chapter, the application of a C–H diamond MOSFET in the circuit applications was discussed. Using the cascode structure, the threshold voltage of the cascode circuit was regulated by a combined normally off Si MOSFET, and the advantages of the diamond MOSFET (slightly current density loss and high breakdown voltage) were retained. The diamond cascode p-type power device with a normally off operation can be realized stably.

Consequently, the threshold voltage of the normally on lateral-type diamond and vertical-type C–H diamond MOSFET shifted to -1 V via the cascode structure. A high breakdown voltage was achieved when applying the lateral-type diamond MOSFET in cascode, with $L_G = 2$ μm, $L_{SG} = 2$ μm, and $L_{GD} = 26$ μm. This diamond cascode reached a breakdown voltage of -1735 V when $V_G = 0$ V.

Furthermore, this is the first study that applied a diamond device as a p-channel and GaN cascode as an n-channel in a high-operation half-bridge complementary inverter. We successfully realized inverter operation at 1000 Hz under high-voltage conditions (200 V for lateral-type diamond cascode, and 150 V for vertical-type C–H diamond cascode) using a two-stage circuit structure (realized using an on-gate driver circuit). By increasing the gate width of the diamond MOSFET, the current of the MOSFET improved. In addition, Fig. 3.21 summarizes the relationship between the maximum current value of the C–H diamond MOSFETSs and T_{on} reported in this chapter. To ease

comparison, the current values of all diamond MOSFETs were obtained based on a V_{DS} of -30 V. As the best data, the switching speed enhanced with Ton = 1.6 μs after applying W_G = 5 mm in the vertical-type diamond MOSFET to the upper arm of the diamond–GaN half-bridge complementary inverter.

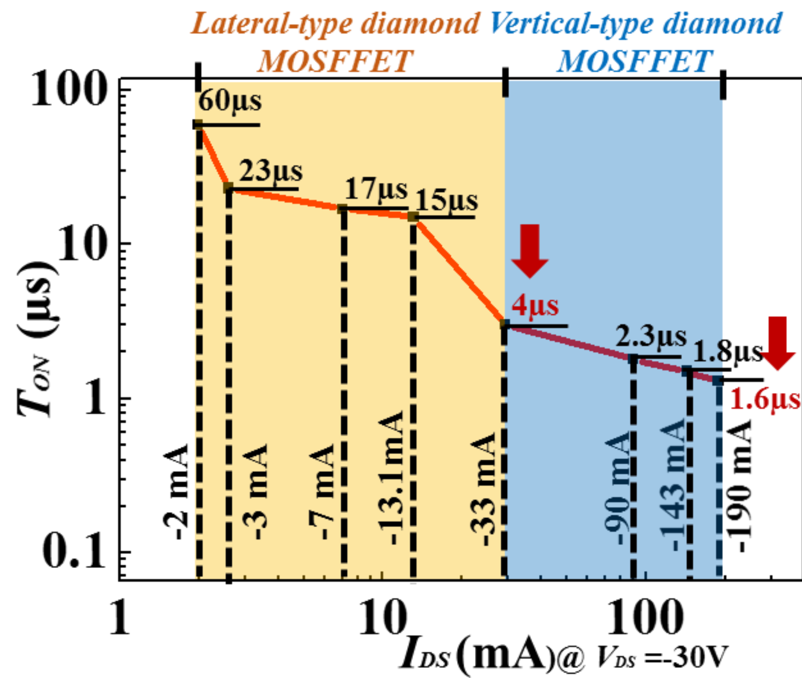

Fig. 3.21 Summary of relationship between different maximum currents of C–H diamond MOSFET @ V_{DS} = -30 V *and* T_{on} *in this chapter.*

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Chapter 4

Formation of the C-Si bonded diamond surface and normally-off C-Si diamond MOSFET with the Wide Temperature Range Stability

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4.1 The C-Si bonded on the diamond surface

Although the surface modification of diamond exhibits p-conductivity with the hydrogen-terminated surface, the termination of the diamond surface is crucial in determining the characteristics of diamond semiconductors. The electron affinity for C-H surfaces is negative and the spontaneous polarization effect of the C-H dipole to adsorbents induces the 2DHG and realizes the operation of the C-H diamond MOSFETs. However, the O-termination of diamond owing to the insulative physical property, and the high density of interface states of OH- termination hinder its application as a conductor for the 2DHG diamond MOSFETs.

A high-performance diamond p-channel MOSFET can be fabricated by modifying the surface of diamonds with hydrogen termination with a high hole density of approximately 10^{13} cm^{-2}. The C-H diamond MOSFETs with an atomic layer deposition (ALD)-Al_2O_3 as the gate insulator exhibit high 2DHG density at the Al_2O_3/diamond interface; this is because of the inset negative fixed charge in Al_2O_3, and the MOSFETs exhibit a wide temperature operation range[1]. Additionally, various applications of insulating films on diamond FETs have been reported[2][3]. Characterizations such as the normally-off operation and high breakdown voltage have been achieved in the C-H diamond FETs[4]. However, for more reliable high-voltage applications, SiO_2/diamond interfaces are preferred because of charge controllability and reliability in SiO_2[5].

Si is a semiconductor material with a diamond cubic lattice structure. Each Si atom

forms covalent bonds with the other four Si atoms in the sp^3 hybrid orbit, forming a regular tetrahedral structure. The Si termination on the diamond surface can be formed by creating a dangling bond to rebuild the covalent bond at the Si/diamond. For Si crystals, it is easy for the outermost Si atom to have an unsaturated dangling bond if the lattice terminates at the interface; it is easier to form such a surface state if there are only a few monolayer Si atoms. Si-terminated diamond is formed on the C-H diamond under ultra-high vacuum system annealing at 920 °C by depositing a 2.7 Å thick layer of silicon[6]. At this high temperature, the hydrogen layer on the diamond surface is removed; therefore, the carbon on the surface has dangling bonds that can interact with the Si atoms to form the C-Si bonds on diamond.

For the C-Si dipole on the diamond surface, the difference between the electronegativities of C and Si atoms is 0.7 Pauling units (C: 2.5, Si: 1.8) [13]. In contrast, in a C-H dipole, the difference between the electronegativities of C and H (C: 2.5, H: 2.1) is 0.4 Pauling units. The negative electron affinity of the C-Si diamond has a similar polarity to that of the C-H diamond, where the electron affinity is negative. The band offset to SiO_2 is sufficient to accumulate holes (Fig. 4.1).

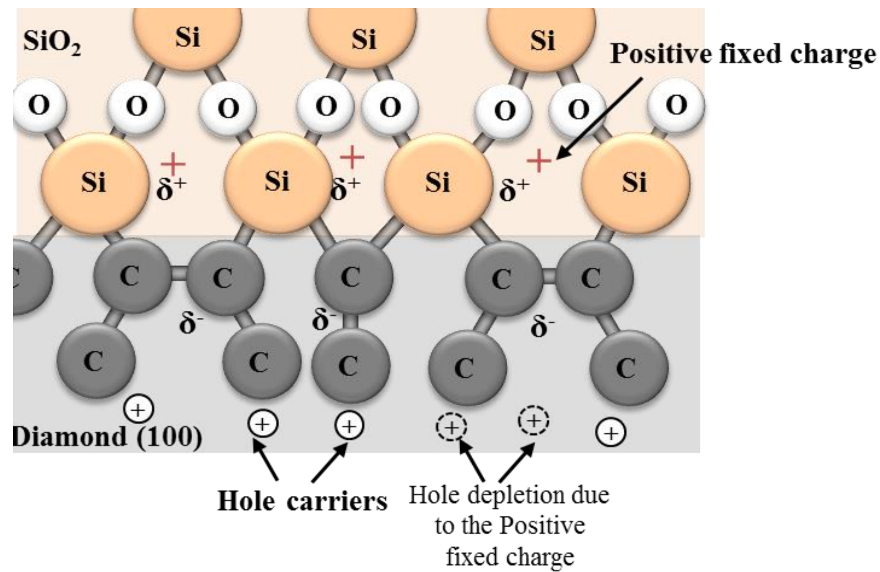


Fig.4.1. Schematic hole accumulation on the C-Si diamond surface at the diamond/SiO_2 interface. In addition, the positive fixed charge in the SiO2 may deplete some hole carriers, which were induced by the C-Si dipoles under the electric field.

During the oxidation process in TEOS-CVD for SiO_2 layer formation, in contrast to alumina, there will be a few positive fixed charges in the SiO_2 film, and the hole carriers induced by spontaneous polarization will be depleted, which makes it possible to realize the absence of the 2DHG layer without an electric field. SiO_2 is used as the pass passivation layer of the Si-terminated diamond.

In the case of the SiC/diamond interface, the valence band maximum of 3C-SiC is lower than that of diamond by more than 1.5 eV when the diamond is H-terminated [7]. A similar situation is expected at the SiO_2/diamond interface because the termination of diamond is inevitably a C-Si bond, which has a similar dipole moment to that of C-H. If the electron affinity is approximately -0.9 eV [13], the band offset is sufficient for holes to accumulate at the SiO_2/diamond (approximately 1.0 eV), which can be used as

a p-channel for fabricating the diamond MOSFETs with a C-Si bonds.

4.2 C-Si bonded diamond surface formation at the SiO_2/diamond interface

Formation of dangling bonds at the Si and diamond interface is crucial for forming a C-Si bond on the diamond surface. A high-pressure high-temperature (HPHT) synthetic Ib (100) diamond substrate with a nitrogen concentration of 10^{18}- 10^{19} cm^{-3} was processed using hot mixed acid treatment (H_2SO_4:HNO_3 = 3:1) at 240 °C and cleaned with an organic solvent. Thereafter, a 2 μm homoepitaxial undoped diamond layer was deposited on the diamond substrate via microwave plasma-assisted chemical vapor deposition (MPCVD),which reduced the nitrogen concentration to 10^{16} cm^{-3}[8]. Afterwards, the diamond substrate underwent UV irradiation in an O_3 atmosphere for 3 h to form oxygen terminals on the surface. This is crucial for the formation of the C-Si bond on the SiO_2/diamond interface. Because C=O diamond surface are reduced in a high temperature and hydrogen atmosphere, dangling bonds are formed on the diamond surface through the detachment of oxygen atoms. Additionally, an oxygen-terminated diamond provides a good interface bonding state for the subsequent deposition of silicon oxide film. Thereafter, a 260 nm (above 230 nm) SiO_2 layer was deposited via tetraethyl orthosilicate CVD (TEOS-CVD)[9].

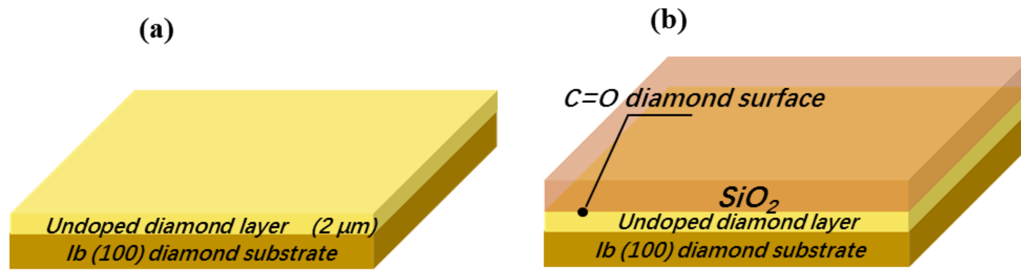


Fig.4.2. (a) A 2 μm homoepitaxial undoped diamond layer deposited on the diamond substrate via MPCVD. (b) The SiO_2 layer was deposited after C=O diamond formed via UV-Ozone treatment.

To make the diamond/SiO_2 interface fully react with the reducing gas at a high temperature to form a C-Si diamond surface, a strip structure was etched on the SiO_2 film to form SiO_2 coverage areas with different widths by photolithography and inductively coupled plasma-ion reactive etching (ICP-RIE) with C_3F_8 gas. Herein, photoresist is required to block the parts that do not need to be etched, and the following should be considered during the experiment:

1. The surface of SiO_2 deposited via TEOS-CVD is hydrophobic, which is same with the hydrophobic of the photoresist (TSMR-27CP). There is a high probability that the entire sample surface cannot be uniformly covered when coating the photoresist, which leads to the failure of lithography of the sample. This is because of humidity in the air in the clean room. Before coating the photoresist, a 180° heating plate was used for 5 min to remove any moisture on the surface of the sample completely.
2. Using two photoresist layers (TSMR-27CP and PMGI-SF5) as the mask of ICP-

RIE will hinder the removal of the residual photoresist after etching. Therefore, it is enough to use a single layer of photoresist with TSMR-27CP.

After etching, the widths of the etched area and the SiO_2-covered area were similar, that is, both were 5, 3, and 1 μm (Fig. 4.3).

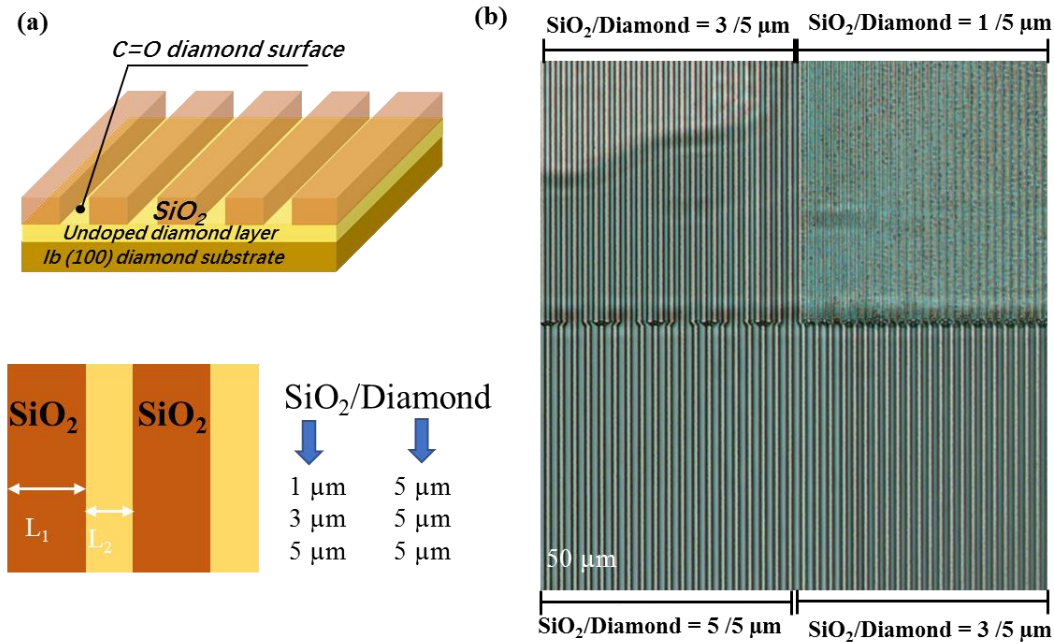


Fig.4.3. (a) Strip structure etched on the SiO_2 film Via ICP-RIE with different cover area (b) Optical microscope picture of the SiO_2 strip structure on the diamond surface.

To satisfy the reaction conditions of high temperature and reducing gas required for the formation of C-Si bonding, B-doped selective diamond growth was obtained via quartz tube-type MPCVD [10] using a mixture gas, the [TMB]/[CH_4] and [CH_4]/[Total gas flow] ratios were 9000 ppm and 5%, respectively . Because of the high-temperature stability of SiO_2, its use as a mask for selective diamond growth in MPCVD [11], and the C-Si formation under selective diamond growth conditions has also been discovered

[12]. The microwave, power chamber pressure, and growth temperature were 360 W, 110 Torr, and above 800 °C, respectively (Fig. 4.4). During this process, the boron-doped diamond grew in areas that were not covered by SiO_2. In addition, at the diamond/SiO_2 interface covered with SiO_2, the Si-O bond near the diamond surface broke and formed a dangling bond. Thereafter, a C–Si bond was formed at the SiO_2/diamond interface (Fig. 4.4 (c)).

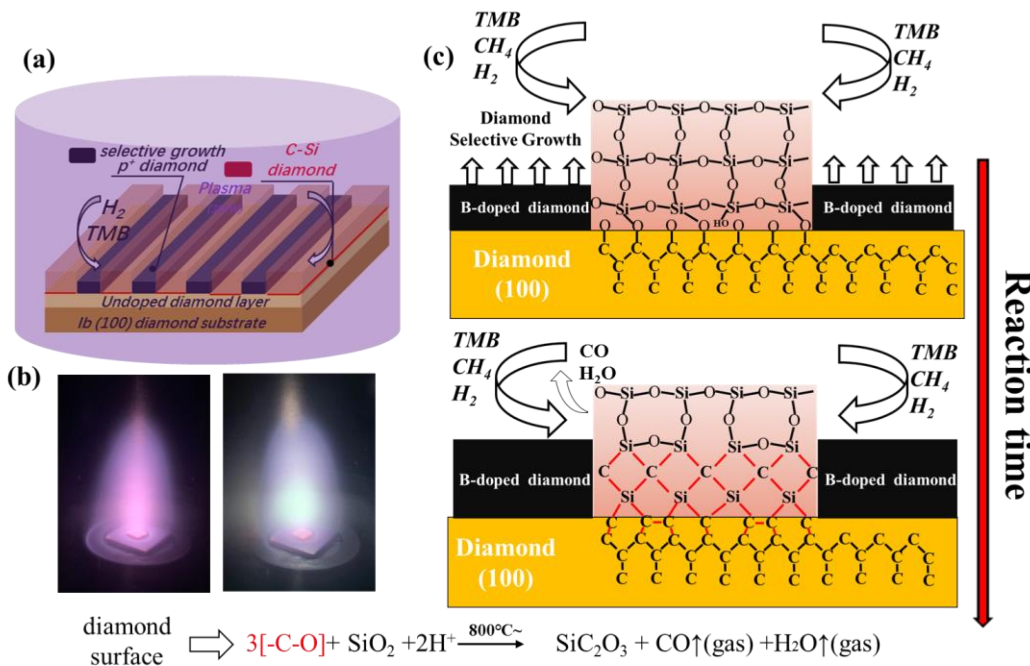


Fig.4.4. (a) B-doped diamond selective growth via quartz tube-type MPCVD (b) image of the sample B-doped diamond selective growth via quartz tube-type MPCVD, the Purple plasma is when only H_2 *is introduced into the chamber, After adding TMB and* CH_4 *gas, a white plasma appears, and the temperature of the substrate is above 800°. (c) Schematic formation of the C-Si diamond surface. The proposed chemical equation for this reaction is written below.*

As CH_4 participates in the reaction, more than one layer of C-Si bond is formed on the interface of SiO_2/diamond. Additionally, CH_4 and H_2 are crucial for the formation of

the C-Si layer because this is the condition necessary for diamond growth. Moreover, maintaining the sp^3 bonds of diamond is crucial for forming a multi-layer C-Si bonded diamond surface. During the reaction, the ionic oxygen formed by bond breaking combines with H_2 to form water vapor that leave the reaction, and the C in the excess CH_4 group forms CO.

Because the C=O diamond surface and the lower SiO_2 surface participate in the reduction, the bonding mode of the covalent bond at the interface is C-Si-O. Similar reactions in the SiO_2/graphite interface under high temperature and reductive conditions to substitute O atoms with C atoms and form C–Si bonds have been reported by Sen et al. [13]and Mitani et al.[14]. The C-Si-O surface is very important for the high electric field mobility of the C-Si diamond MOSFETs. The high interface state density of the C-O-Si interface will decrease the electric field mobility. This will be discussed in the section on the characteristic analysis of the C-Si MOSFETs.

The in-depth distribution of element concentrations in the SiO_2-covered area was analyzed via secondary ion mass spectroscopy (SIMS). After SIMS measurement, the SiO_2 film on the diamond substrate was removed using hydrofluoric acid (HF); however, the C-Si diamond surface remained. The C-Si diamond surface was evaluated via X-ray photoelectron spectroscopy (XPS) (VersaProbeII, UIVAC-PHI Inc.) with a monochromatic Al Kα line (line width = 0.85 eV, energy =1486.6 eV) as the excitation source. The angle of photoelectron detection (θ) was 45°, and the diameter of the surveyed area was 100 μm. The XPS results were analyzed using a PHI MultiPak.

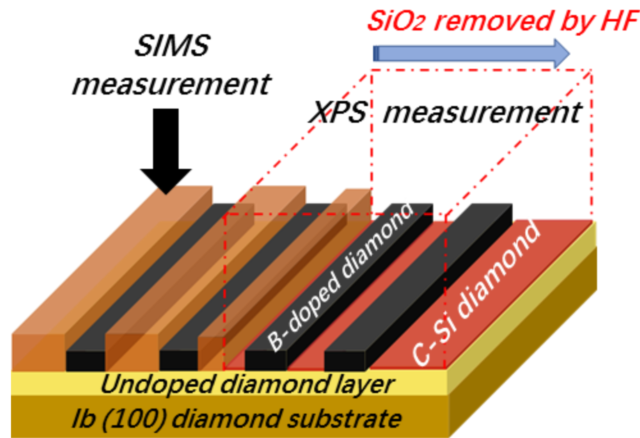


Fig.4.4. SiO_2-covered area was analyzed via SIMS. After SIMS measurement of the B-doped diamond selective growth, and the C-Si diamond surface is evaluated via XPS after removing the SiO_2 using HF.

4.2.1 The analysis of SIMS and XPS measurement results on C-Si diamond surface

The distribution of the H_2 concentration at the diamond/SiO_2 interface after the growth of the B-doped selective diamond is shown in Fig. 4.5, which is 5×10^{20} cm^{-3}. In addition, the H_2 concentration of the Al_2O_3/diamond interface on a (100) diamond substrate is 2.8×10^{22} cm^{-3} [23], and the H concentration is approximately two orders of magnitude lower at the diamond/SiO_2 interface. The existence of hydrogen is because the diameter of the H atom is very small, which allowed that hydrogen atoms enter SiO_2 to participate in the chemical reaction of the SiO_2/diamond interface during the B-doped diamond selective growth. The sources of hydrogen include the water

molecules on oxygen terminated (C-O) surface, because original surface is C-O. Methyl groups exist in SiO_2 deposition. Also the H radicals come from the decomposition of the reaction gas CH_4/H_2 during diamond growth conditions. On the other hand, diameter of H atoms is relatively small. Hence, it is inevitable that H atoms enter SiO_2 in this process. Thus, the H is detected in the SIMS results, it should be noted that the hydrogen concentration at the SiO_2/diamond interface is less than 1/50 at the Al_2O_3/C-H diamond interface. The p-type conductive channel can be formed by C-Si diamond mainly. Based on the above phenomena, the following C-Si formation has been considered. The surface C atoms react with Si atoms in SiO_2 and likely to replace O atoms of SiO_2 through the edge of the SiO_2 strip structure to participate in the reduction reaction, to form the C-Si bond formation during high temperature MPCVD with CH_4 and H_2 gas.

Similarly, there is also high H content on the SiO_2 surface, and the secondary ion intensity of the C suggests that the upper surface is etched by hydrogen plasma, which makes SiO_2 on the upper surface react with CH_4. This surface product with high carbon content could be a diamond-like-carbon (DLC) layer[15][16]. The generation of this DLC layer significantly reduces the H atoms entering the middle part of the SiO_2 film in the subsequent reaction, thus there is only less H content in the middle part of the longitudinal element distribution of SiO_2, which is also reflected in the SIMS results.

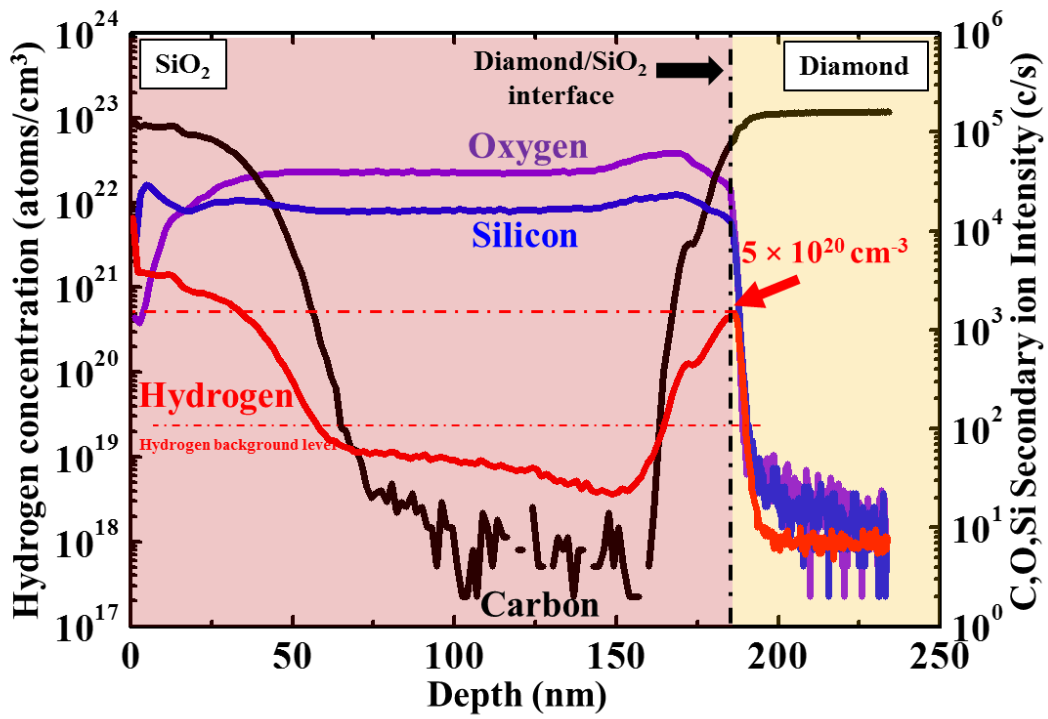


Fig.4.5. Longitudinal distribution of element concentrations in the SiO_2 covered area after formation of a C-Si bond at the diamond/SiO_2 interface.

However, the low C-H bond density at the interface is because the C atoms on the diamond surface terminated by oxygen, which react with Si atoms in the SiO_2, and they are likely to replace oxygen atoms at the diamond/SiO_2 interface through the edge of the strip structure of SiO_2. Thus, it can participate in the reduction reaction of the formation of the C-Si diamond surface in the MPCVD, which is also illustrated in the XPS results.

The XPS wide-scan survey spectrum of the C-Si diamond surface of the SiO_2/diamond is 5 / 5 μm with binding energy (BE) ranging from 0 to 1100 eV, as shown in Fig. 4.6(a). The Si2s (150.1 eV) and Si2p (99.1 eV) peaks for Si can be clearly observed, thereby

indicating that C-Si bonds are not etched by HF from the diamond surface. The B peak exists because 50% of the surveyed area comprises the B-doped diamond. Fig. 4.6 (b) shows the C1s core level of the C-Si diamond surface. There are four curve-fitted peak components in the C1s peak. The most evident peak is the bulk diamond component (B_C) at a BE of 284.8 eV. P_1 is the C-O peak at a BE of 286.1 eV, C-O mainly comes from the surface of the selectively grown diamond after the UV-ozone and the oxidation reaction in TEOS-CVD. The C-Si peak appears only at a position that is lower than the BE of the B_C peak because the electronegativity of C atoms is higher than that of Si atoms. The significant components such as P_2 and P_3 are observed at -1.38 eV and -2.85 eV, respectively, relative to B_C with an intensity ratio of P_2:P_3=2.95:1.45; these components are related to C-Si bonding. This is because the intensity ratio is the same as that reported by Schenk, Pakes et al. at a monolayer of C-Si bond on the diamond (100) surface[6]. However, by analyzing the intensity ratio of B_C to the P_2 and P_3 components in Fig. 5(b), there are 3 monolayers of C and Si atoms on the diamond surface.

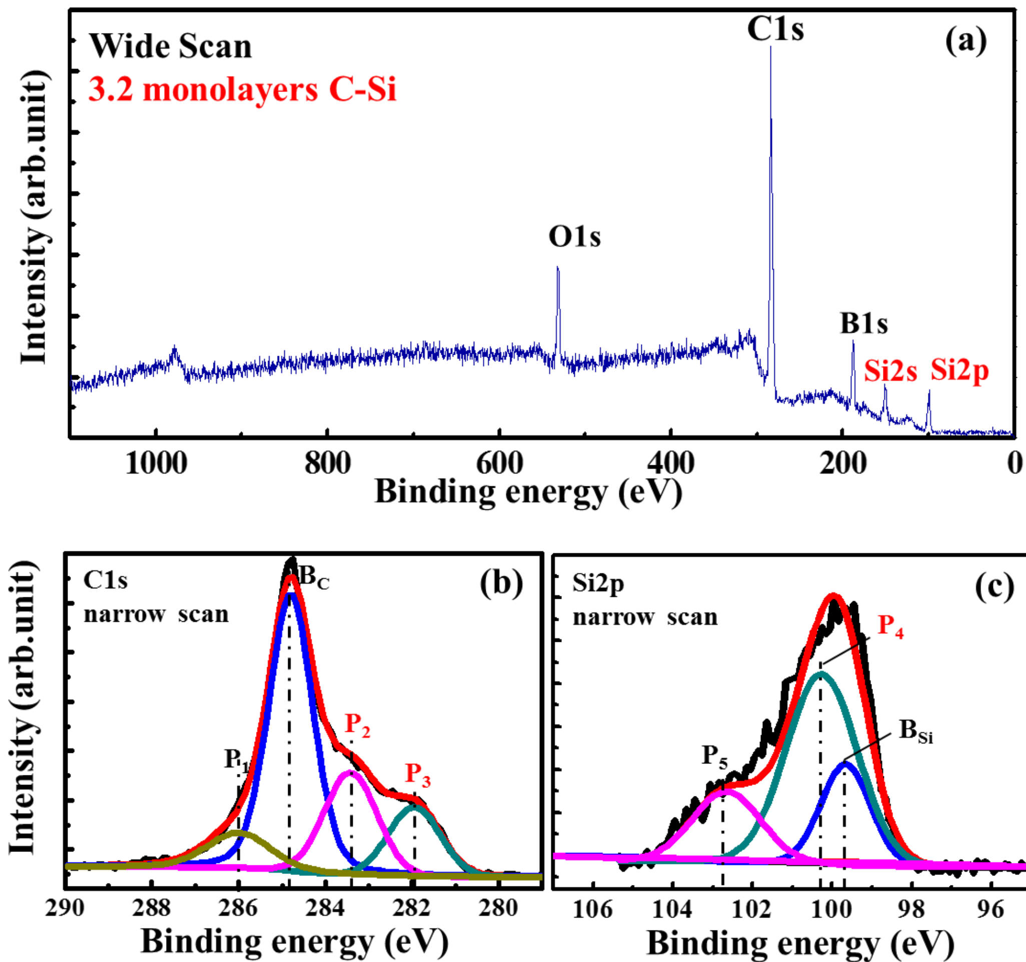


Fig. 4.6. (a) Wide scan and (b) narrow scan of C1s and (c) Si2p core levels on the C-Si diamond surface in XPS survey spectrum. P_2, P_3, and P_4 component peaks suggest that there are C-Si bonds on the diamond surface.

During the narrow scan in the Si2p region (Fig. 5(c)), with the BE ranging from 107 to 95 eV, the BE of the bulk Si (B_{Si}) is 99.66 eV. The P_4 peak at this BE indicates the presence of C-Si bonds on the diamond surface. The other components (P_5 at 102.65 eV) represent the oxide of Si, which suggests that Si atoms with positively electric charge Si^{2}+ are bonded to complex O atoms [17]. This chemical bond structure at the diamond/SiO_2 interface suggests that the SiC_2O_3 [18] is formed with the C-Si-O

bond[19] [20]during the selective epitaxial growth.

Notably, there are 3 monolayers of Si atoms on the C-Si diamond surface when analyzing the composition of C1s. This shows that the C-Si diamond surface is not only a monolayer termination but also a multi-layer structure extending from the diamond surface to the inside of the SiO_2 film.

Decreasing length of SiO_2 in the strip structure indicates that the SiO_2/diamond interface in the strip easily reacts with the gas in the MPCVD in the selective growth process, and the XPS results also show different layers of the C-Si bonding (Fig. 4.7). In the region where SiO_2/diamond = 3/5 μm, there is 3.8 monolayer C-Si bonding, and in the region where SiO_2/diamond = 1/5 μm, the C-Si bonded layer increases to the 4.2 monolayers.

In the survey spectrum of the diamond region, XPS results show that there is no Si peak. Moreover, there is no C-Si bonding at the BE of C1s and Si2p, which indicates that there are no free Si-containing groups to form C-Si bonded diamond surfaces in the selective growth diamond region during the formation of C-Si bonding in MPCVD.

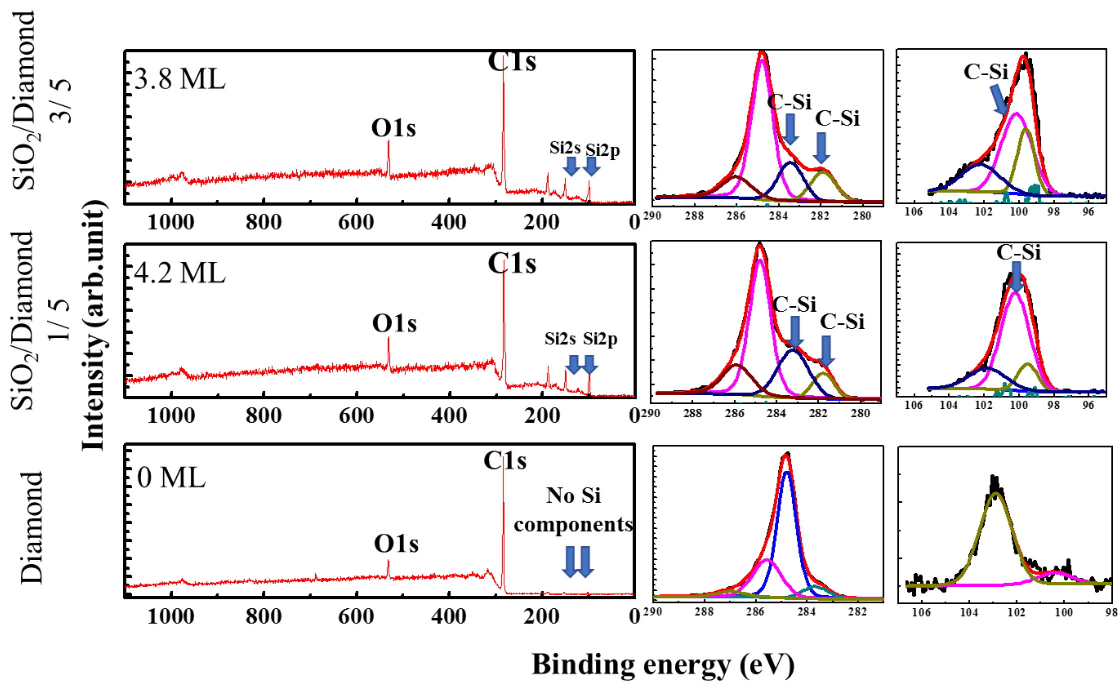


Fig. 4.7. XPS wide-scan survey spectrum and the narrow-scan of the C1s, Si2p in different SiO_2 length regions on the strip structure surface

4.3 Fabrication of the C-Si-bonded diamond MOSFETs

The fabrication of the C-Si diamond MOSFETs is shown below. To form the C-Si bonded diamond surface in the MOSFET channel, the strip-like source-drain diamond selective growth region is etched on the surface of the diamond substrate covered by SiO_2.

The pre-treatment of samples is similar to that in the previous section. First, an HPHT synthetic (100) diamond substrate was processed using hot mixed acid treatment and cleaned with an organic solvent. Thereafter, a 2 μm homoepitaxial undoped diamond

layer was deposited on the diamond substrate via MPCVD using a mixture of H_2 (394 sccm), CH_4 (3 sccm), and CO_2 (3 sccm). The microwave power, chamber pressure, and temperature during growth were 750 W, 35 Torr, and 600 °C, respectively. To form O_2 terminals on the diamond surface, the H on the diamond surface was removed through UV irradiation in an O_3 atmosphere for 3 h. Thereafter, a 260 nm SiO_2 layer was deposited via TEOS-CVD. Dry SiO_2 etching for the selective growth of the heavily B-doped diamond (p++) was carried out via ICP-RIE using C_3F_8 gas (Fig. 4.8).

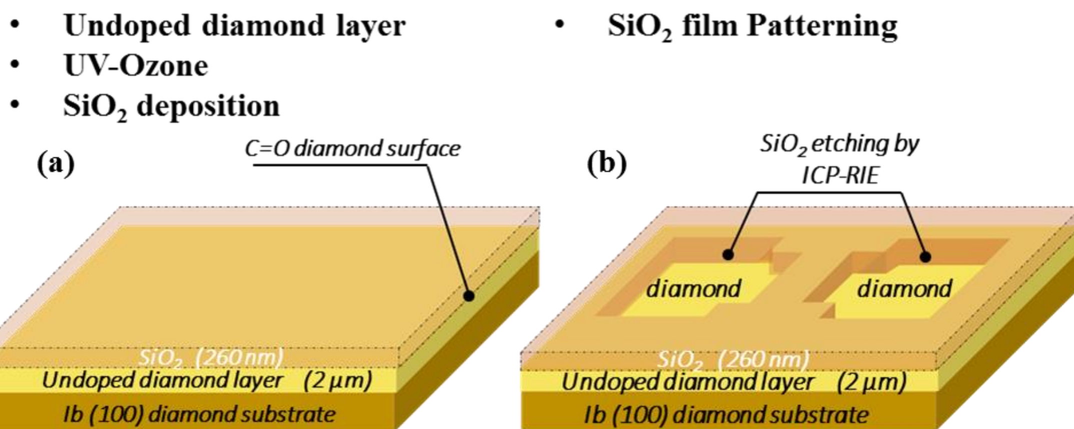


Fig. 4.8. (a) *The undoped diamond layer and the SiO_2 film (260nm) deposition on the (100) diamond substrate. (b) The source/drain diamond selective growth region*

The p++ selectively grown diamond was deposited via quartz tube-type MPCVD under similar conditions to those for the formation of the C-Si diamond surface. During this process, C-Si bonded layers were formed at the interface between SiO_2 and diamond, as discussed in the previous subsection. After selective growth, Ti/Pt/Au (20 nm/30 nm/100 nm) was deposited as the source and drain electrodes using an electron beam deposition system (Fig. 4.9 (a)).

Thereafter, the diamond substrate with the Ti/Pt/Au electrodes was annealed in a H_2 atmosphere for 30 min at 500 and 600 °C via point-arc MPCVD. During this process, TiC was formed between the p++ diamond layer and electrodes (Fig. 4.9 (b)).

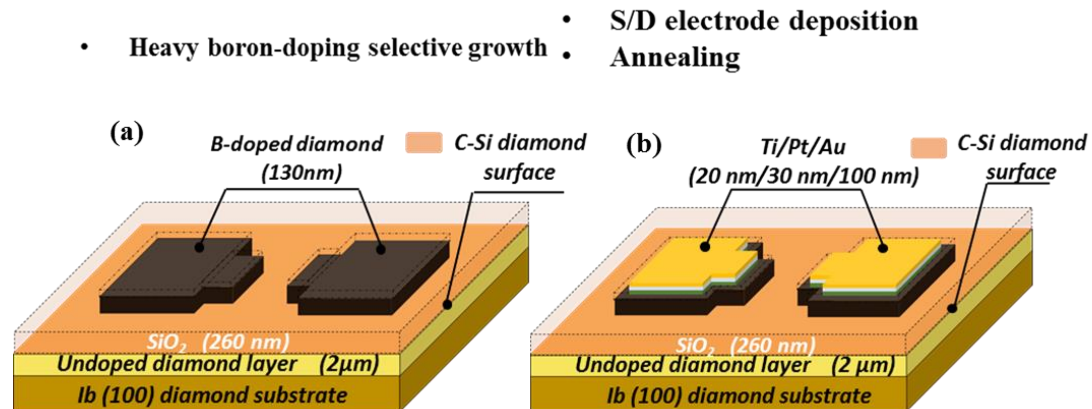


Fig. 4.9. (a) The 130nm boron-dope diamond selective growth via MPCVD, and the C-Si diamond surface was formed in this process. (b) Source and drain electrodes deposition and the Ti/Pt/Au electrodes was annealing process.

To retain the C-Si channel and the SiO_2 film in the MOSFETs channels, ICP-RIE was used to remove the SiO_2 and C-Si from the channel, and the gate width (W_G) of each device was 25 μm. Afterwards, oxygen plasma was used to remove the residual C-H on the diamond surface and isolate each MOSFET. Thereafter, a 100 nm Al_2O_3 layer was deposited as the passivation layer on the surface of the MOSFETs through high-temperature (450 °C) ALD. Herein, the Al_2O_3 layer prevents the source/drain electrode and thus preventing a short circuit between the source-drain electrode and the overlapping gate, and the negative fixed charge in the Al_2O_3 can provide a weak electric field between the insulating films, which can improve the mobility and current density of the C-Si diamond MOSFETs. However, it evidently has a reverse effect on the

realization of a normally-off operation. The thickness and deposition temperature of the ALD-Al_2O_3 layer are very important in the fabrication of the C-Si diamond MOSFETs.

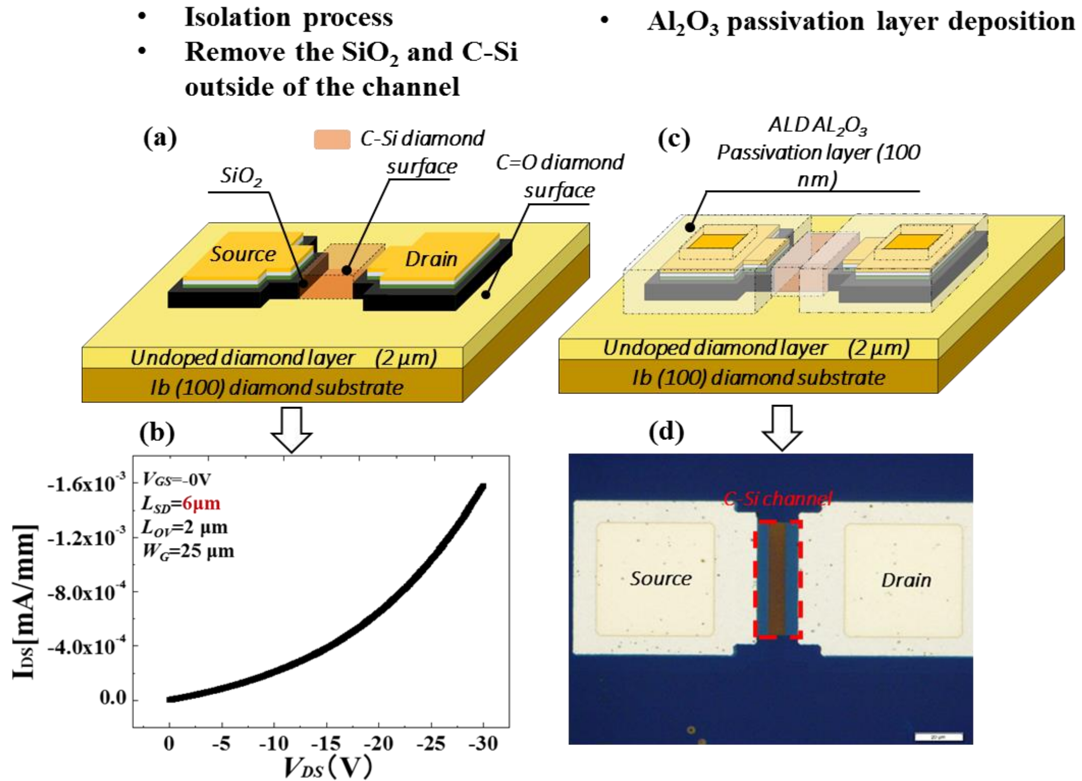


Fig. 4.10. (a) The isolation processes via ICP-RIE and oxygen plasma to remove the SiO_2 and C-Si diamond surface where out of the channel region. (b) Characteristic current between source and drain of the C-Si MOSFET with L_{SD} = 6 μm after isolation process. (c) 100 nm ALD Al_2O_3 layer was deposition and source/drain contact area etching using the NMD-3. (d) Optical microscope photograph of the C-Si diamond MOSFET after the ALD process, the C-Si channel covered with SiO_2 was indicated.

The current between the source and drain of the C-Si MOSFET without gate electrode with L_{SD} = 6 μm after device isolation process during the C-Si diamond MOSFETs fabricating is shown in Fig. 4.10 (b). According to the I_{DS}–V_{DS} characteristic of the C-Si diamond MOSFET before the ALD passivation layer and gate electrode deposition, the I_{DS} is in very low level at -1.6×10^{-3} mA/mm (-4×10^{-8} A) at V_{DS}=-30 V, there is almost no current passes through the source/drain without gate bias, The SiO_2/diamond

interface is expected to be normally-off channel. This result is different with the C-H diamond as a channel between the source/drain electrodes completely, the 2DHG will induced even without gate bias and there should be have current flow. However, in case of the C-Si diamond surface with the SiO_2 insulator, there is a shortage of hole carriers and no conductive channels are being generated. It might be due to the positive fixed charge in SiO_2 film, which deplete the holes without gate electrode. So, the C-Si MOSFET is expected to be normally-off operation.

Finally, 100 nm of Al was used to form the overlapping gate of the C-Si MOSFETs (Fig. 4.11). The gate-source and gate-drain overlap length (L_{OV}) of the MOSFETs was 2 μm, and the length between the source and drain electrodes ranged between 14–22 μm. The diamond was metal-like owing to the 130 nm heavily B-doped selectively grown diamond (B concentration: ~10^{21} cm^{-3}). In addition, it can be clearly observed that the metal electrode is plated on the p+ selectively grown diamond layer. The margin region between the source/drain metal and p+ selectively grown diamond layer is 5 μm (Fig. 4.11 (b) (d)). The actual length from source to drain (L_{SD}) should be the distance between the selected growth regions; this was the C-Si channel length in the C-Si MOSFETs (4–12 μm).

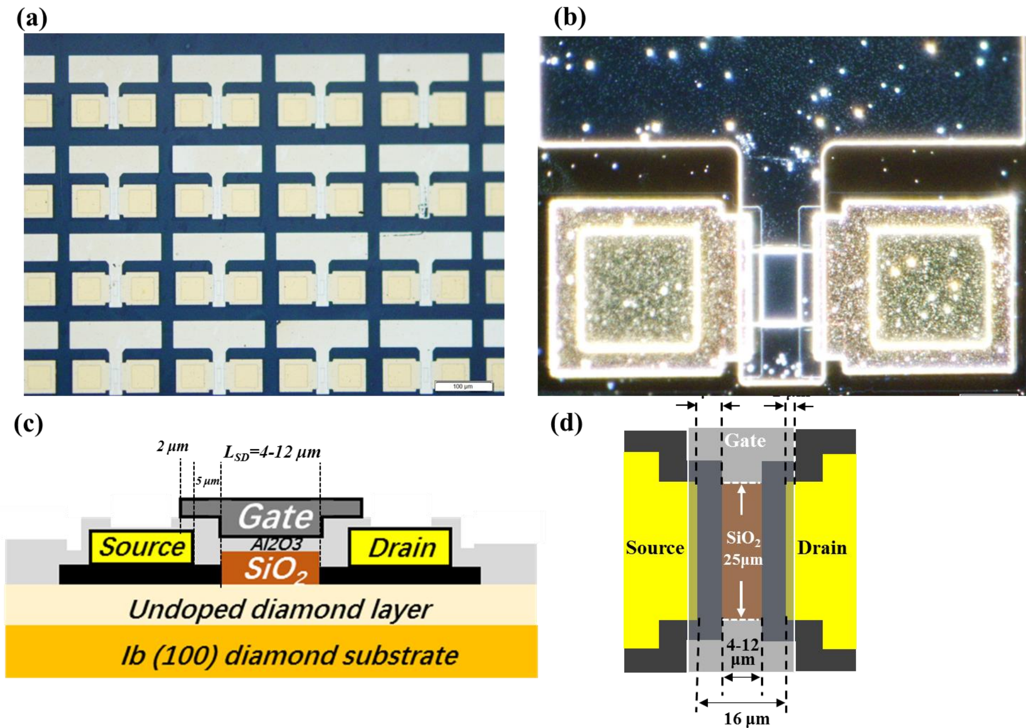


Fig.4.11 (a) Optical microscope photo of the completed C-Si Diamond MOSFET (b) Differential Interference Contrast Microscope picture of the C-Si diamond MOSFET with overlapping gate (c).(d) Top view between source and drain electrodes of the C-Si diamond MOSFET.

The scanning electron microscope (SEM) photos by focused ion beam method were shown in Fig.4.12, the Fig.4.12(a) and (b) were the SEM photo of the whole body and the source-drain region of the C-Si MOSFET with LSD=10 µm, respectively. By enlarging the scanning area of channel via SEM, the different layers in section area can be observed clearly (Fig.4.12 (c)), the layers are Al, Al2O3, SiO2, C-Si layer and diamond from top to bottom in the Fig.4.12 (d), Fig.4.12 (e) shows the section area near the source region and the selective growth B-doped diamond also can be confirmed, and the detailed SEM photo in the channel region of the C-Si diamond MOSFET is shown in Fig.4.12 (f).

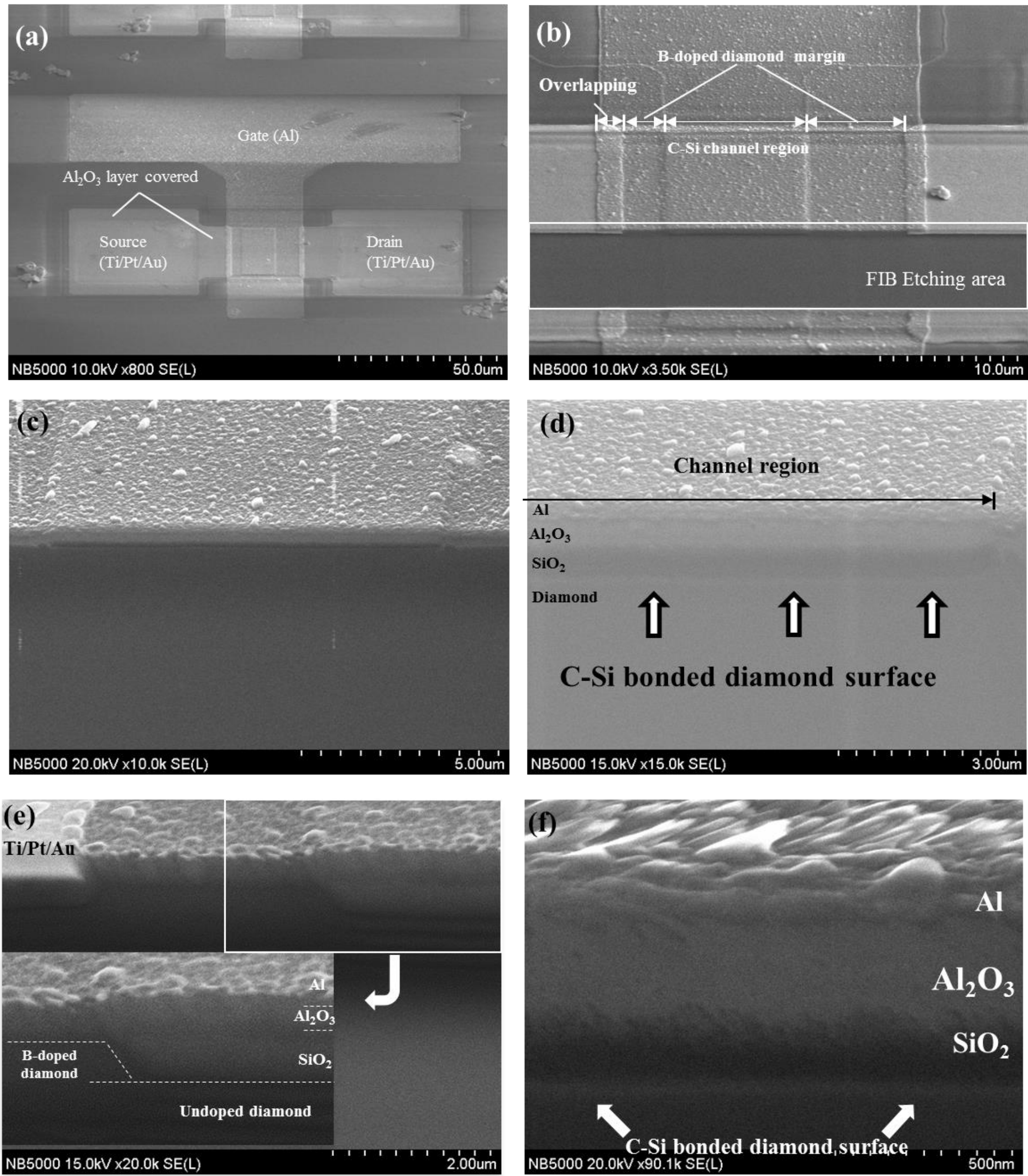


*Fig.4.12 (a) SEM photo of the C-Si diamond MOSFET with L_{SD}=*10 μm. *(b) The SEM photo of the channel region after the ion beam etching .(c)and (d)are the section photo of the gate electrode covered area.(e) Section photo by FIB-SEM in near the source electrode area. (f) Area enlarged FIB-SEM section photo in the channel region of the C-Si diamond MOSFET.*

4.3.1 Electrical characterization of the C-Si bonded diamond MOSFETs

DC measurement is adopted for the electrical characteristic measurement. The overlapping-gate C-Si MOSFETs were placed in a high-voltage measurement system (B1500A, Agilent) to measure the electrical characteristics at room temperature (300 K). Fig. 4.13 shows the V_{DS}–I_D and V_{GS}–I_D characteristics of the C-Si diamond MOSFETs with the L_{SD} = 12 μm, and the tested V_{DS} ranged from 0 to -30 V whereas V_{GS} ranged from -40 to 20 V (△V_{GS} = 4 V). The C-Si diamond MOSFET with L_{SD} = 12 μm shows a normally-off operation (threshold voltage V_{TH} = -5.1 V) with an excellent field-effect mobility (μ_{FE}) of 140 $cm^2V^{-1}s^{-1}$. μ_{FE} was calculated as follows:

$$\mu_{\mathrm{FE}} = \frac{g_m L_{SD}}{C_{oxide}|V_{DS}|}$$

$$C_{oxide}^{-1} = C_{SiO2}^{-1} + C_{Al2O3}^{-1} \quad (\varepsilon_{SiO2} = 3.9,\ \varepsilon_{Al2O3} = 8.9)$$

Notably, when calculating μ_{FE}, the thickness of the SiO_2 insulating film should be reduced appropriately. During fabrication of this MOSFET, the target value of the SiO_2 film thickness in the TEOS-CVD is approximately 260 nm. However, the film thickness will differ according to the placement position of the sample in the TEOS-CVD deposition. In addition, the SiO_2 mask should be etched slightly during MPCVD selective growth. This is also shown in the SIMS results (the thickness of the

SiO_2 film thickness of the SIMS sample before MPCVD is approximately 220 nm. However, the total thickness of the oxide above the diamond in the results (shown in Fig. (4.5) after selective growth is approximately 180 nm, indicating that SiO_2 is etched by approximately 40 nm under similar fabrication conditions). Therefore, the thickness of the SiO_2 film is 220 nm. g_m is the maximum transconductance, and it is obtained

from the value of V_{DS} in the linear region of the V_{DS}–I_D characteristics (@V_{DS} = -10 V).

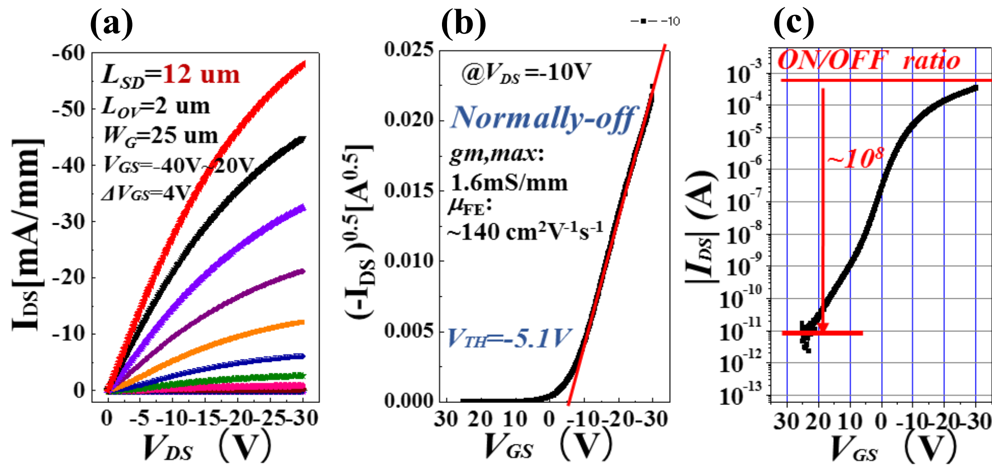


Fig. 4.13. (a) (b) V_{DS}–I_D and V_{GS}–I_D characteristics of the C-Si diamond MOSFETs with L_{SD} =12 μm, the maximum current density is -58 mA/mm and the gm.max is 1.6 mS/mm of the MOSFET, and it shows normally-off operation with the V_{TH}=-5.1 V @V_{DS}=-10 V, the on/off radio (c) is 10^8 A at room temperature (300 K).

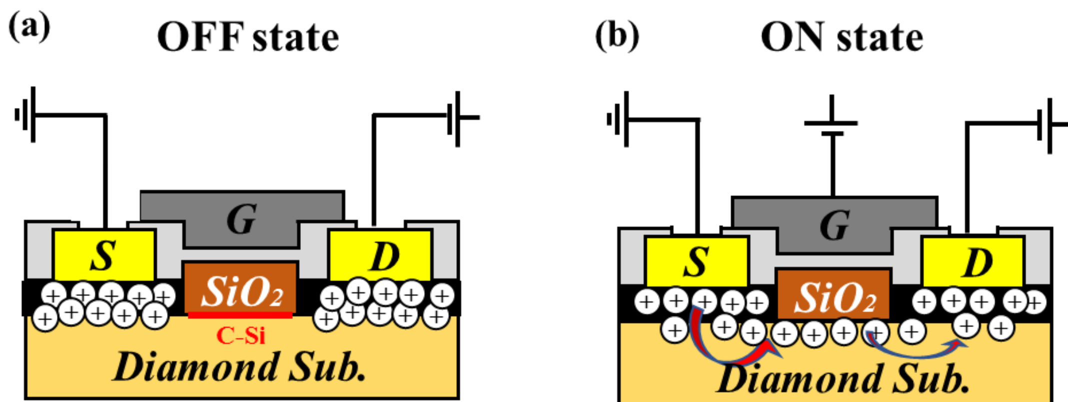


Fig. 4.14 (a) The C-Si diamond MOSFET in off-state, and there are almost no hole carriers in the channel region.(b)Hole carriers under C-Si channel area of C-Si diamond MOSFET in OFF/ON state. When a negative voltage is applied to the gate electrode, holes existing in the source/drain B-doped selective growth diamond region are attracted to the channel, and the C-Si diamond MOSFET is turned on.

The mechanism of the C-Si diamond MOSFET in the off-state and on-state is shown in Fig. 4.14. This is different from the C-H diamond MOSFET with an Al_2O_3 insulator with a negative charge [21], almost no hole carriers exist under the C-Si diamond surface when no negative voltage is applied to the gate metal of the device. This may be owing to the existence of a small amount of positive fixed charges in the SiO_2 insulating film. The positive fixed charges in the SiO_2 film proposed to depleted the negative fixed charges in the Al_2O_3 film, or the hole carriers induced by the C-Si dipoles polarization. Without negative gate bias to the C-Si diamond MOSFET, the C-Si dipoles under the gate electrode region could not generate enough hole carriers to forming a 2DHG channel to turn on the MOSFET, and the device showed a normally-off operation. On the contrary, when a negative voltage is applied to the gate, hole carriers are formed under the C-Si bonded surface under the action of the electric field, and the hole carriers existing in the selectively grown diamond region are attracted to the channel region, the 2DHG channel is formed, and the C-Si diamond MOSFETs turn to the on-state.

The C-Si diamond MOSFETs with L_{SD} = 10 μm, 8 μm, and 6 μm show normally-off characteristics with μ_{FE} of approximately 100 $cm^2V^{-1}s^{-1}$, and the on/off ratio is 10^8 at 300 K (shown in Fig. 4.15). However, the threshold voltage of the devices does not show significant regularity. This is because it is difficult to control the charge in the SiO_2 insulator film completely during fabrication. Furthermore, during selective growth, the position of the plasma affects the reaction temperature of the SiO_2 diamond interface, thus affecting the depth of H atoms entering the SiO_2 insulating film, which is one of

the reasons affecting the threshold voltage.

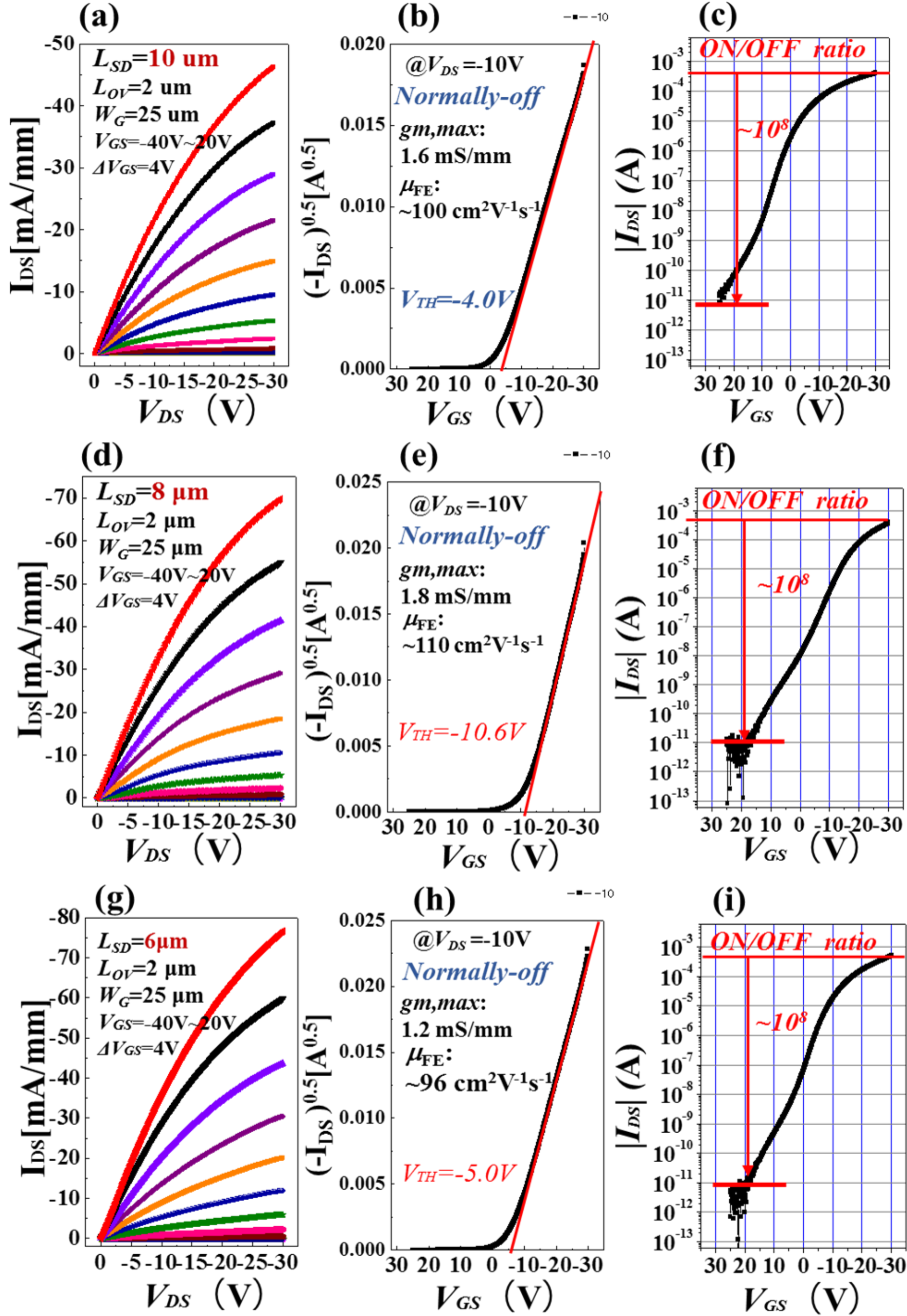


Fig. 4.15. V_{DS}–I_{DS} and V_{GS}–I_{DS} characteristics of the C-Si diamond MOSFETs with (a, b) L_{SD} =10 μm, (d, e) L_{SD} = 8 μm, (g, f) L_{SD} =6 μm. These devices have the same dimensions except L_{SD}, and all show normally-off operation with the μ_{FE} of approximately 100 $cm^2V^{-1}s^{-1}$, those devices show high on/off ratio of 10^8 at 300 K.

4.3.2 Wide temperature operation of the C-Si diamond MOSFET.

A few MOSFETs show normally-on operation with a short channel length. However, these devices exhibit high current density and transconductance. The V_{DS}–I_D and V_{GS}–I_D characteristics of the C-Si diamond MOSFET with L_{SD} = 4 μm at 300 to 673 K are shown in Fig. 4.16 (a) and (b), respectively

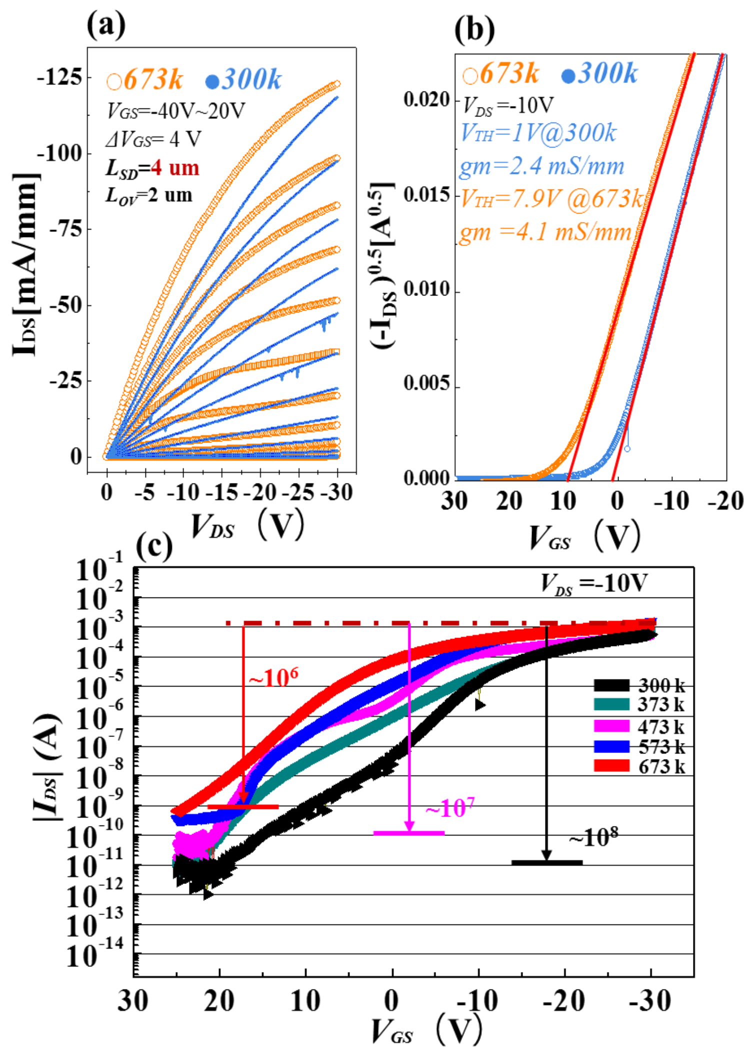


Fig. 4.16. (a) Composite V_{DS}–I_D and (b) V_{GS}–I_D characteristics of the C-Si diamond at 300 and 600 K. (c) On/off ratio of C-Si diamond MOSFET from 300–673 K.

The blue V_{DS}–I_D characteristic curve shows that the maximum current density ($I_{D.max}$) is -118 mA/mm (Ron=7x10^3 Ω at V_{DS} = -5 V) and the ^-g_m is 2.4 mS/mm at V_{DS} = -10 V at 300 K. The MOSFET shows normally-on operation with V_{TH} = 1 V. At 673 K (orange characteristic curve), $I_{D\cdot max}$ was -124 mA·mm^{-1} (Ron=4x10^3 Ω at V_{DS} = -5 V), g_m was 4.1 mS·mm^{-1}, and μ_{FE} increased from 108 to 188 cm^{2}V^{-1}s^{-1}. However, in a high-temperature environment, the threshold voltage shifts to 7.9 V.

Compared to that at room temperature (300 K), the current density of the MOSFET in a high-temperature environment does not increase significantly, but the current saturation speed is enhanced. This is because the B concentration in the (100) diamond in the boron-doped selectively grown diamond is not uniform. The lower B concentration at the bottom of the selectively grown diamond [22] causes contact resistance with the undoped diamond layer. When the temperature increases, the resistance between the B-doped and undoped diamonds decreases, where the activation energy of boron is 0.38 eV [22]. This increases the hole carrier concentration in the diamond and decreases the ohmic resistance of the source and drain electrodes of the MOSFETs [23], which enhanced the g_m of the device.

The turn-off current gradually increases with the increase in temperature. Fig. 4.16 (c) shows the V_{GS}–I_D characteristics of the C-Si MOSFET with increasing temperature. At 300 K, the drain-off current is significantly low at 10^{-11} A (at V_{DS} = -10 V) and the on/off ratio is 10^8. The on/off ratio is approximately 10^7 at 473 K and 10^6 at 673 K.

Therefore, the wide temperature range operation of the C-Si diamond MOSFETs was

confirmed, and the C-Si diamond MOSFETS exhibited normal operation and good on/off radio at high temperatures.

4.3.3 Analysis of the C-Si diamond MOSFET switching application

In Chapter 3, we discuss the realization of a normally-off operation of the C-H diamond MOSFET using a diamond cascode circuit, and diamond cascode embodies the excellent electrical characteristics of the diamond device and excellent gate control capability of the enhanced Si MOSFET. Additionally, the C-H diamond MOSFETs are used as p-type power devices in high-voltage inverter circuits through diamond cascode, and inverter operation is realized.

In general, the development direction of diamond devices in integrated circuits in the future is to realize high-performance normally-off 2DHG diamond MOSFETs. Herein, the C-Si diamond MOSFET realizes a normally-off operation with high mobility and high current density. However, the breakdown voltage of the current C-Si diamond MOSFET is not very high (lower than 100 V) because of its overlapping gate structure, but it is suitable for CMOS switching circuits with low supply voltage to implement a NOT- logic gate.

The CMOS (C-Si CMOS) inverter circuit is composed of a C-Si diamond MOSFET (measured in Fig. 4.13.). The n-type Si MOSFET product (TK100E10N1) is shown in

Fig. 4.17 (a), and the input/output waveform is shown in Fig. 4.17 (b). In Fig. 4.17 (c) and (d), as a control group, the diamond cascode discussed in Chapter 3 combined with the C-H diamond MOSFET (W_G = 25 μm, Chapter 3 Fig. 3.3) is used as a p-type device to form a CMOS inverter switching circuit with similar n-type Si MOSFET (C-H CMOS).

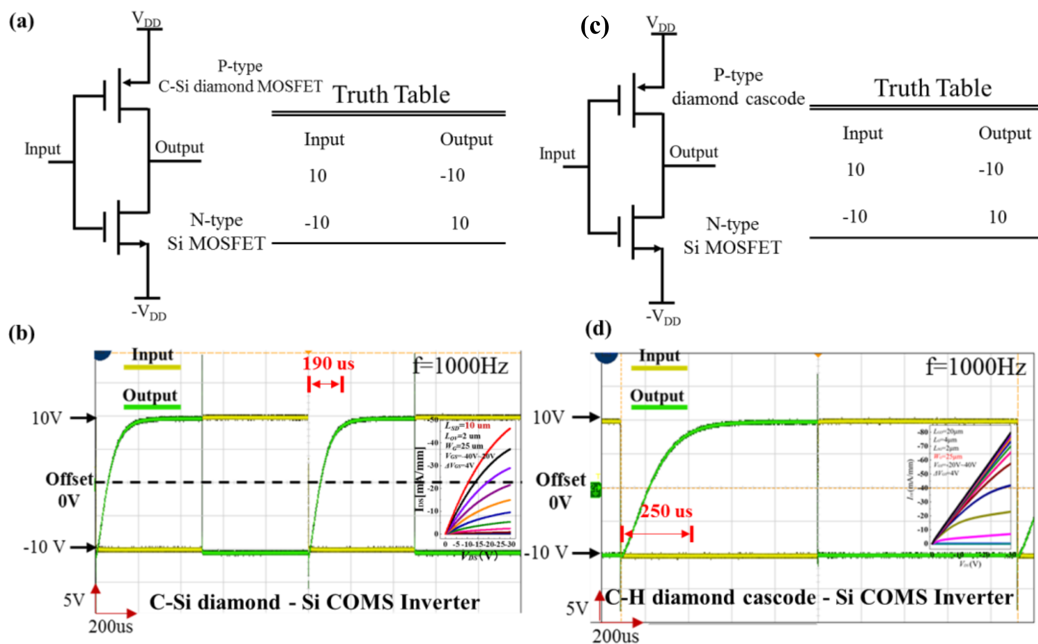
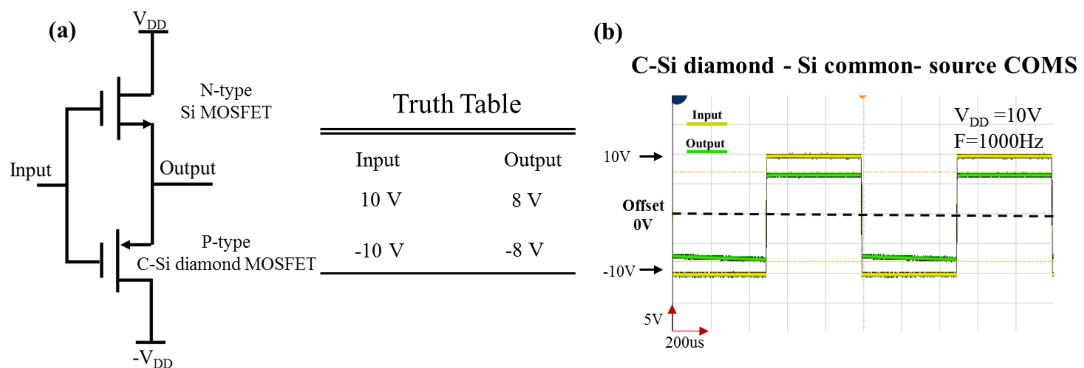


Fig 4.17 (a) Schematic CMOS NOT logic gate composed of the normally-off C-Si diamond MOSFET and (c) C-H diamond cascode as a p type device. (b) and (d) input/output waveform of the C-Si CMOS and the C-H CMOS, respectively.

The C-Si CMOS switching circuit operation with a turn-on time of 190 μs was confirmed, and the C-H CMOS switching circuit exhibited a turn-on time of 250 μs under similar test parameter. Compared to that of the diamond cascode applied at low voltage, the response speed of the C-Si diamond MOSFET is faster. However, because the C-Si diamond MOSFET has a large gate length and an insulating film thickness of 320 nm, the charging time of the gate capacitor affects the switching speed when the

device is turned on.

In the Chapter 3, a common source CMOS inverter switching circuit structure, which has fast charge and discharge speed, is discussed. In Fig. 4.18 (a), the C-Si diamond MOSFET is also applied to the inverter circuit for testing. The input/output waveform shows that the output signal and the input signal realize the same phase and almost no delay switching waveform, but the output waveform does not reach a supply bias of ±10 V. This is because although the charge and discharge speed of the capacitor in the MOSFET has been improved, the C-Si diamond MOSFET has not reached saturation when V_{GS} = -5 V and V_{DS} = -10 V.



Truth Table

Input	Output
10 V	8 V
-10 V	-8 V

Fig 4.18 (a) Schematic common-source CMOS inverter composed of the p-type C-Si diamond MOSFET and the n-type Si MOSFET. (b) Input/output waveform of the CMOS inverter.

4.4 Conclusions

In this chapter, the formation of the C-Si bonded diamond surface is realized at a diamond/SiO_2 interface through MPCVD at a high temperature of over 800 °C and a reducing gas atmosphere of H_2 and CH_4. This is different from the thermal oxidation treatment in fabrication technology of the Si device. The C-Si-bonded layer is formed at the diamond/SiO_2 interface, and it reduces the interface state owing to the C-Si-O bonds at the interface but not the C-O surface. Additionally, it decreases the fixed charges in the SiO_2 insulator, which can improve the μ_{FE} of the C-Si MOSFETs. The C-Si diamond MOSFETs show a normally-off operation and the 2DHG is formed in the channel region at the diamond surface with a negative gate bias. The selective growth of the B-doped diamond by SiO_2 masking under the source/drain electrode improves the ohmic resistance and performance of the MOSFETs. The C-Si MOSFETs can work in a high-temperature environment, and they exhibit excellent temperature stability and the characteristics of CMOS applications have been confirmed.

Herein, the C-Si diamond MOSFET with a thinner SiO_2 insulating film was fabricated. Figs. 4.15 (a) and (b) show the Al_2O_3/SiO_2 insulator with a thickness of 100 nm/100 nm in the C-Si diamond MOSFET and its electrical characteristics. The V_{DS}–I_{DS} and V_{GS}–I_{DS} characteristics of this C-Si diamond MOSFET with L_{SD} = 12 μm show a higher current density of -110 mA/mm (@V_{GS} = -40 V, V_{DS} = -30 V), which is approximately 1.5 times higher than that of the device with thicker SiO_2 insulating film, but the

threshold voltage is shifted to -0.2 V. Notably, the thinner the SiO_2 insulating film in the C-Si MOSFET, the stronger the polarization effect owing to the negative fixed charge in Al_2O_3 on the C-Si channel region, which causes the device to be closer to normally-on. This device shows an excellent mobility (μ_{FE} is 122 $cm^2V^{-1}s^{-1}$.)

In contrast, if the insulating film above the C-Si diamond MOSFET is entirely replaced with SiO_2, the device will show better normally-off characteristics, and the C-Si diamond MOSFET with insulating film of SiO_2/SiO_2 = 50 nm/100 nm and its V_{DS}–I_{DS} and V_{GS}–I_{DS} characteristics shown in 4.19 (c) (d).

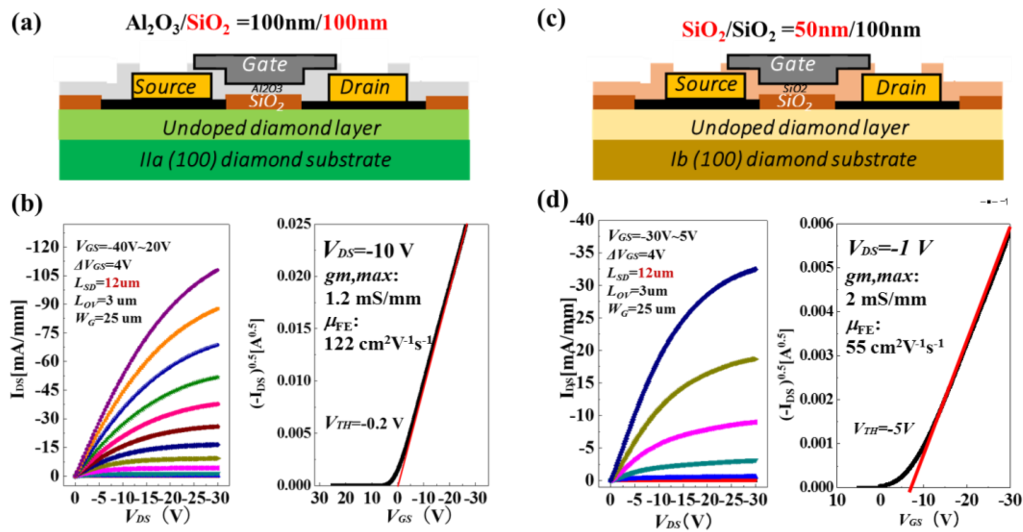


Fig 4.19. (a) Sectional model of the C-Si diamond MOSFET with insulating film of Al_2O_3/SiO_2 = 100 nm/100 nm and its V_{DS}–I_{DS} and V_{GS}–I_{DS} characteristics shown in (c) The sectional model of the C-Si diamond MOSFET with insulating film of SiO_2/SiO_2 = 50 nm/100 nm and (b) is the V_{DS}–I_{DS} and V_{GS}–I_{DS} characteristics of this MOSFET.

The device without Al_2O_3 insulating film shows low current density and good normally-off operation (V_{TH} = -5 V), the μ_{FE} of this MOSFET is 55 $cm^2V^{-1}s^{-1}$. Based on the C-Si diamond MOSFET discussed herein, the fixed charge in the insulating film

has an influence on the threshold voltage of the device. Today, the threshold voltage is unstable because the type and quantity of the fixed charge in the insulating film cannot be controlled effectively. To stabilize the threshold voltage by adjusting and controlling the fixed charge in the insulating film of the C-Si devices using ion implantation technology (fluoride ion implantation), and expanding the W_G of the device to fabricate high current normally-off C-Si diamond power devices is the next step for C-Si diamond devices in power conversion applications.

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Chapter 5

Summary

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Summary

The focus of this doctoral thesis is on two key aspects: the first is the manufacture of high-performance normally off diamond MOSFETs, the second is the analysis of the performance of diamond devices in circuits.

Expanding the size of the diamond device in a circuit is the most direct approach to enhance the current output performance of the device. Due to the specificity of the surface conductivity of hydrogen-terminated diamond, and the insulation of oxygen-terminated surfaces, the fabrication of high-performance power devices with diamond as a semiconductor substrate has more advantages than the current mainstream semiconductor materials.

In this work, for the large gate width lateral-type diamond MOSFET, the gate width was widened to 500 μm and the drain current output (50 mA) was found to be nearly 20 times that of the C–H diamond MOSFET with $W_G = 25$ μm. Further broadening of the gate width of lateral-type diamond MOSFETs may prove to be difficult. The first reason is that the size of the diamond substrate limits the area of the device, the second reason is that a long gate width will inevitably require gate electrodes that match the width, which will increase the difficulty of fabrication and reduce the fault tolerance in the experiment.

In the experiment, a lateral-type diamond device with a gate width of more than 10mm was produced, but the production of the source electrode became exceedingly demanding. After fabrication, the device showed only a lower current value owing to

the metal fracture of the gate electrode in the lift-off process (Fig.5.1). Therefore, in the production of high-drain current diamond devices, vertical-type devices are a viable proposition for future developments. In the vertical-type diamond MOSFET, the maximum value of I_{DS} was -90 mA with W_G = 1 mm and −185 mA with W_G = 5 mm. The maximum output current of the diamond MOSFET is enhanced by increasing the gate width.

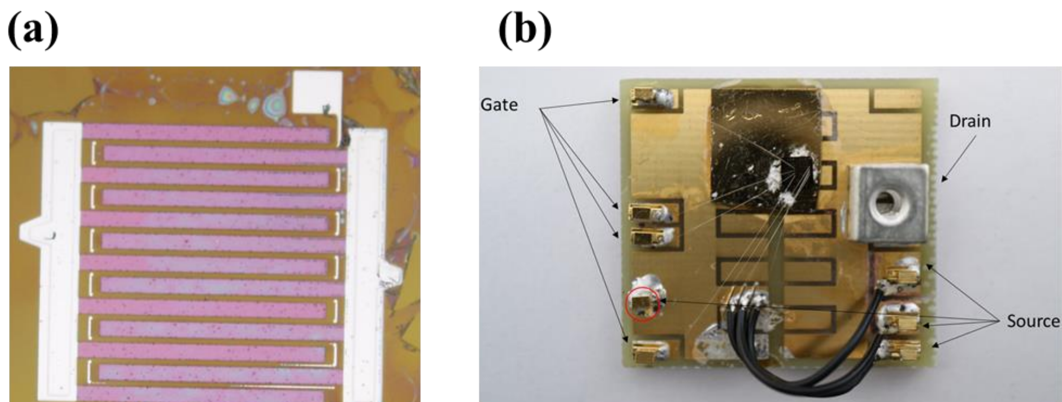

Fig. 5.1 (a) The large gate width lateral-type diamond MOSFET fabricated in the experiment, which failed due to gate metal fracture. (b) Packaging of vertical-type diamond MOSFET through external wiring.

In the application of the circuit, a diamond cascode circuit was used to achieve a high reliability off-operation and a low current loss. Stable threshold voltage control was achieved through a low-voltage enhancement Si MOSFET, as the threshold voltage of the diamond cascode is determined by the Si MOSFET. The diamond cascode demonstrates the advantage of high breakdown voltage in diamond devices, reaching a breakdown voltage of -1735 V. We used a diamond cascode as a p-type power device in the double-stage diamond–GaN half-bridge complementary inverter to achieve high-

speed and high-voltage inverter characteristics with one gate driver inverter. This is also the first application of diamond devices in the field of high-voltage inverter circuits. It should be pointed out that because of the small size of the diamond device, it can only be built through the B1500A system. The experimental results will inevitably be affected by parasitic resistance and capacitance in the circuit. Therefore, diamond packaging technology is important for power conversion applications in the future. Fig 5.1 (b) shows a sample diagram of a vertical-type diamond MOSFET packaged with Pt metal wires. As the Pt wire was too thin and had a low fuse, the sample short-circuited due to the fusing of the wire during the test, but this is a very important attempt in the general direction of diamond device packaging. In the future, the insulating filler can be improved and higher melting points should be achieved. The metal wire is encapsulated, which is useful for realizing the commercialization of diamond devices.

In this work, a completely new method for realizing high-performance normally off diamond MOSFETs is proposed. A C-Si dipole was used to replace the C–H dipole to form a few C-Si bonded layers on the SiO_2/diamond interface. These layers can be used as the channel of a C-Si diamond MOSFET.

It is worth noting that the formation of the C-Si bonded layer is due to the effect of high temperature and reducing gas, which break the Si–O bond in SiO_2 to form a dangling bond, which combines with the dangling bond on the diamond surface to form a C-Si bond layer. This condition is also the growth condition of diamond, which means that while using SiO_2 as a selective growth mask for boron-doped diamond selective

growth, it also completes the production of the MOSFET channel and insulating film. Which is very efficient in the manufacturing process of diamond devices. Owing to the low interface state density and few positive fixed charges in SiO_2, the C-Si diamond MOSFET shows a normally off-operation with excellent field-effect mobility, and surpasses C-H diamond MOSFETs that realize a normally off-operation through surface modification. The C-Si diamond MOSFET also achieves good stability over a wide temperature range. These properties also provide the possibility of making C-Si diamond power devices for power conversion applications with high drain current and high breakdown voltage. Integrated circuit applications with low loss and high switching speed may also be possible in the future.

List of research achievements

Paper:

T. Bi, J. Niu, N. Oi, M. Inaba, T. Sasaki, H, Kawarada, "Application of 2DHG Diamond p-FET in Cascode with Normally-off Operation and Breakdown Voltage of Over 1.7 kV", IEEE Trans. Electron Devices, 67, 10, 4006-4009,(Oct. 2020)(DOI: 10.1109/TED.2020.3019020) .

T. Bi, Y. Chang, W. Fei, M. Iwataki, A. Morishita, Y. Fu, N, Niikura, H. Kawarada"C-Si Bonded Two-Dimensional Hole Gas Diamond MOSFET with Normally-off Operation and Wide Temperature Range Stability", Carbon, 2021 (accepted)

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