Graduate School of Fundamental Science and Engineering
Waseda University

# 博　士　論　文　概　要
# Doctoral Dissertation Synopsis

論　文　題　目
Dissertation Title

## Hardware Optimization of Stochastic Computing

## ストカスティックコンピューティングのハードウェア最適化

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The number of hardware devices used in our everyday lives has been growing rapidly. For example, most people in the whole world owns a smartphone, very large amount of money are deposit in bank systems, and even crucial systems such as automobiles and planes are controlled by computer systems. Not only the amount, developing hardware devices on ones own has been realistic. For example, Xilinx Inc. has developed low-cost and highly integrated System on Chips (SoC) products which integrates software programmability of an ARM-based processor with hardware programmability of an FPGA (Field-Programmable Gate Array) core. Therefore, developing high-functioning hardware devices became more easily than ever. When implementing applications on hardware, not so much precision is required in many areas such as image processing and machine learning. Instead of high precision with larger circuit size, smaller circuits are desired due to the increasing amount of data and more complex operations. For its small-sized implementation, compared with conventional computation, approximate computing is attracting interest.

Stochastic computing (SC) is one of the approximate computing methods, aiming to miniaturize circuits by allowing errors in calculation results. SC repeats bit-level logical operations to achieve stochastic arithmetic operations using stochastic numbers (SNs). SNs are bit streams whose values are defined by the appearance rates of 1's in their bit streams. In SC, SNs' bit streams are input into simple logic circuits sequentially for arithmetic calculations. For example, an AND gate, a MUX circuit, and a NOT gate implement multiplication, weighted addition, and inversion, respectively. Hence, SC enables smaller-sized implementation compared with binary computing and was applied to many hardware applications such as neural networks and image processing. Other than its small-sized hardware implementation, SC has many characteristics. For example, SC has noise resiliency. This is because all the bits of the bit streams of SNs have the same weight. This means that when one bit of an SN is mistakenly flopped, the value of an SN has small errors. On the other hand, when one bit of a binary number is flopped, the value can have error of half the range in maximum. With this characteristic, SNs have been applied to reliable systems. SC also has the flexibility over accuracy and SNs are recursive, i.e., the SC-based circuits can change their accuracies by only changing the length of the inputs, without changing their circuits.

Even with these merits, SC is yet to be used in practical situations. One reason for this is: SN-to-binary converter is required for calculation, but its hardware cost is large. Then, why is SN-to-binary conversion required? There are two main reasons: To guarantee the independency of the bit streams of SNs; To implement steep or discontinuous functions such as step function. The root cause of

the first reason is the dependency of bit streams of SNs. To obtain the correct calculation result, the bit streams of the input SNs must be independent. The second reason is especially required to implement activation functions, such as the Rectified Linear Unit function, the step function, and their composite functions. However, without re-generation of SNs, no steep or discontinuous functions were proposed alone. The problem of SN-to-binary conversion is its large hardware cost. In terms of circuit area, SN-to-binary conversion, when 255-bit SNs are generated, costs more than 50 times larger compared with an SN multiplier. Not only the case of circuit area, SN-to-binary conversion also requires large latency. If SN-to-binary converters are used in series, 255 clock cycles per converter are required after the first input bit to output the first output bit. In addition, flexibility over accuracy is lost due to this conversion.

To solve these problems, we aim to omit the use of SN generator as much as possible, proposing two types of circuits: SN duplicators; and a step function circuit with its applications. This dissertation proposes hardware optimization of SC, especially to omit use of SN generators. This dissertation is organized as follows:

Chapter 1 describes the backgrounds and overview of this dissertation.

Chapter 2 proposes FSR (Flip-flop Selecting circuit using a Random bit stream) and RRR (Register based Re-arrangement circuit using a Random bit stream) duplicators, which generate and output new SNs which have the same value and independent bit streams. In SC, the bit streams of the input SNs must be independent to obtain the correct calculation result. In many functions, two or more identical values are input. In these cases, duplicating SNs, or re-generating SNs with the equivalent value and independent bit stream, is required. In a conventional method, a flip-flop is used to delaying one bit of the input SN, creating a different, 1-bit delayed bit stream. Since the output SN has the (nearly) same value and different bit stream compared withe the input SN, this circuit can be said to have duplicated an SN. However, the output SN's bit stream is always the same if the same input SN is given. As mentioned above, if bit streams of the duplicated SNs are dependent on each other, their arithmetic operation results become inaccurate. In this chapter, a randomized bit stream is introduced to re-arrange the bits stored in flip-flops. The SNs duplicated by the proposing FSR and RRR duplicators have the equivalent values but have independent bit streams, by effectively utilizing bit re-arrangement using randomized bit streams. Experimental evaluation results demonstrate that the RRR duplicator obtains more accurate results, reducing the mean square errors by 20%–89% compared with a conventional SN duplicator.

Chapter 3 proposes $2^n$RRR duplicator, which uniquely extends the RRR

duplicator and has a scalable structure by changing the numbers of flip-flops for bit re-arrangement. As a nature of SC, changing the length of the input SNs will change the whole circuit's accuracy. However, in some implementations with re-convergence paths, the circuit itself will cause errors due to the dependency of the SNs, i.e., the length of the input SNs does not change that circuit's accuracy. In this chapter, we extend the RRR duplicator proposed in Chapter 2, enabling to change the accuracy of the circuit itself. The proposing $2^n$RRR duplicator outputs different SNs every time and are all independent of each other. The $2^n$RRR duplicator can be theoretically proved to flexibly change the accuracies of the arithmetic circuits. Also from the experimental evaluation results, this chapter clarifies that the $2^n$RRR duplicator enables accuracy-flexible circuits. In a particular case, one instance of the proposed $2^n$RRR duplicator reduces the mean square errors by more than 50% compared with the RRR duplicator proposed in Chapter 2.

Chapter 4 proposes step function in SC and its applications. With the rise of neural network and image processing, implementation of activation functions are becoming popular. Implementation of steep functions and discontinuous functions, such as activation functions, is indispensable for the practical application of SC. However, when implementing arithmetic operations in SC, there is a constraint that the original function must be differentiable. Some steep functions have been proposed, but can only be used in specific situations, and not alone. To solve the problems of the conventional methods, this chapter firstly proposes hardware implementation of step function. The proposing circuit of utilizes flip-flops and an adder to perform as step function uniquely calculating the stored bits in the flip-flops. The proposed step function can be theoretically proved to perform as a step function. This chapter confirms that the proposing circuit behaves as a step function through experimental evaluations. Also as an application, steep functions or discontinuous functions can be realized by applying the discontinuity of the step function. As a steep function, this chapter also proposes hardware implementation of absolute function and discontinuous function, by synthesizing an arbitrary function as a discontinuous function. As an example, a composite function of trigonometric function of sin and cos function is implemented in this chapter. Through experimental evaluations, this chapter confirms that the circuits of step function, absolute function, and discontinuous function perform as target function.

Chapter 5 summarizes this dissertation and gives future directions on hardware optimization of SC. In conclusion, hardware optimization of SC has future prospect. However, there remain several tasks to be done soon. Further optimization and practical applications are our future works.

# List of research achievements for application of Doctor of Engineering, Waseda University

Full Name :石川　遼太　　seal or signature

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| 種類別<br>(By Type) | 題名、 発表・発行掲載誌名、 発表・発行年月、 連名者（申請者含む）<br>(theme, journal name, date & year of publication, name of authors inc. yourself) |
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# List of research achievements for application of Doctor of Engineering, Waseda University

Full Name :石川　遼太　　seal or signature

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| 種類別 (By Type) | 題名、 発表・発行掲載誌名、 発表・発行年月、 連名者（申請者含む） (theme, journal name, date & year of publication, name of authors inc. yourself) |
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